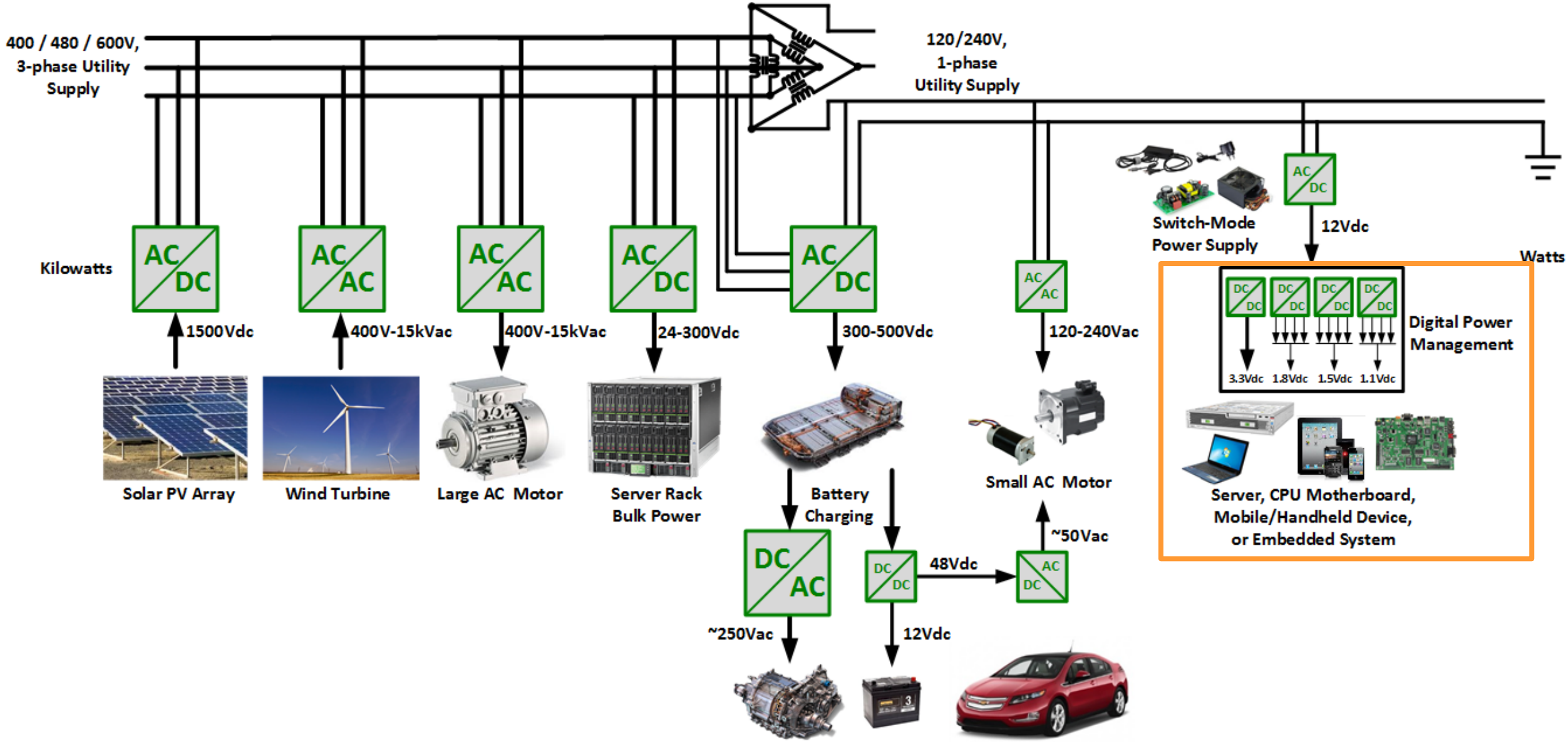
Digital Power Management, Power Integrity, and Power Rail Sequence Analysis & Testing

Ken Johnson

February 1, 2017 (DesignCon, Santa Clara, CA)

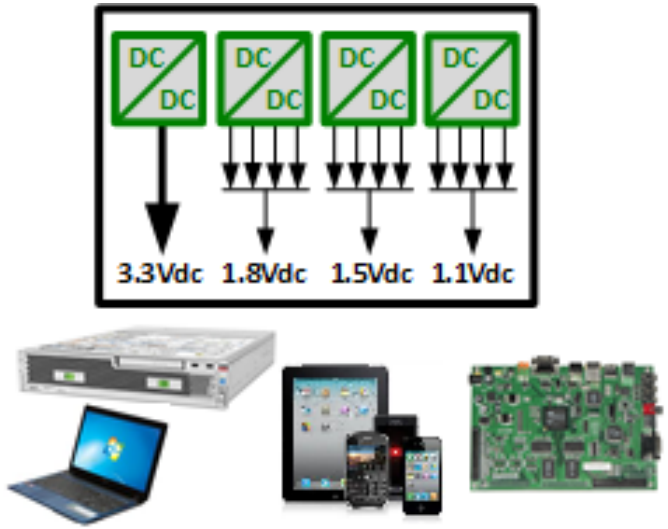
Power Electronics Designs are Used Everywhere

But today we will focus on the DC-DC Converter Digital Power Management application



Brief Definitions….

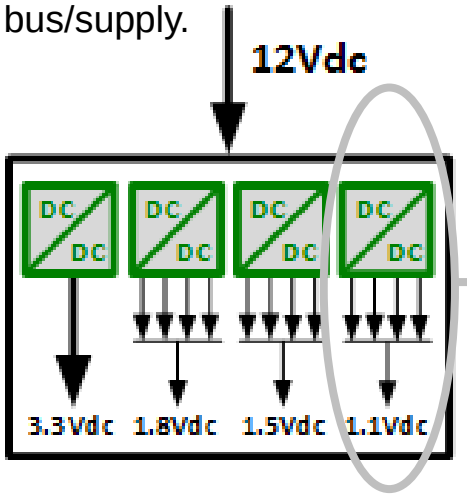
- **Digital Power Management**
  - The control of various DC-DC converter voltages to ensure appropriate and prompt delivery of current (power) over one or more DC power/voltage rails to various CPU, memory, or other devices in a motherboard or embedded computing system.
- **Power Integrity**
  - The analysis to determine whether expected voltage and current requirements are met from regulated DC output to the power consuming device.
- **Voltage/Power Rail Sequence Testing**
  - The control of the ramp times and sequence of the various DC power/voltage rails in a motherboard or embedded computing system.



Digital Power Management – The Basics

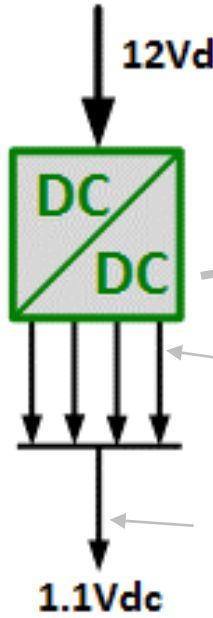
High Level Overview

Bulk power is supplied to an embedded computing system through a high voltage (e.g., 12Vdc) bus/supply.



An embedded computing system requires one or more different “rails” (e.g., 3.3, 1.8, 1.5, 1.1Vdc) to provide voltage and current to the CPU and other on-board devices.

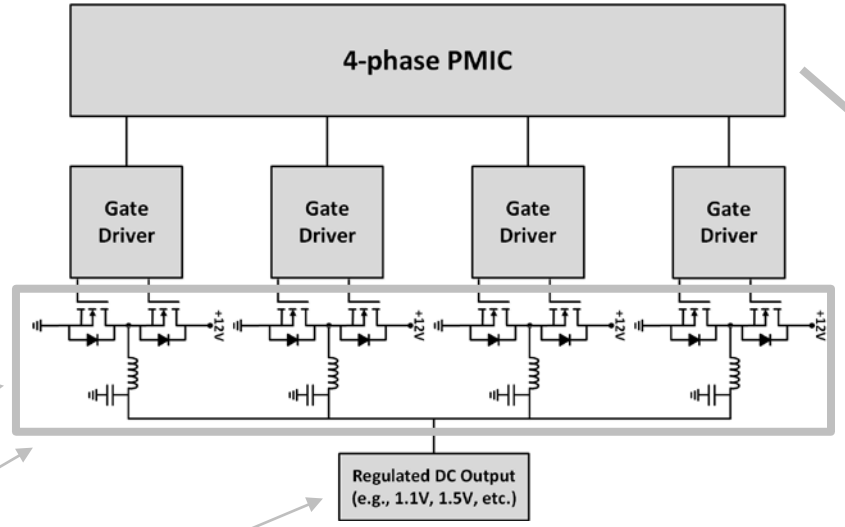
To provide high efficiency, each DC-DC converter power supply is actually several DC-DC converters in parallel.



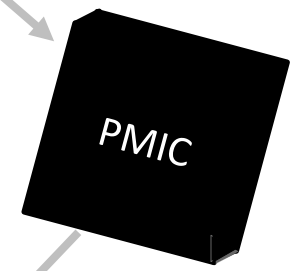
4 “phase” or “channel” outputs from one DC-DC converter

1 DC power / voltage rail

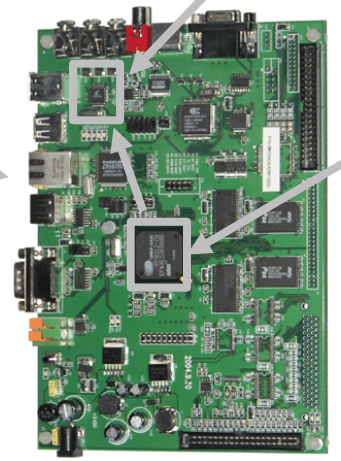
In this example, there are four parallel DC-DC converters (called “phases” or “channels”) that each supply 25% of the total output current to the 1.1Vdc rail.



A Power Management IC (PMIC) turns the phases on and off as load power requirements change, and time interleaves the PWM outputs into one output.



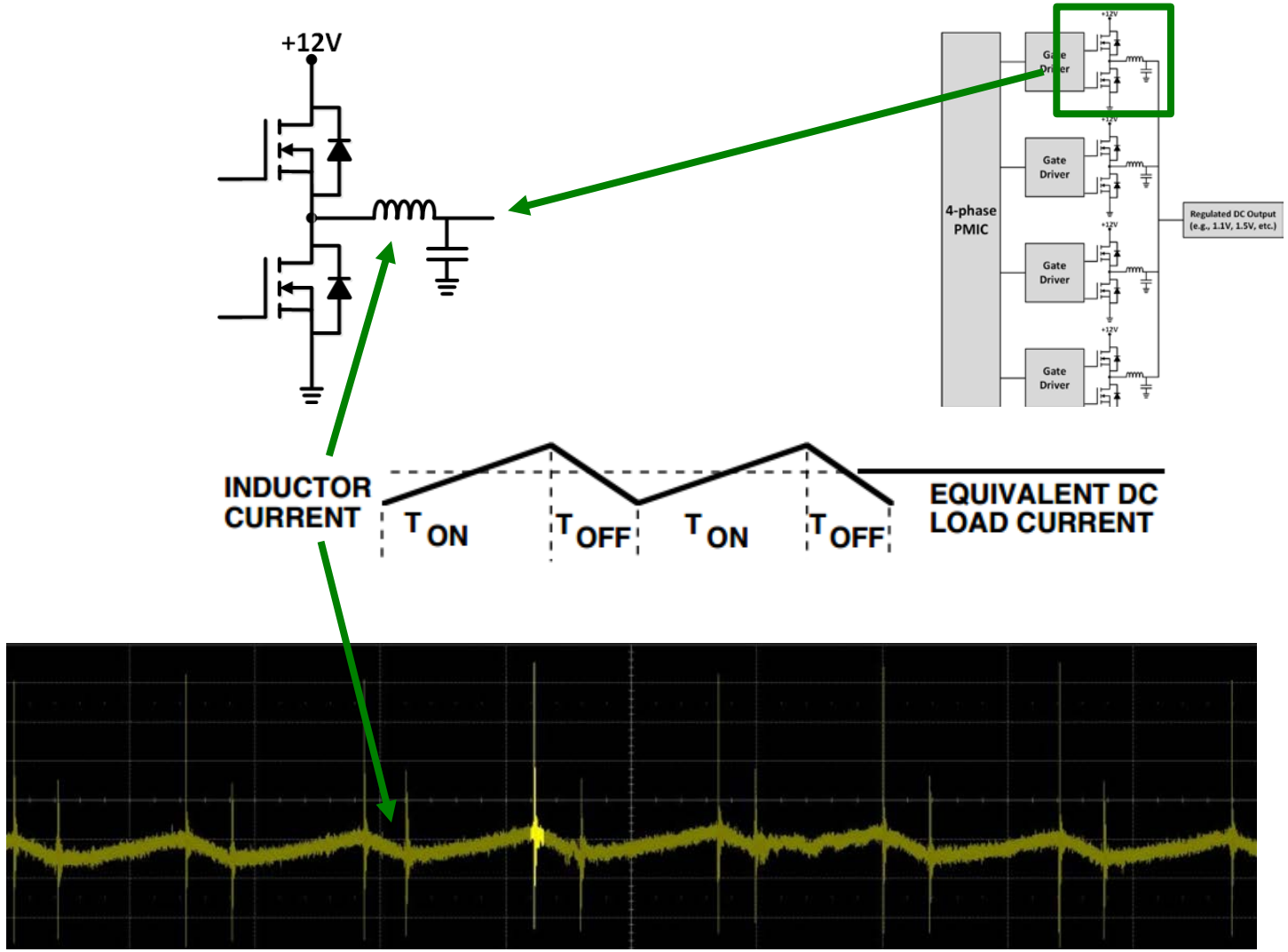
The PMIC and CPU are both located on a motherboard of some type. The motherboard may be part of a larger stand-alone embedded system, or it could be used in a server, laptop, tablet, mobile phone, gaming system, consumer device, etc.



The CPU issues serial data commands to the PMIC so as to ensure proper current supply to all devices

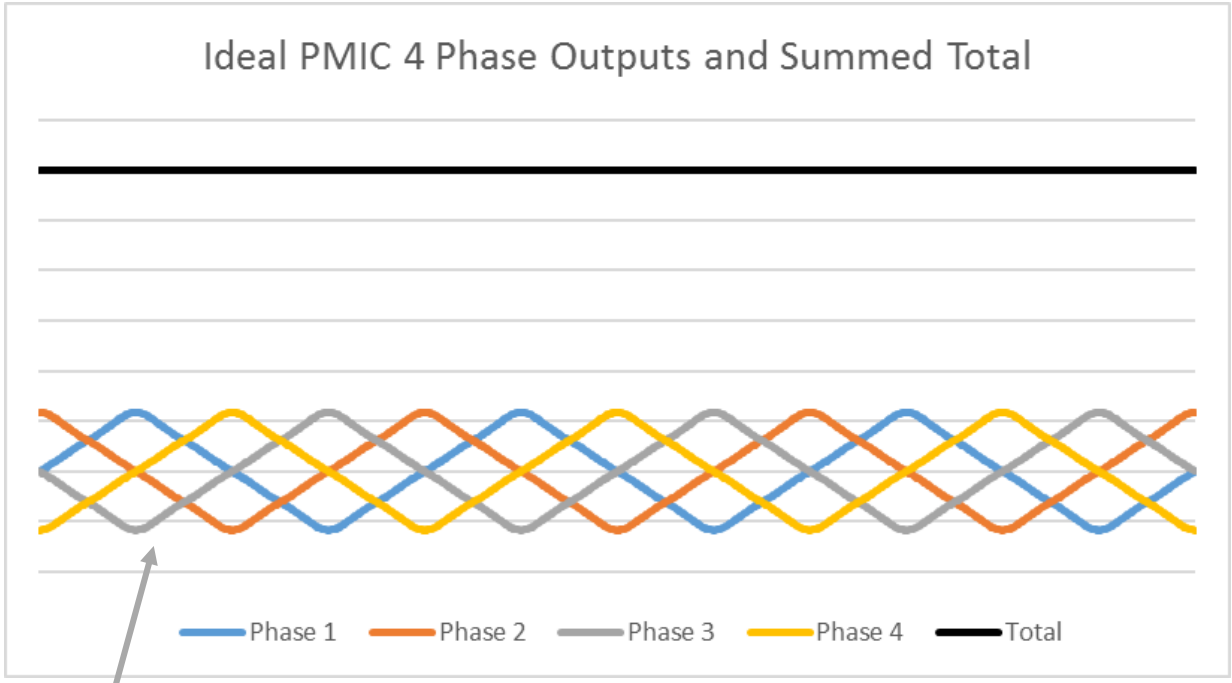
Digital Power Management and Power Integrity – The Basics

- The half-bridge output current is commonly called the “inductor current” because it flows through the output inductor (filter).
  - It increases (ramps up) when PWM signals are “ON” and ramps down when PWM signals are “OFF”
- Additional load capacitance will filter this further



Digital Power Management and Power Integrity – The Basics

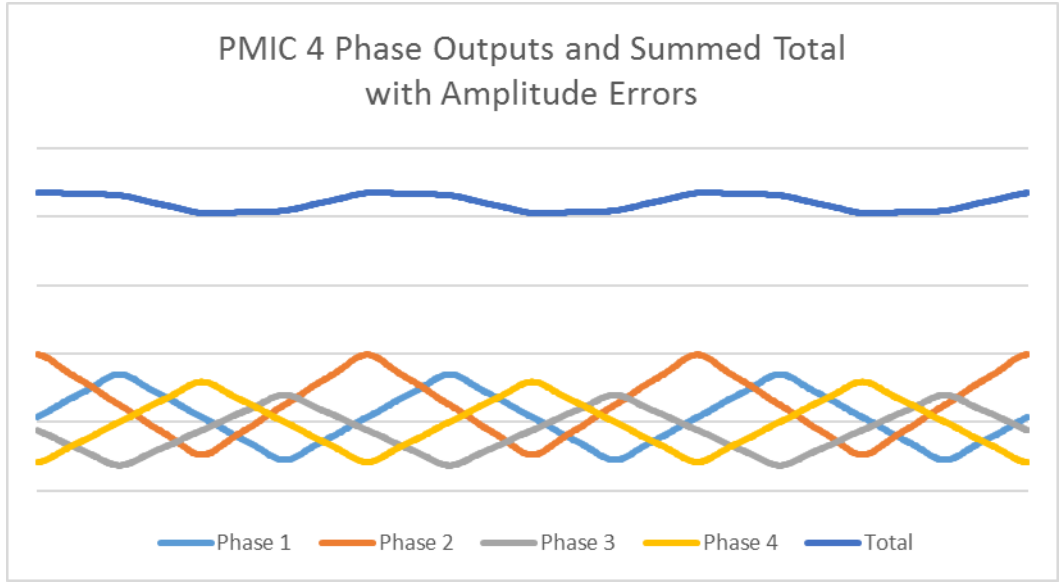
- Ideally, each PMIC phase under steady-state load condition is balanced
  - Same amplitude (voltage PWM)
  - Phase relationship to other phases of $(1/f_s)/N$
    - f_s is the power semiconductor device switching frequency
    - N is the number of phases



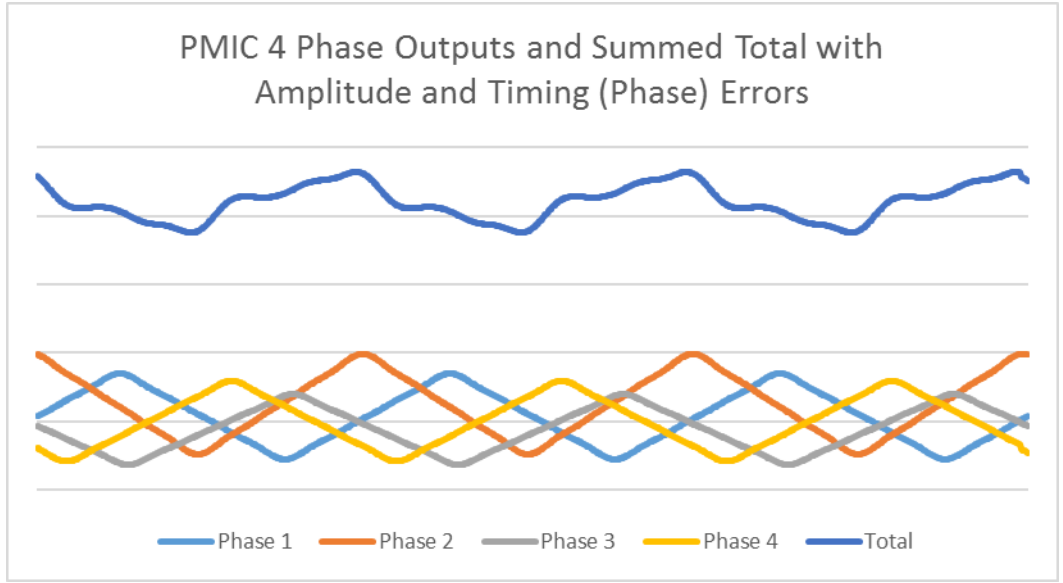
Example - these are the phase currents under steady-state operating conditions after filtering by the inductor

Digital Power Management and Power Integrity – The Basics

- If there are amplitude errors between the different phases, output ripple will result

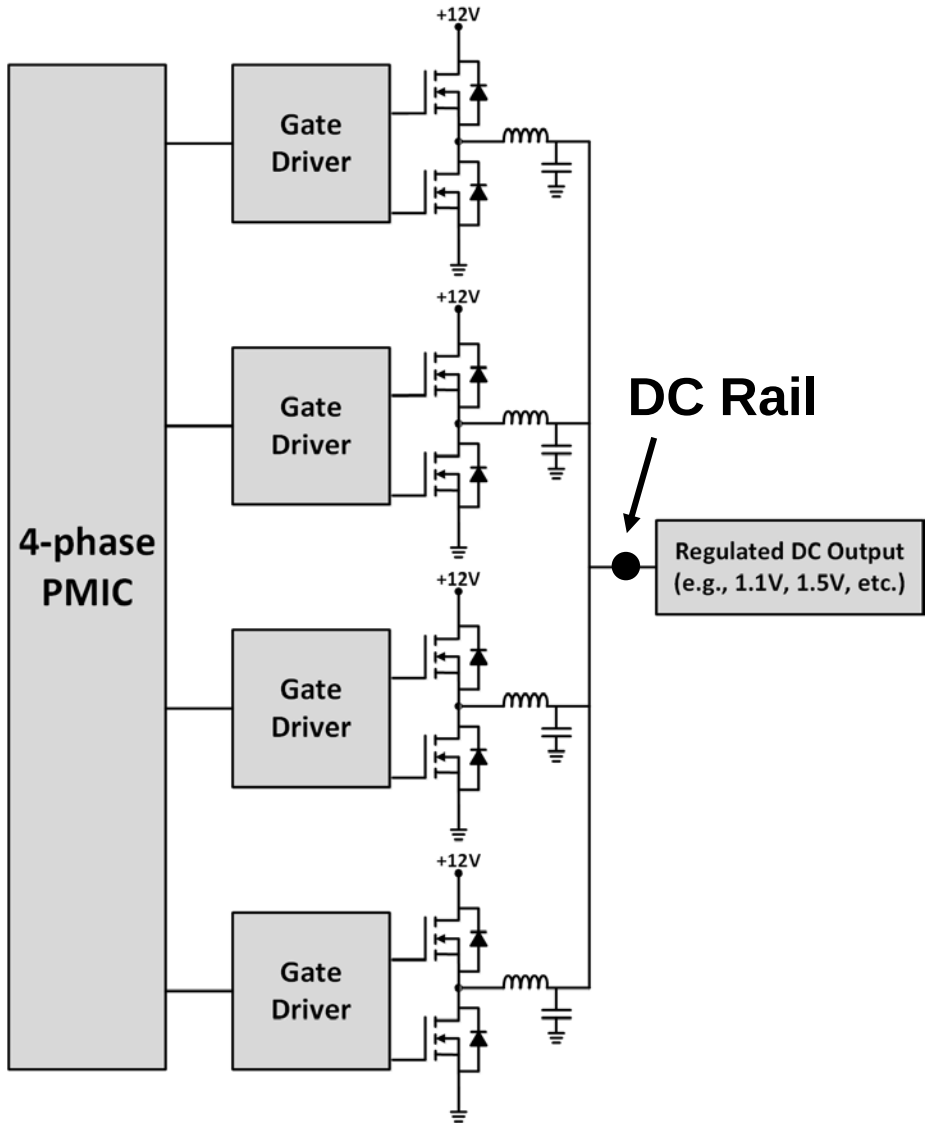


- If there are amplitude and phase errors between the different phases, more complicated distortion patterns will be introduced



Typical Digital Power Management and Power Integrity Tests
For One PMIC (One DC Power/Voltage Rail)

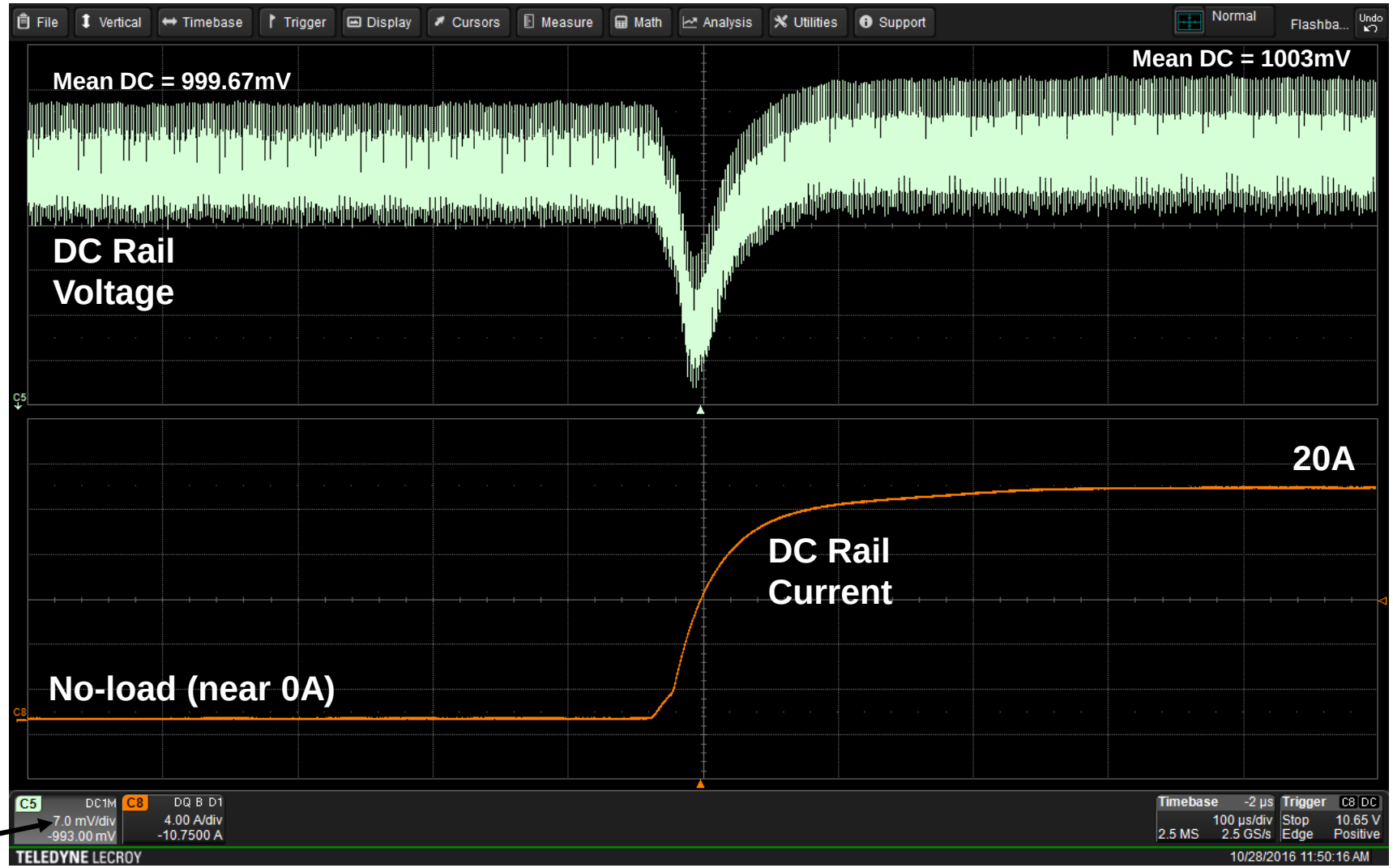
- PMIC Transient DC Rail Response
  - Addition or release (subtraction) of load
    - Dynamic test
    - Long capture time is very useful
    - Correlate activity to other signals
      - Serial data commands
      - Clocks / Strobes
      - Enable lines
  - Measure DC Rail voltage ripple
  - Measure DC Rail voltage ringing
  - Measure settling time to DC Rail voltage stability – ensure it is within tolerance at all times



PMIC Transient Rail Response Testing

Acquiring and Viewing the Transient Response of a Single DC Rail

- Load increased from ~0 to 20A
- DC Rail voltage is monitored
  - Ripple
    - e.g. +/-20mVp-p
  - Overshoot
  - Droop
  - Noise
  - Settling time
  - etc.



7 mV/div gain setting with 1Vdc offset

PMIC Transient Rail Response Testing, cont'd

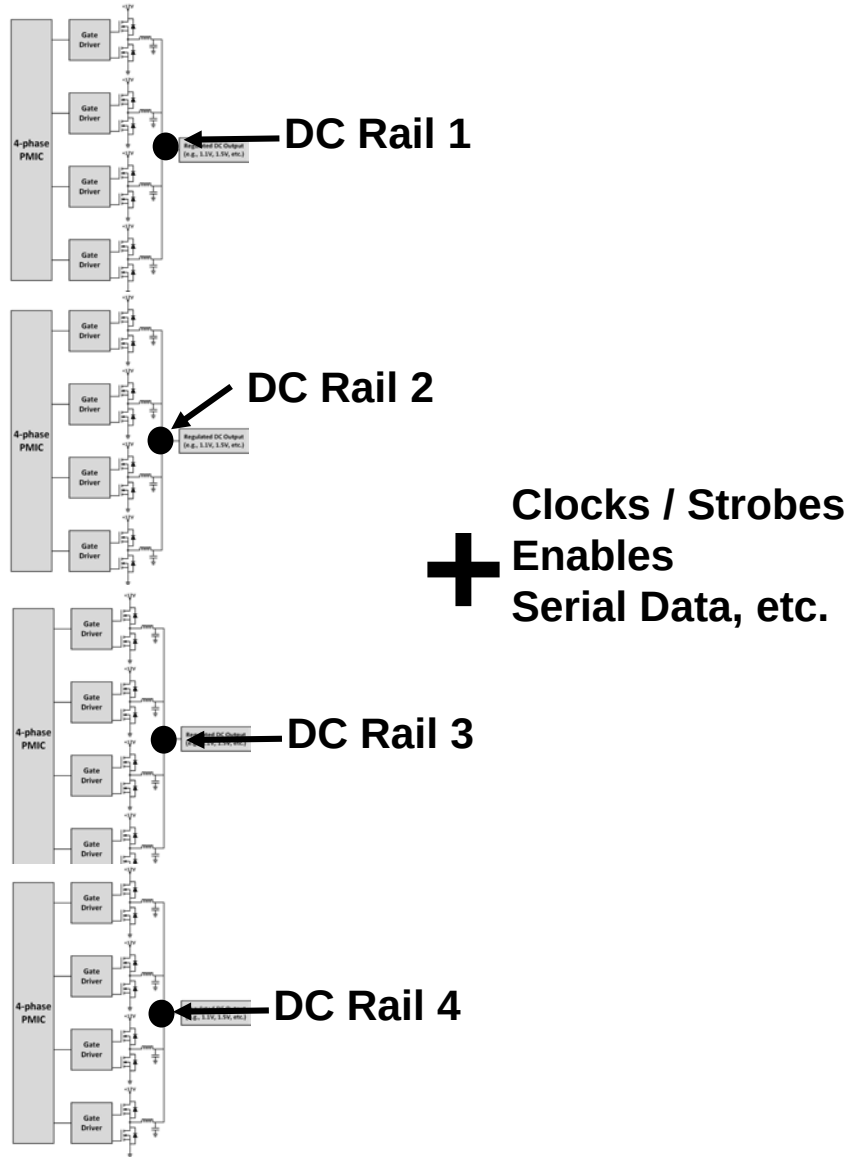
Measuring the Transient Response of a Single DC Rail

- Measurement Parameters with Gates can be used to measure Vdc_{RAIL} before and after load.
  - 999.67 mV before
  - 1003.00 mV after
- Zooms and measurement parameters can be used to understand high-frequency behaviors
  - Z1 = V_{MIN} at step (967.70 mV)
  - Z5 = V_{MAX} before step (1012.21 mV)
  - Z7 = V_{MAX} after step (1016.38 mV)
- Measure Parameter can be used to measure step load change
  - 20.436 A

PMIC Transient Rail Response Testing, cont'd

Multiple PMICs and Multiple DC Rails

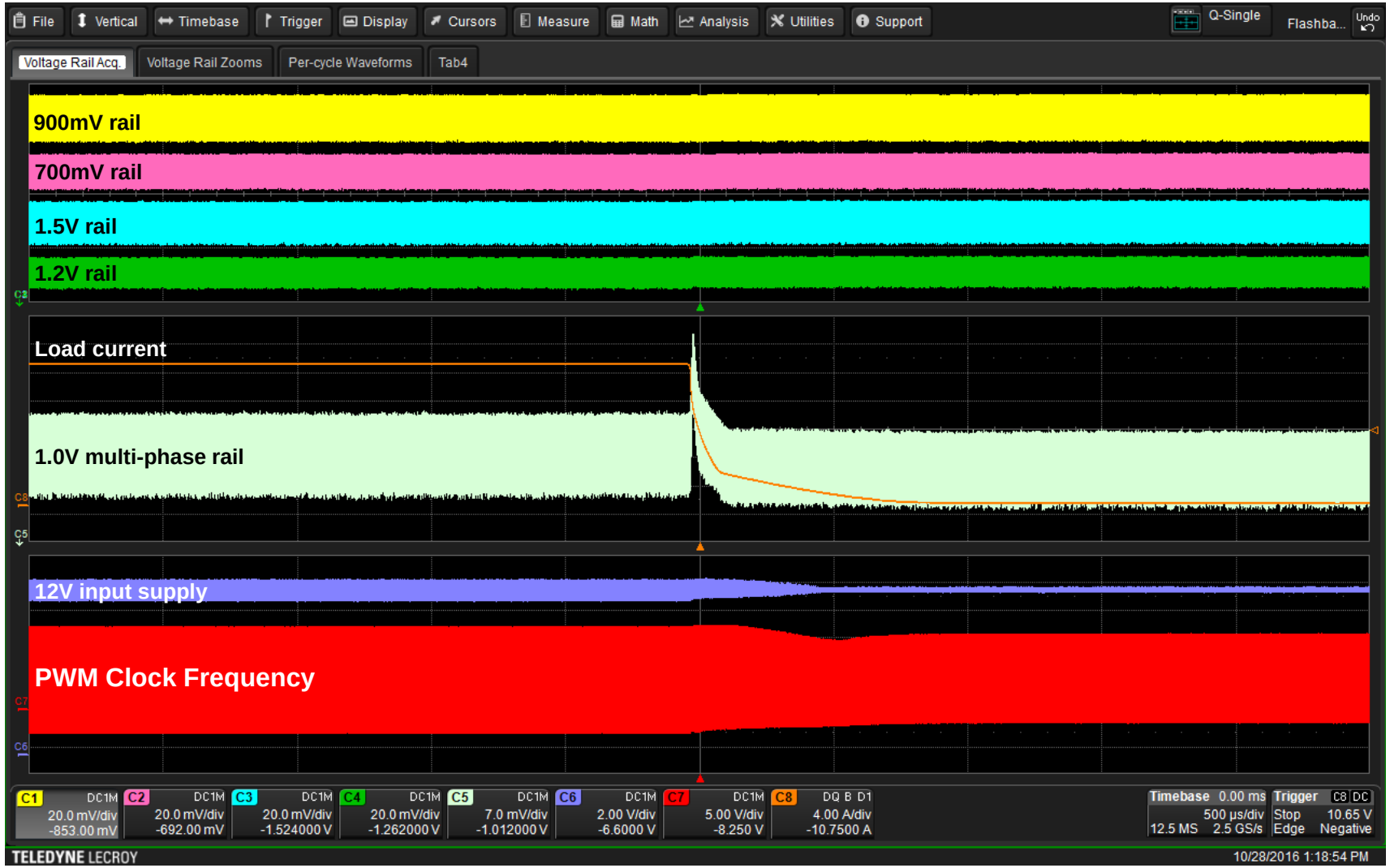
- Same Tests as Single Rail Case
- Objective is to Understand Impacts of Load Changes on All Rails at One Time



PMIC Transient Rail Response Testing, cont'd

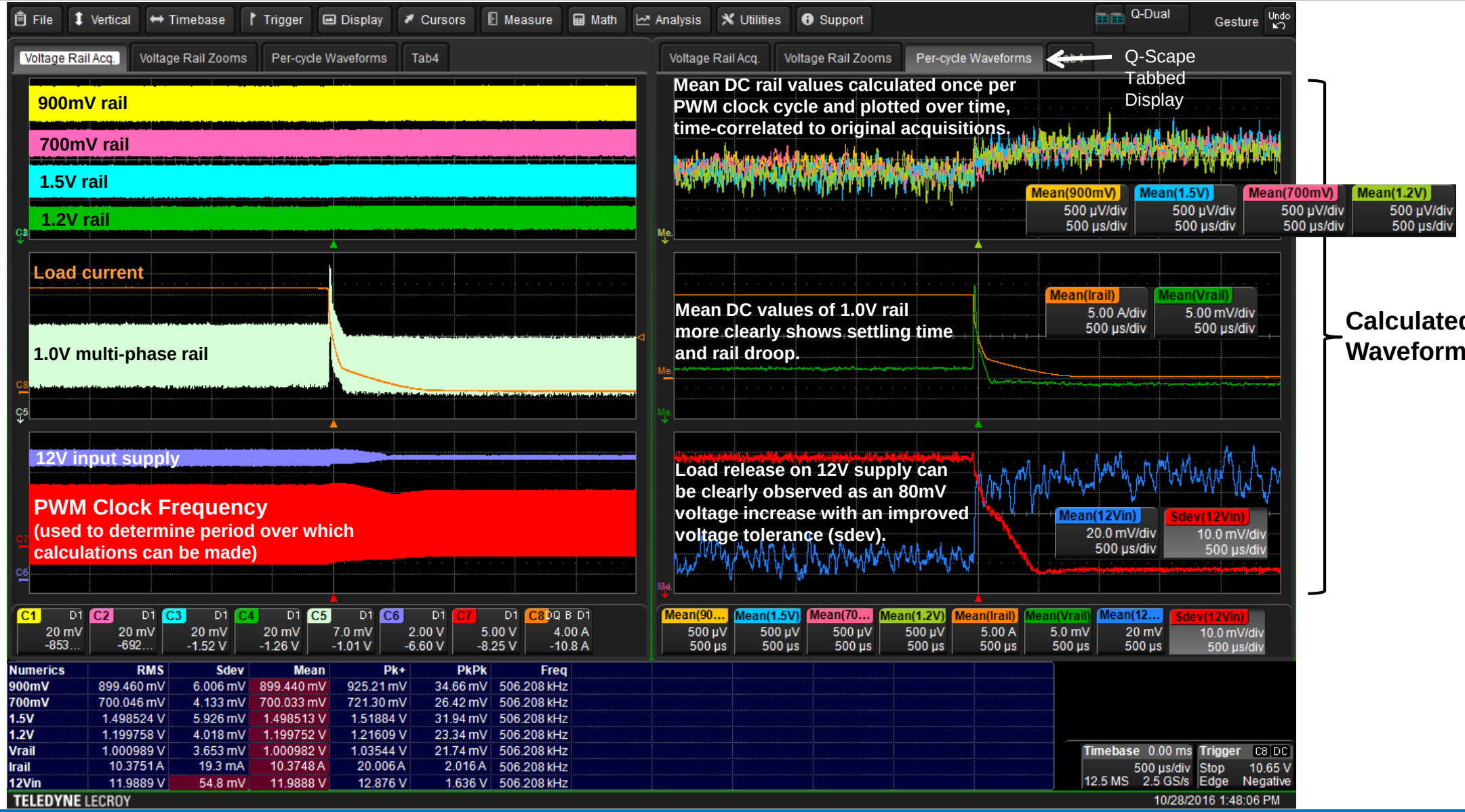
Understanding the Transient Response of a Load Release on Multiple Rails

- Monitored input signals included
  - Simple DC Rails
    - 700mV
    - 900mV
    - 1.2V
    - 1.5V
  - Multi-phase DC Rail (1.0V)
  - 12V supply Rail
  - Load Current (20A to 0A)
  - PWM Clock



PMIC Transient Rail Response Testing, cont'd

Digital Power Management (DigPwrMgmt) Application Package Provides More Information



Numerics	RMS	Sdev	Mean	Pk+	PkPk	Freq
900mV	899.460 mV	6.006 mV	899.440 mV	925.21 mV	34.66 mV	506.208 kHz
700mV	700.046 mV	4.133 mV	700.033 mV	721.30 mV	26.42 mV	506.208 kHz
1.5V	1.498524 V	5.926 mV	1.498513 V	1.51884 V	31.94 mV	506.208 kHz
1.2V	1.199758 V	4.018 mV	1.199752 V	1.21609 V	23.34 mV	506.208 kHz
Vrail	1.000989 V	3.653 mV	1.000982 V	1.03544 V	21.74 mV	506.208 kHz
Irail	10.3751 A	19.3 mA	10.3748 A	20.006 A	2.016 A	506.208 kHz
12Vin	11.9889 V	54.8 mV	11.9888 V	12.876 V	1.636 V	506.208 kHz

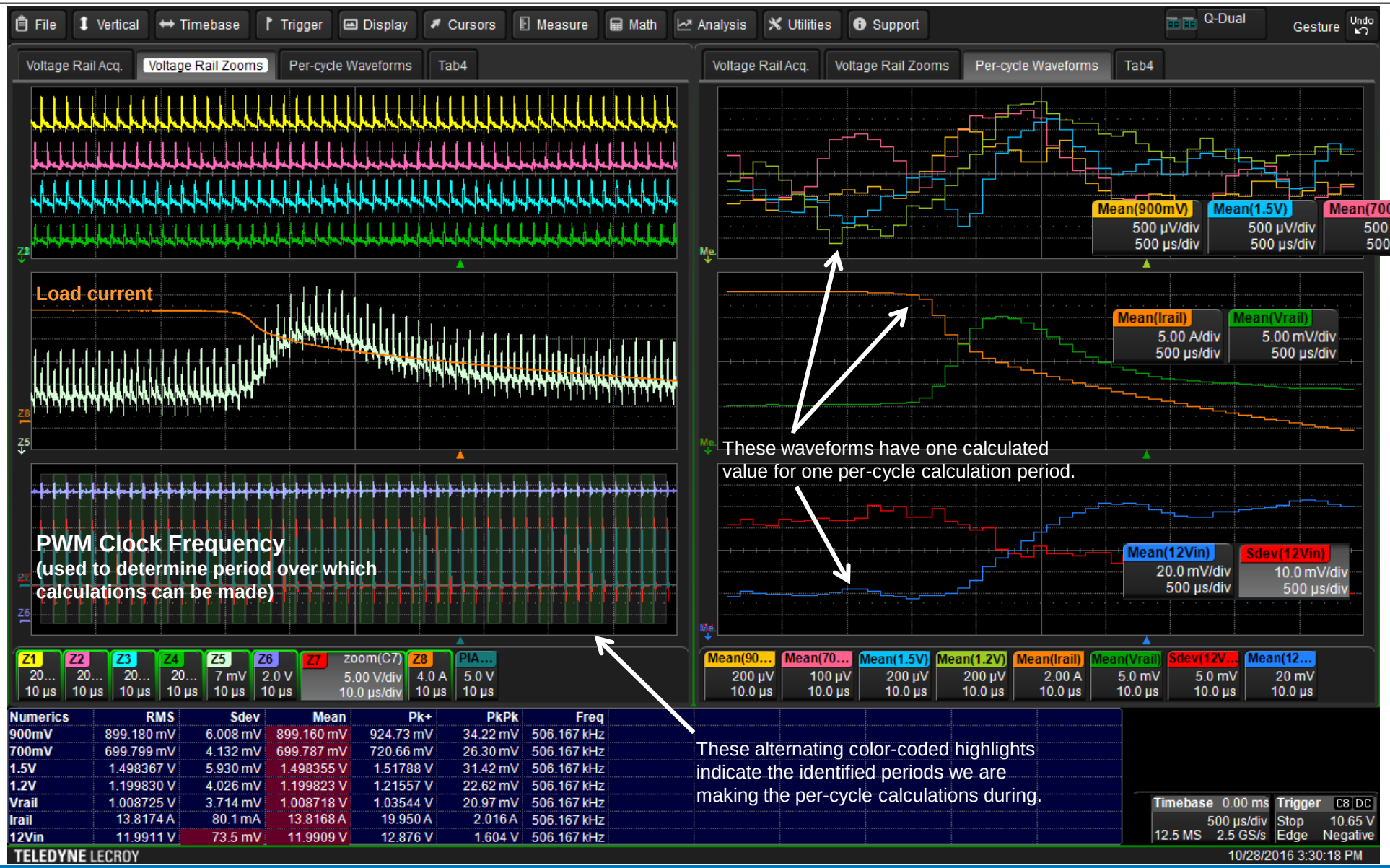
Acquired Waveforms

Calculated Waveforms

Mean Value Numerics Table

PMIC Transient Rail Response Testing, cont'd

Zooms provide capability to understand details of system response



50x Zooms of Acquired Waveforms

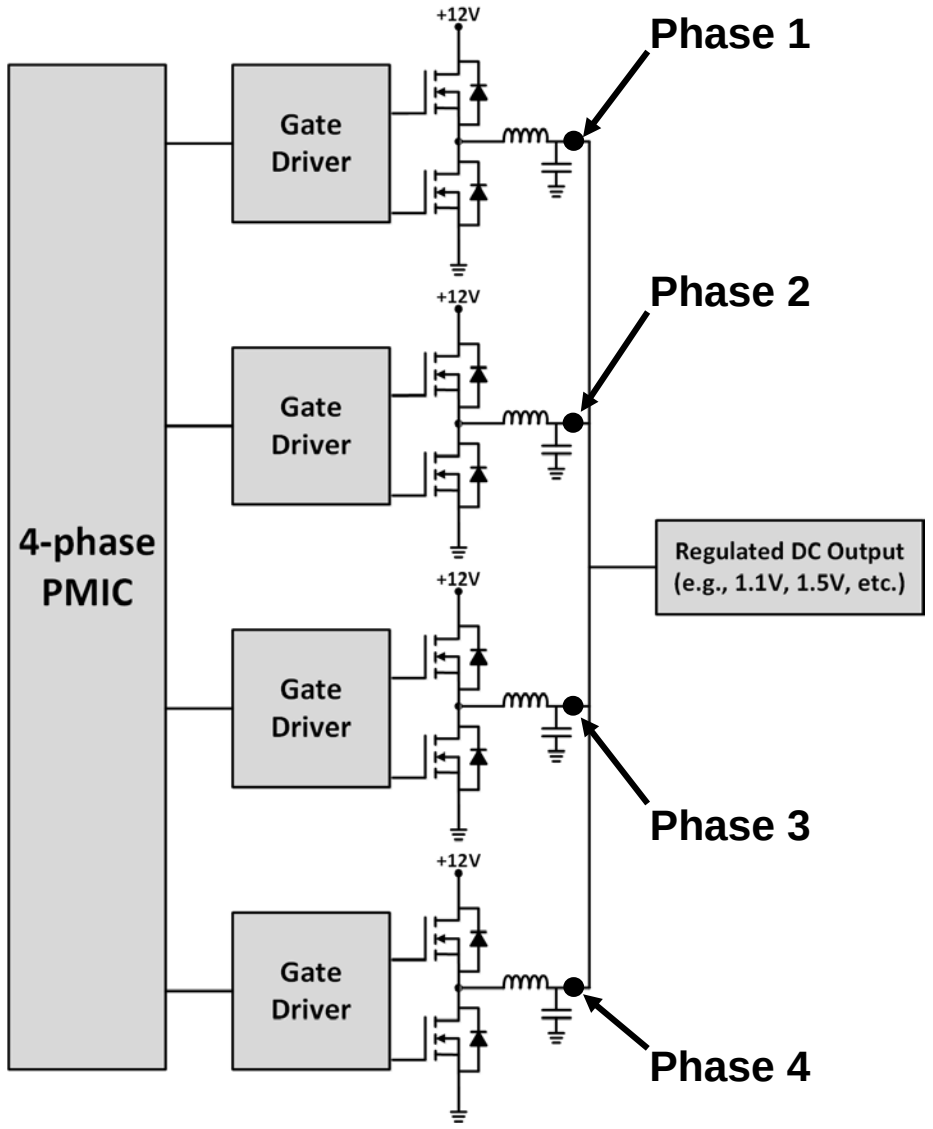
50x Zooms of Calc'd Waveforms

Mean Value Numerics Table

PMIC Transient Rail Response Testing, cont'd

For Multiple Phases in One PMIC

- PMIC Load/Current Sharing/Tracking
  - Measure voltage/current on each individual phase output
  - Difficult to do – PMIC normally does not make output accessible for measuring current
- Pete Pupalaikis will be presenting on this topic at the end of this session



Teledyne LeCroy High Definition Oscilloscopes (HDO)

For acquisition and analysis of DC power/voltage rails and currents

- HDO8108
  - 8ch, **12-bit**, 1 GHz
  - MSO option
  - Up to 250 Mpts/Ch
  - Power Management, Power Sequence, Power Integrity

- HDO9404
  - 4ch, **10-bit**, 4 GHz
  - MSO model
  - Power Integrity

Voltage/Power Rail Sequence Testing

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February 1, 2017

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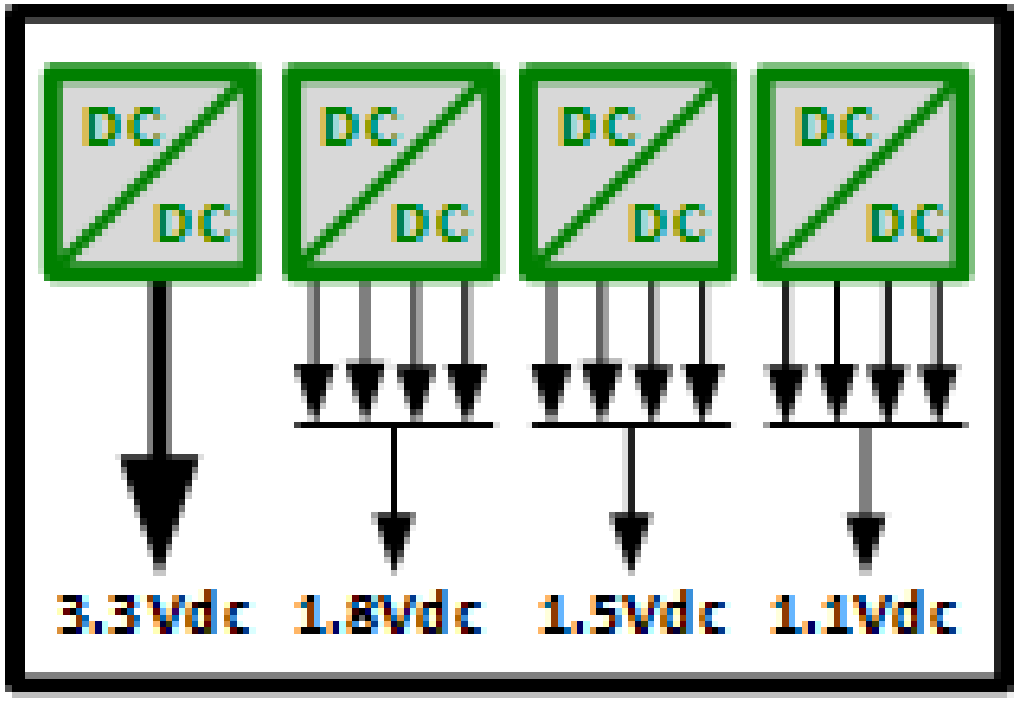
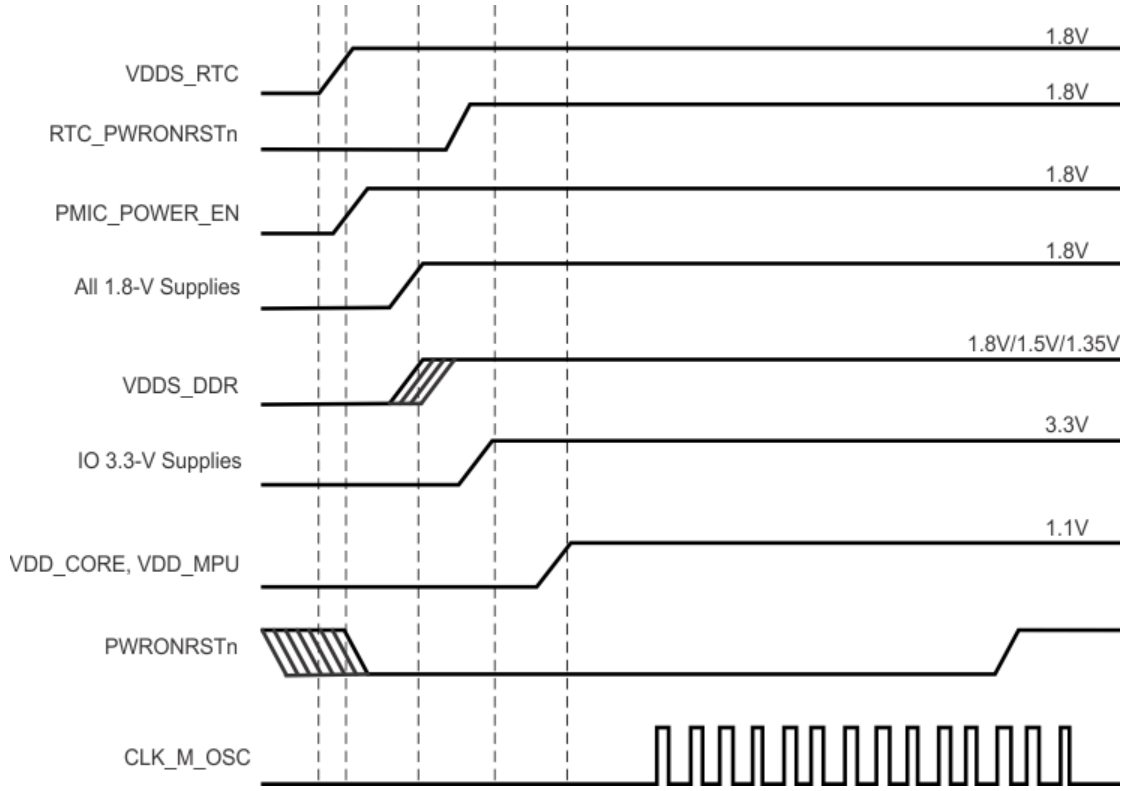
What is Sequence Testing?

- For the computing system to “boot-up” correctly, the DC rails must turn ON in a specific order with specific “wait times” between each turn ON.
- For example,
  - First 3.3Vdc goes high
  - Then, 200-500ms later, 1.8Vdc goes high
  - Then 200-500ms later, 1.5Vdc goes high
  - Lastly, 500ms-800ms later, 1.1Vdc goes high



What are Sequencing Tests?

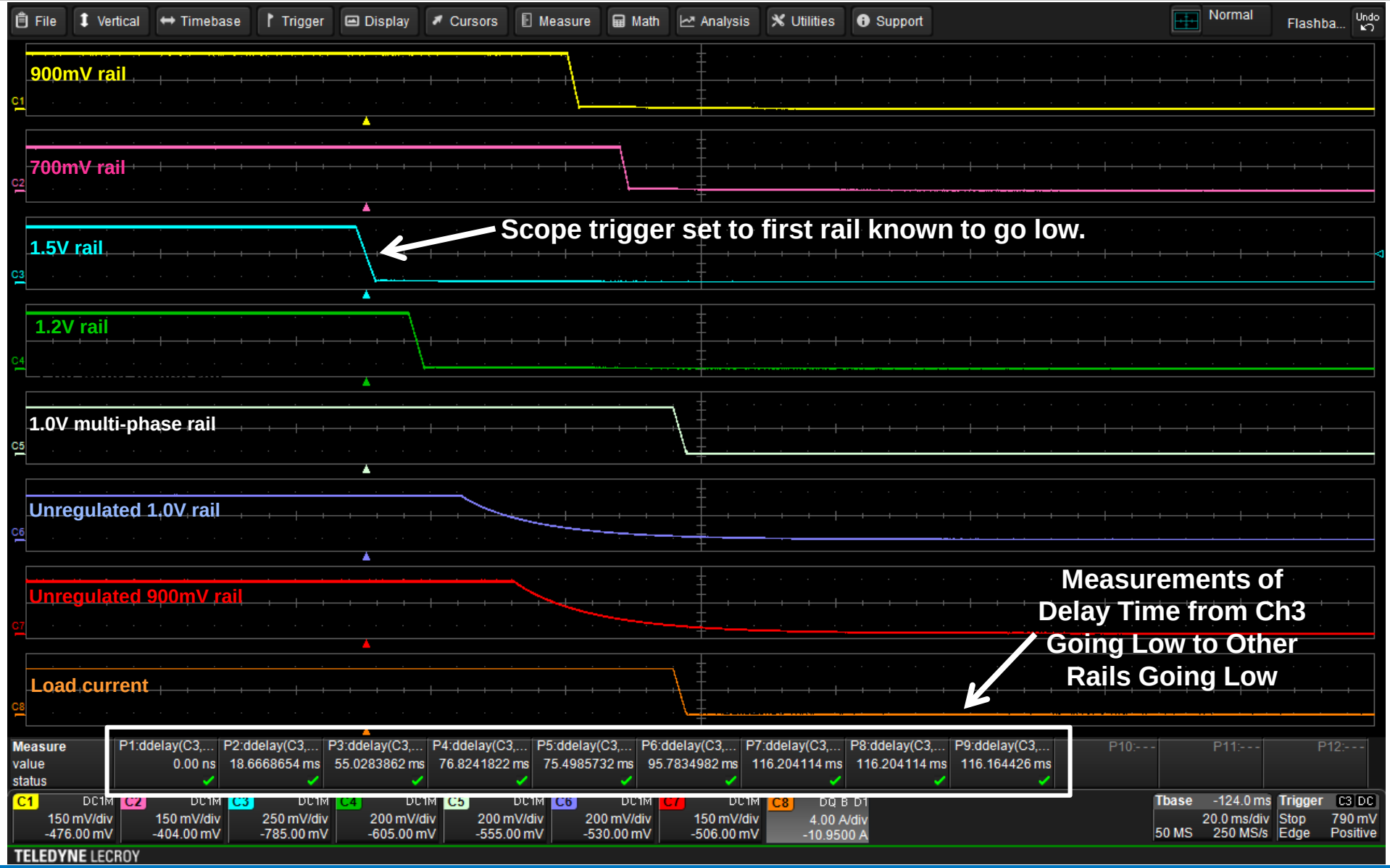
- Acquire as many DC rail signals as possible
  - More is better – great 8ch application
- Acquire other signals,e.g.:
  - Clocks
  - PMIC enable
  - Strobes
  - Serial data command signals to PMIC
- Measure timing between signals
  - Usually with cursors
  - Serial TDME options could be useful to some customers
- Long capture times with high SR are common
  - 250 Mpts of memory is very useful
  - Capture a lot of time at high sample rate in many different start-up scenarios, and zoom for details



- The image above is a start-up sequencing requirement (timing details are omitted) for a TI embedded ARM microprocessor (http://www.ti.com.cn/product/cn/AM3358-EP/datasheet/6_ZHCSE24A
- Note the many different rail voltages (5 different) and multiple 1.8Vdc rails – this is very common
  - Important reason why 8ch is very, very useful

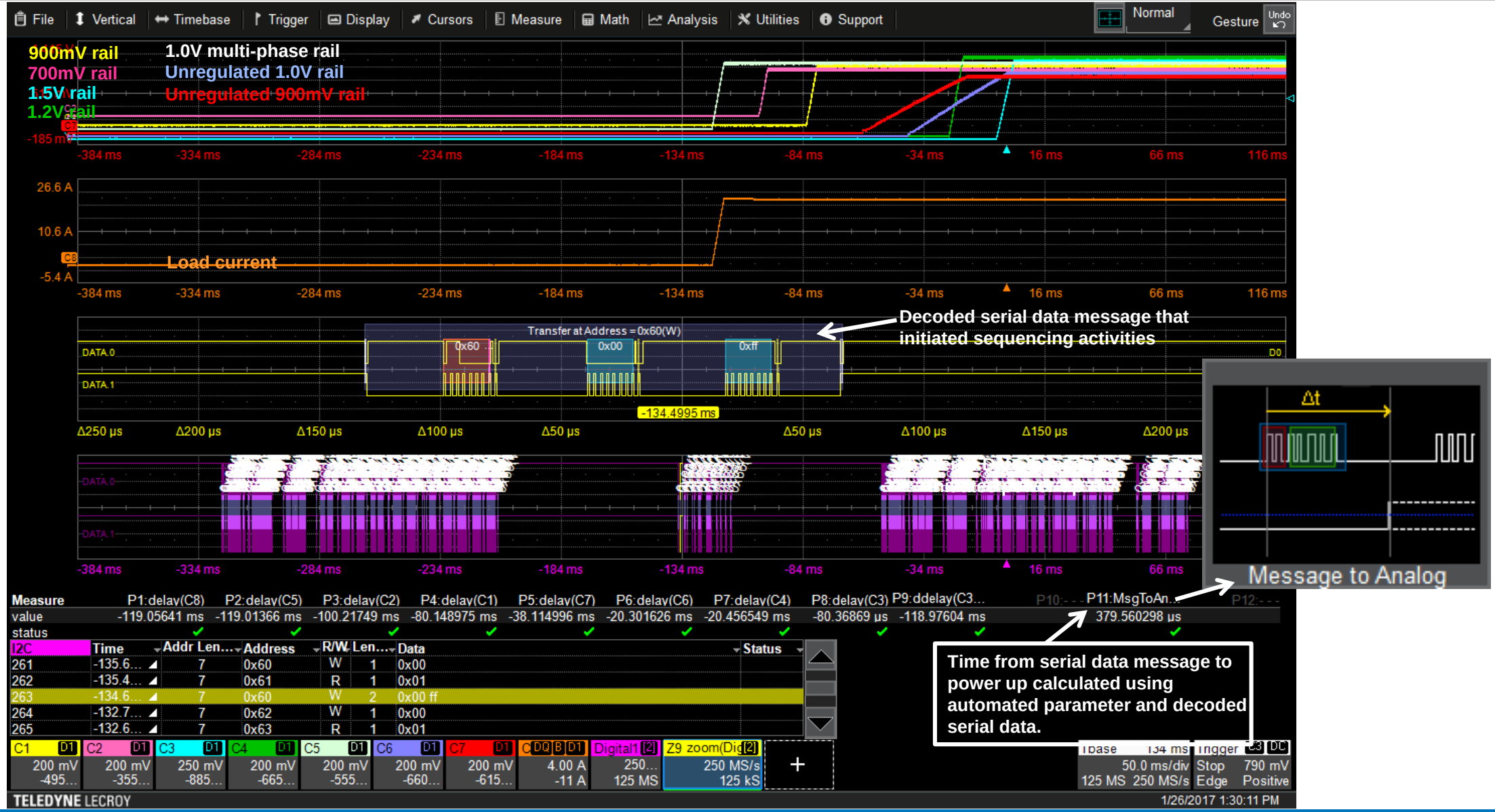
Power/Voltage Rail Sequence Testing on Power Down

50 Mpt capture at 250 MS/s (200 ms) – using timing parameters to measure delta times



Power/Voltage Rail Sequence Testing – Using Serial Data Toolsets

Trigger on a Serial Data Message, Decode It, and Make Automated Timing Measurements

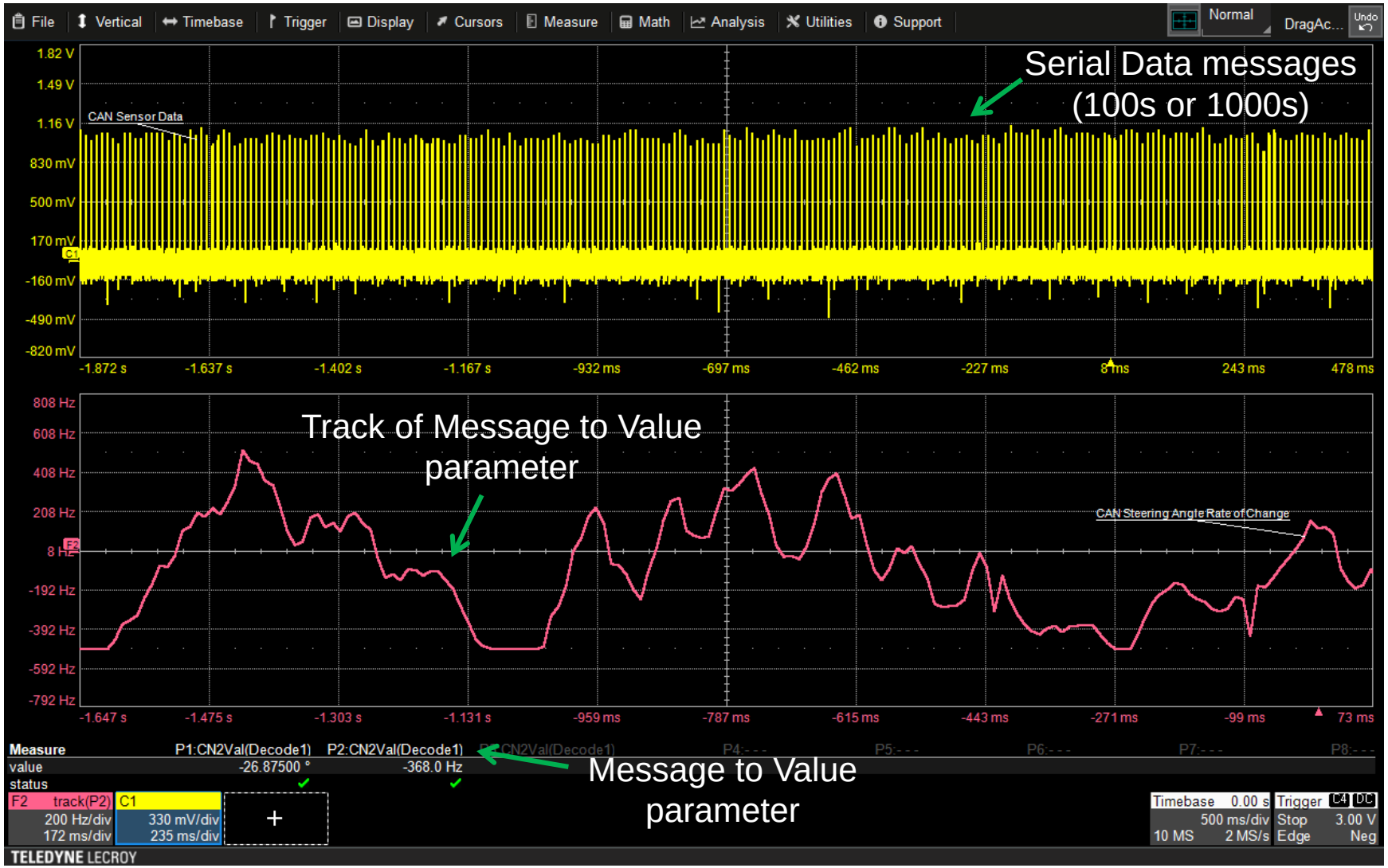


Serial Data Toolsets – Measurements and Graphing

- Timing Measurements
  - Message to Analog
  - Analog to Message
  - Message to Message
- Message to Value
  - “Serial DAC”
- Automatic
  - Run corner cases, gather statistics
  - Display histograms
  - Correlate cause-effect timing relationships to other events

“Serial Data DAC” Graphing of Digitally Decoded Data

- Message to Value parameter
- View serial data change over time
- Examples
  - PMbus voltage
  - I²C or SPI temperature
  - CAN wheel speed (ABS)
  - I²S audio



SPMI (System Power Management Interface) Decoder

- SPMI
  - MIPI standard
- More than 20+ other complete solutions
  - I2C (PMbus)
  - UART-RS232
  - SPI
  - USB2
  - HSIC
  - etc.

Acquiring DC Power/Voltage Rails and Current Signals

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Acquiring DC Power/Voltage Rails

There are three primary methods

- 50Ω Coaxial Cable Terminated at Oscilloscope Input with DC 1MΩ Coupling
  - 1x attenuation (low noise), but…
  - Requires high native offset capability in the oscilloscope equal to the DC rail voltage
    - This is rare at high sensitivities (e.g., 5 mV/div), though Teledyne LeCroy HDOs provide this capability
  - Or Requires use of a DC block
    - DC blocks do not have response to DC – they always block some low frequencies
  - There will be reflections due to impedance mismatch
  - 1MΩ bandwidth <1 GHz

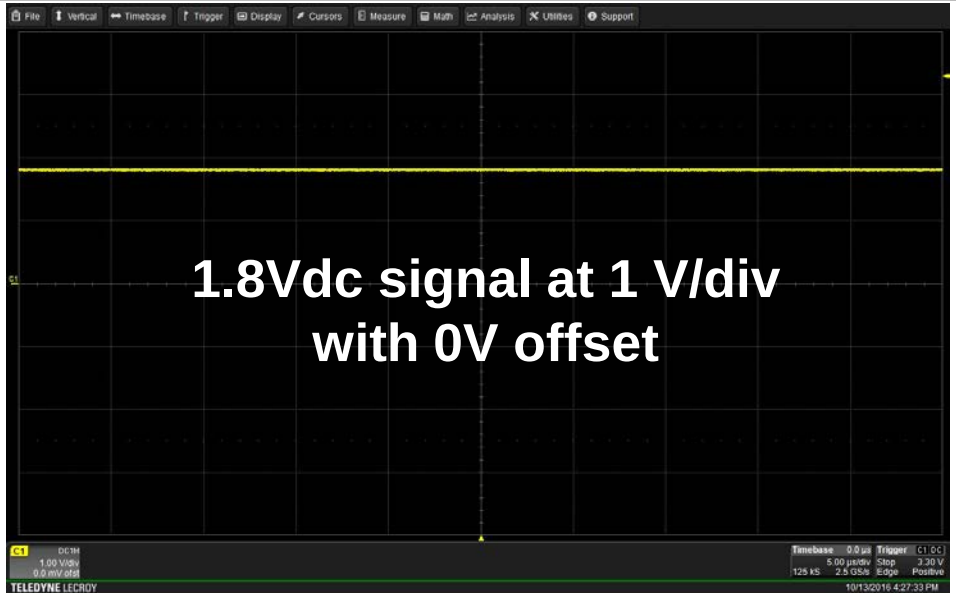
- Use of Specialized DC Power/Voltage Rail Probe
  - Ideal solution – low attenuation, high bandwidth, low circuit loading
  - Most expensive solution

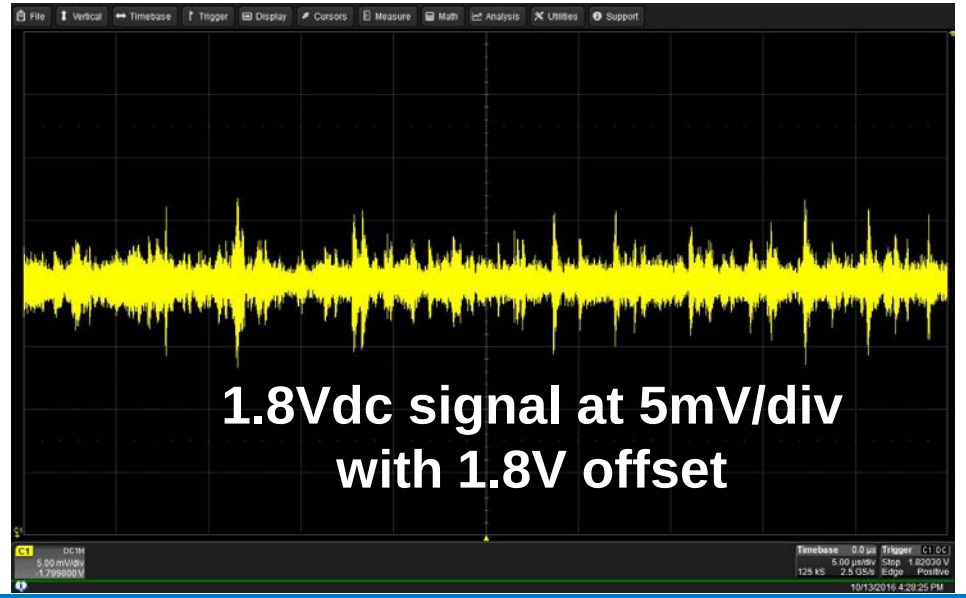
Acquiring DC Power/Voltage Rails

Teledyne LeCroy HDOs have large offset capability built-in to the oscilloscope input

- HDO native offset capability is very large
  - +/-1.6V (1mV to 4.95mV/div)
  - +/-4.0V (5mV to 9.9mV/div)
  - +/-8.0V (10mV to 19.8mV/div)
  - +/-10.0V (20mV to 1V/div)
  - This is the most of any oscilloscope on the market

- This makes it more practical to use a home-made coaxial cable probing solution
  - ***IF*** the limitations of this approach are acceptable

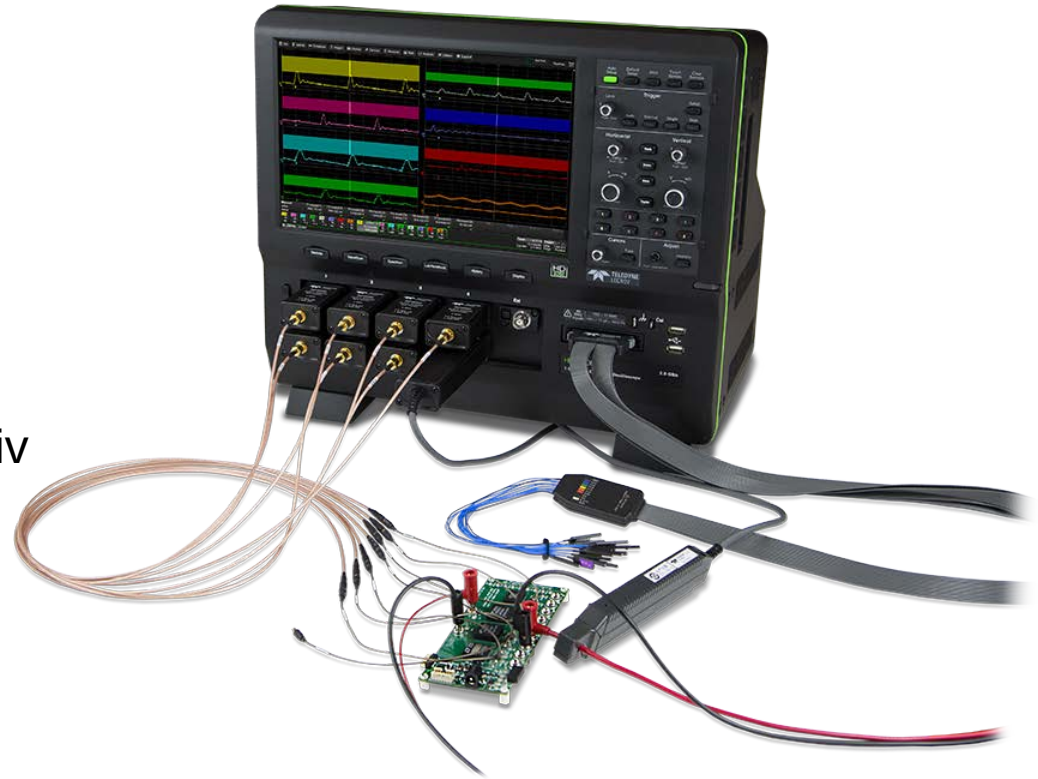




Acquiring DC Power/Voltage Rails

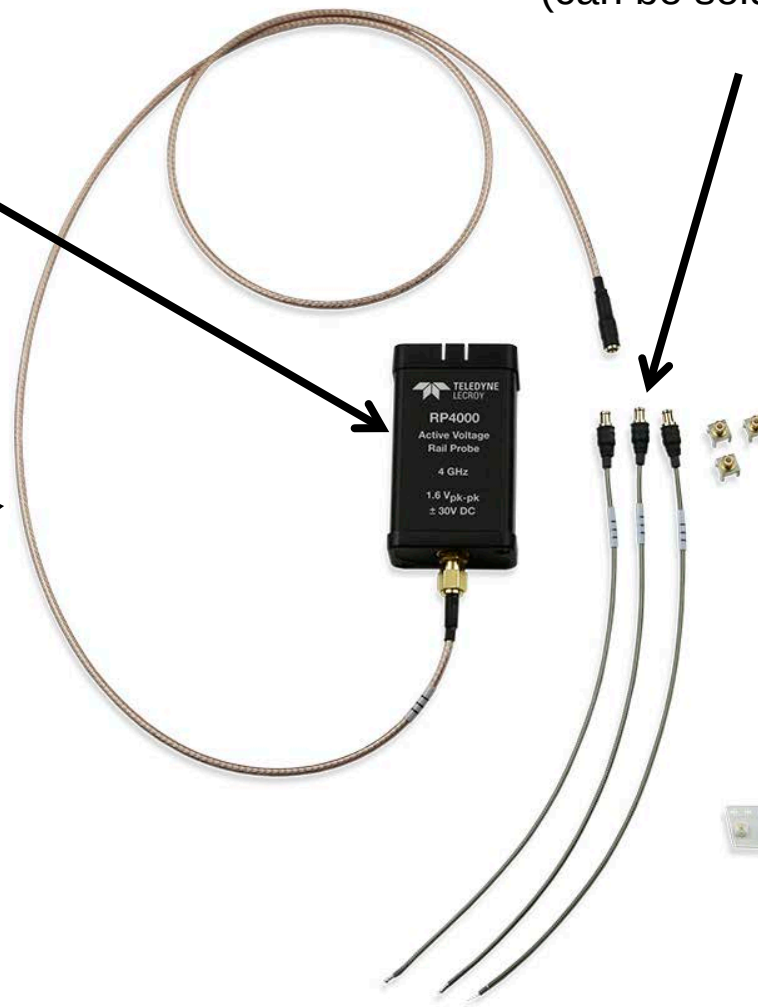
Using an HDO Oscilloscope and the RP4030 Power/Voltage Rail Probe

- The RP4030 Rail Probe is the ideal solution:
  - 4 GHz of Bandwidth
    - 4 GHz MCX Solder-in
    - 3 GHz U.FL Coax Cable with PCB Mount
    - 350 MHz Browser tip
  - 50 kΩ Input Impedance
    - Very low circuit loading on the DC rail
  - 1.2x Attenuation
    - Keeps scope+probe noise performance very low
    - ~165 µVrms with HDO4096 at 1 GHz and 1 mV/div
  - +/-30V Offset (+/-0.5% Accuracy)
    - Center a DC signal and use high-sensitivity gain setting (e.g., 2-20 mV/div)
  - +/-800 mV Dynamic/Differential Range
  - Can also be re-purposed for power rail sequence testing
    - Use an SMA to BNC adapter and attach directly to BNC input with 1 MΩ coupling



RP4030 Power/Voltage Rail Probe

Wide Variety of Tips and Leads for DUT Connection



MCX Solder-in Lead
(can be soldered-in and left in circuit)

ProBus-compatible amplifier

MCX PCB Mounts
(good for larger circuit boards – attach and leave in place for quick and easy connection to cable)

MCX to SMA Adapter

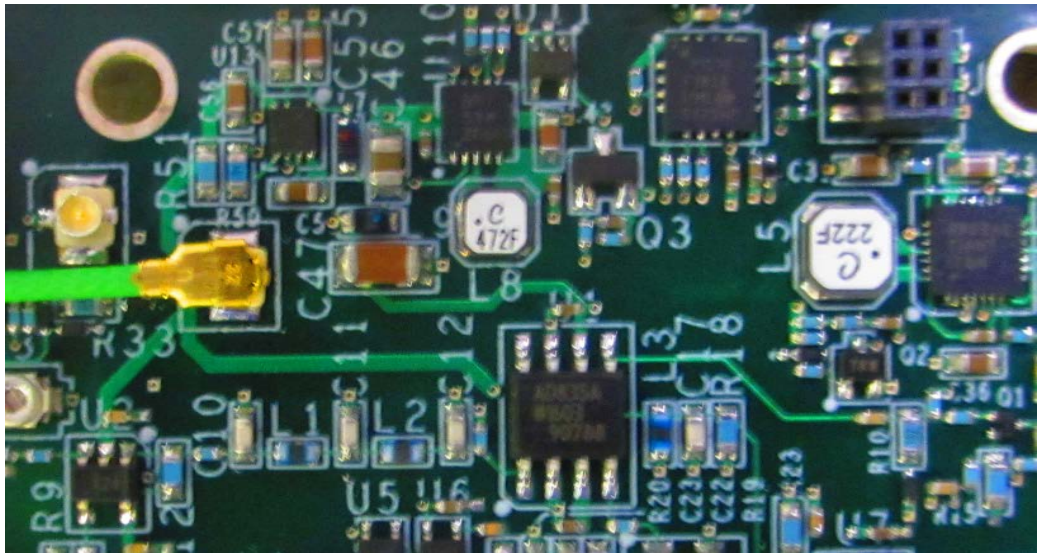
SMA to MCX short cable

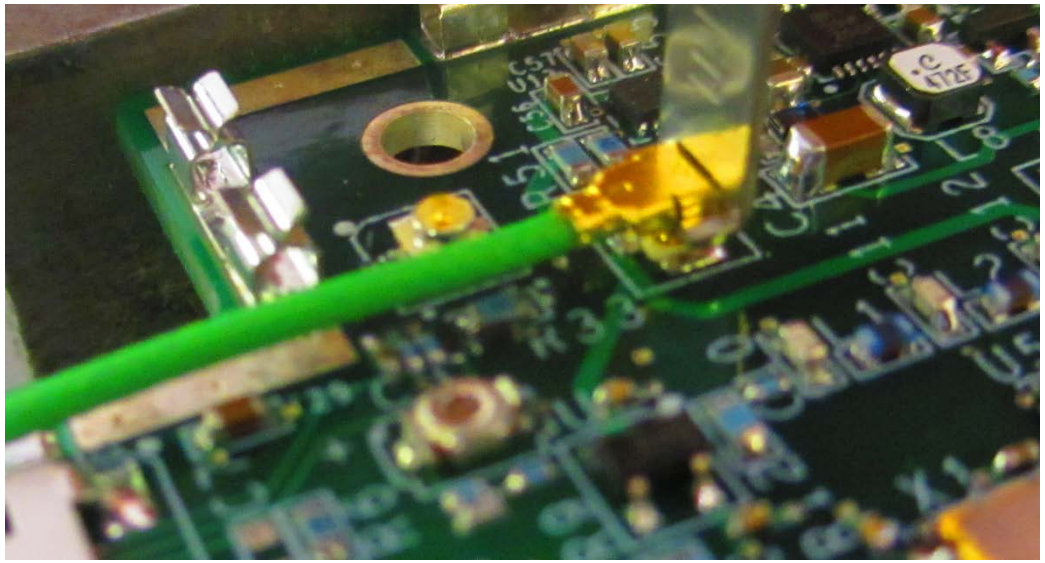
MCX to U.FL Lead
(attaches to compact UFL PCB Mounts).

U.FL PCB Mounts
(compact size for dense, mobile or handheld systems)

RP4030 U.FL Solution for Compact PCBs

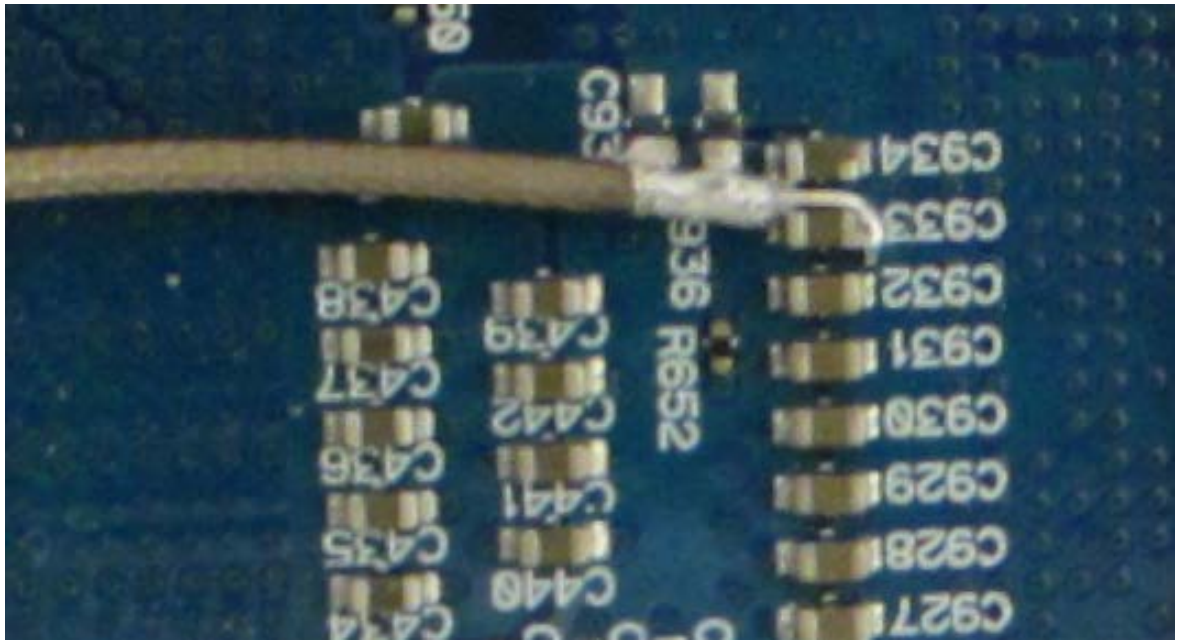
- Hirose U.FL ultra-miniature PCB mounts can be designed in to make probing easy
  - 3mm x 3mm
  - Functionally equivalent to PX and UMCC connectors
  - 3 GHz
  - Low cost
- Removal is simple with a widely available special-purpose extraction tool





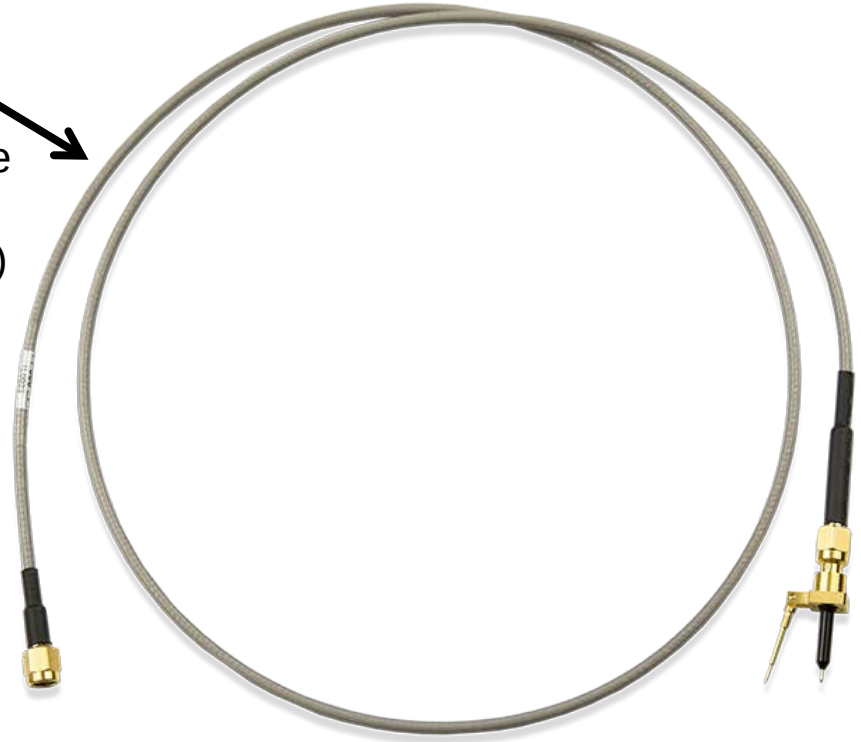
RP4030 Solder-in Lead

- Solder-in Lead Provides Optimum Performance
  - 4 GHz
  - Reasonable cost
- Multiple Leads Can be Soldered-in and Left in Place



RP4030 Optional Browser

SMA to SMA Cable
(for connecting to the RP4030 ProBus compatible amplifier)



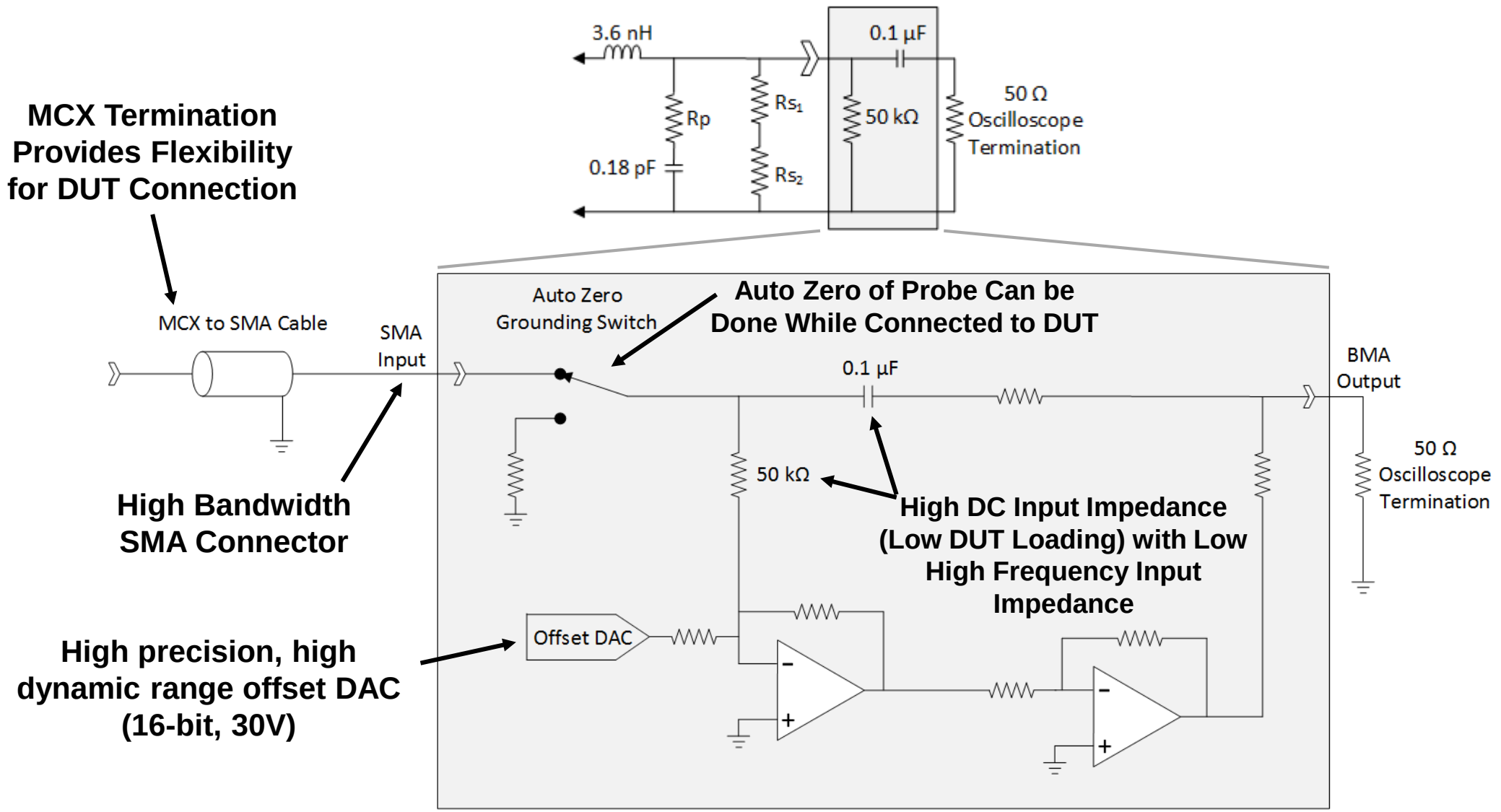
Browser Tip with 0Ω Resistor
(for low attenuation, good noise performance)

SMA to BNC Adapter
(for connecting directly to a scope BNC input if used as a PP066 Transmission Line Probe)

450Ω and 950Ω Resistors
(for use as 10x or 20x PP066 equivalent)

RP4030 Equivalent Circuit Diagram

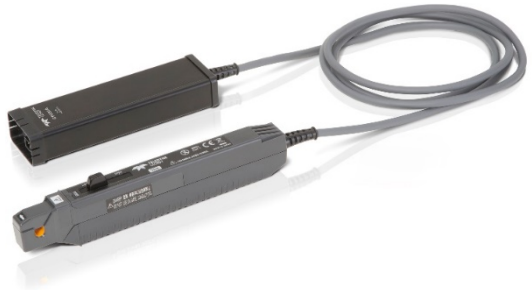
The RP4030 probe is shaded in gray, and the cable and oscilloscope are not shaded



Other Teledyne LeCroy Voltage and Current Probes

- Differential Amplifiers (DA1855A) and Probes (AP033) with 10x Gain
  - Ideal for shunt/series resistor measurements
  - Up to 100 dB CMRR

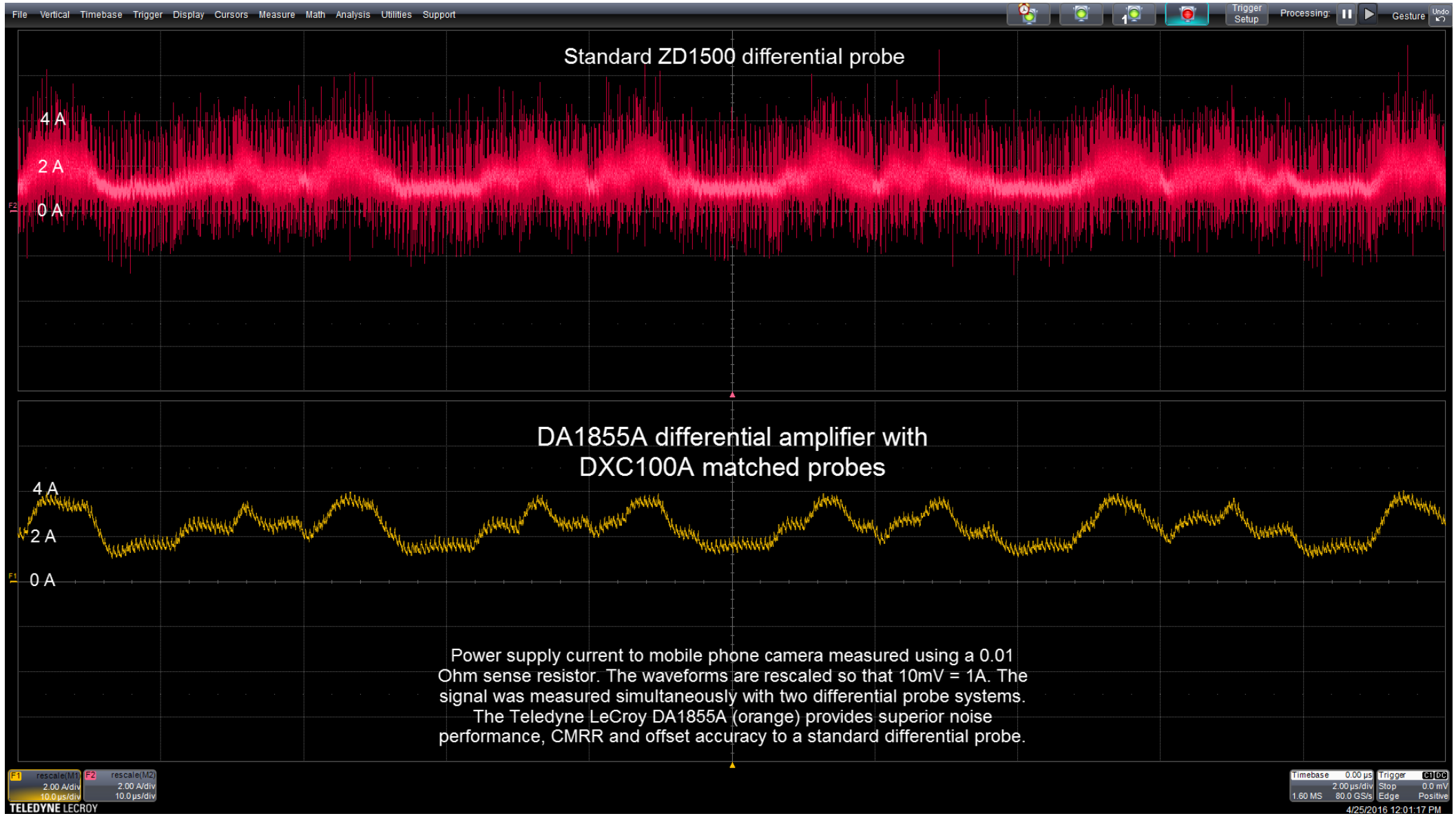
- High Sensitivity Current Probes
  - 50 or 100 MHz



- Low-cost 1 GHz Active FET Probe
  - Great for general probing or power sequence testing

Common-mode Rejection Ratio (CMRR) Performance Difference

Top is a conventional diff probe, bottom in a CMRR optimized probe with 10x gain



Power Integrity Measurement Examples

What is Power Integrity?

From Wikipedia (with reference to Eric Bogatin)

- **Power integrity** or **PI** is an analysis to check whether the desired voltage and current are met from source to destination. Today, power integrity plays a major role in the success and failure of new electronic products. There are several coupled aspects of PI: on the chip, in the chip package, on the circuit board, and in the system. Three main issues must be resolved to ensure power integrity at the printed circuit board level:[1]
  - Keep the voltage ripple at the chips pads lower than the specification (e.g. less than +/-50 mV variation around 1V)
  - Control ground bounce (also called synchronous switching noise, simultaneous switching noise, or simultaneous switching output (SSN or SSO))
  - Control electromagnetic interference (EMI) and maintain electromagnetic compatibility (EMC): the power distribution network (PDN) is generally the largest set of conductors on the circuit board and therefore the largest (unwanted) antenna for emission and reception of noise.

1. *Bogatin, Eric (13 July 2009). Signal and Power Integrity - Simplified. Pearson Education. ISBN 978-0-13-703503-8.*

Power Integrity Measurement Example 1

Jitter on a 10 MHz clock circuit is traced back to a 2.9 MHz Point-of-load (POL) DC-DC converter

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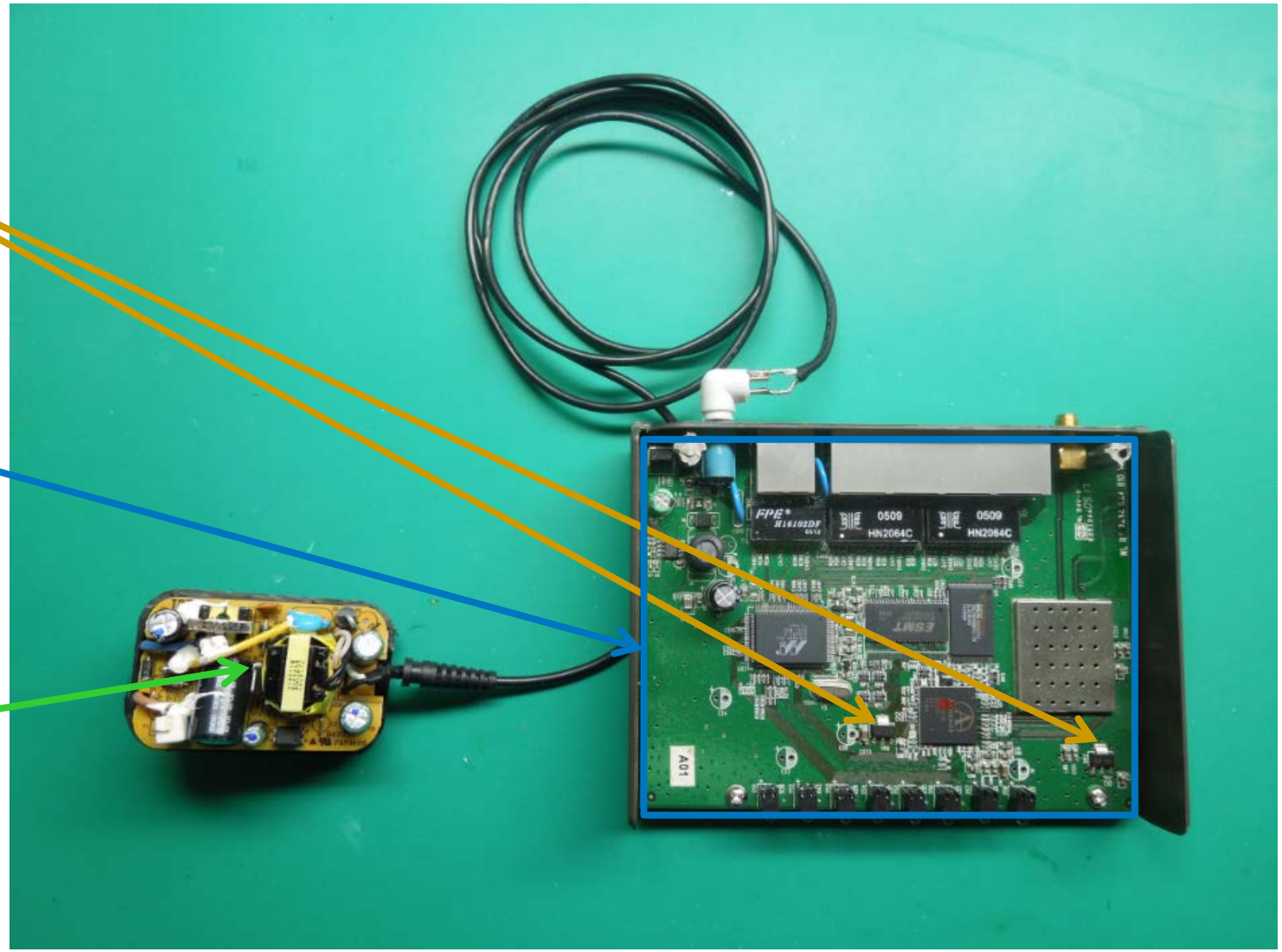
Overview of DUT

Power Delivery System for a Wireless Router

Point-of-Load (POL) DC-DC converter

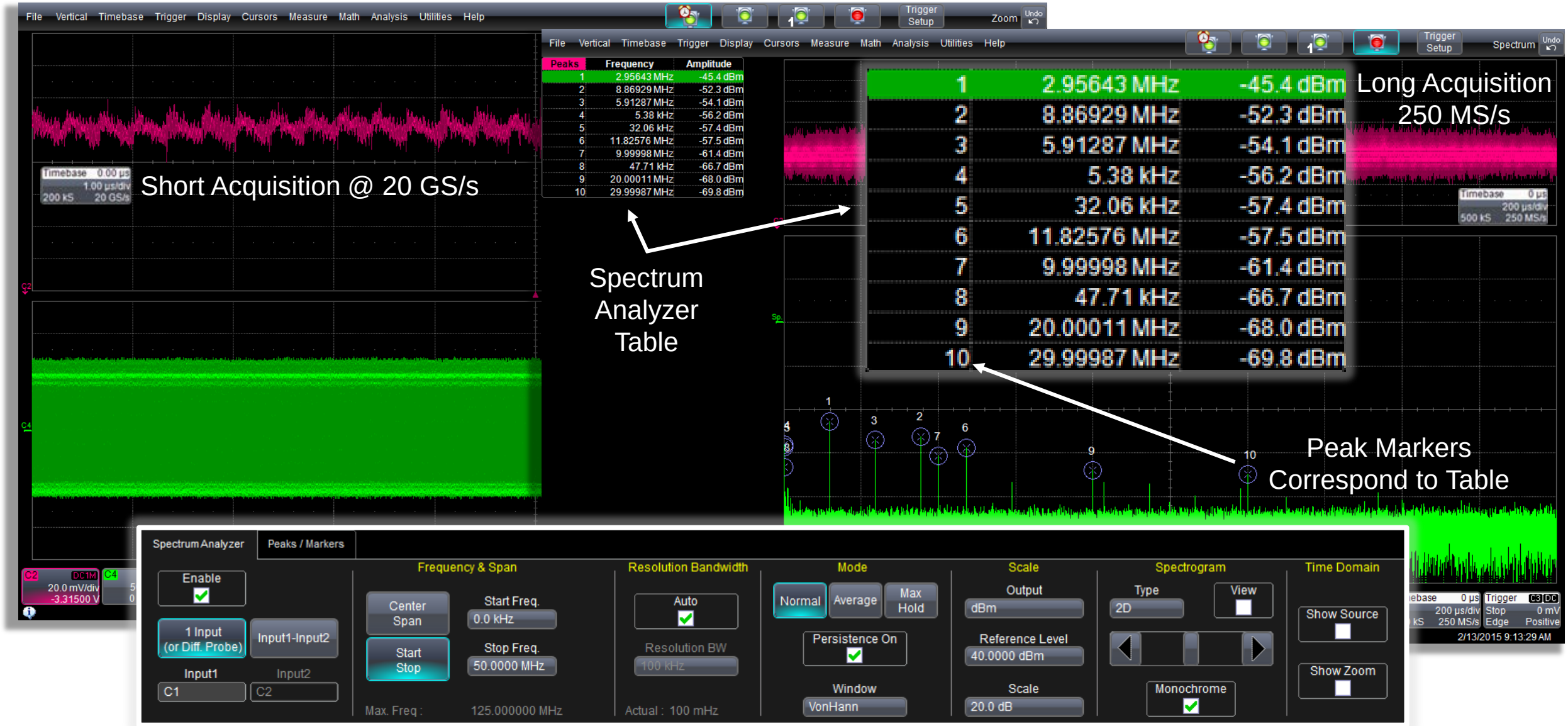
Power delivery network

Switched-mode AC-DC power supply



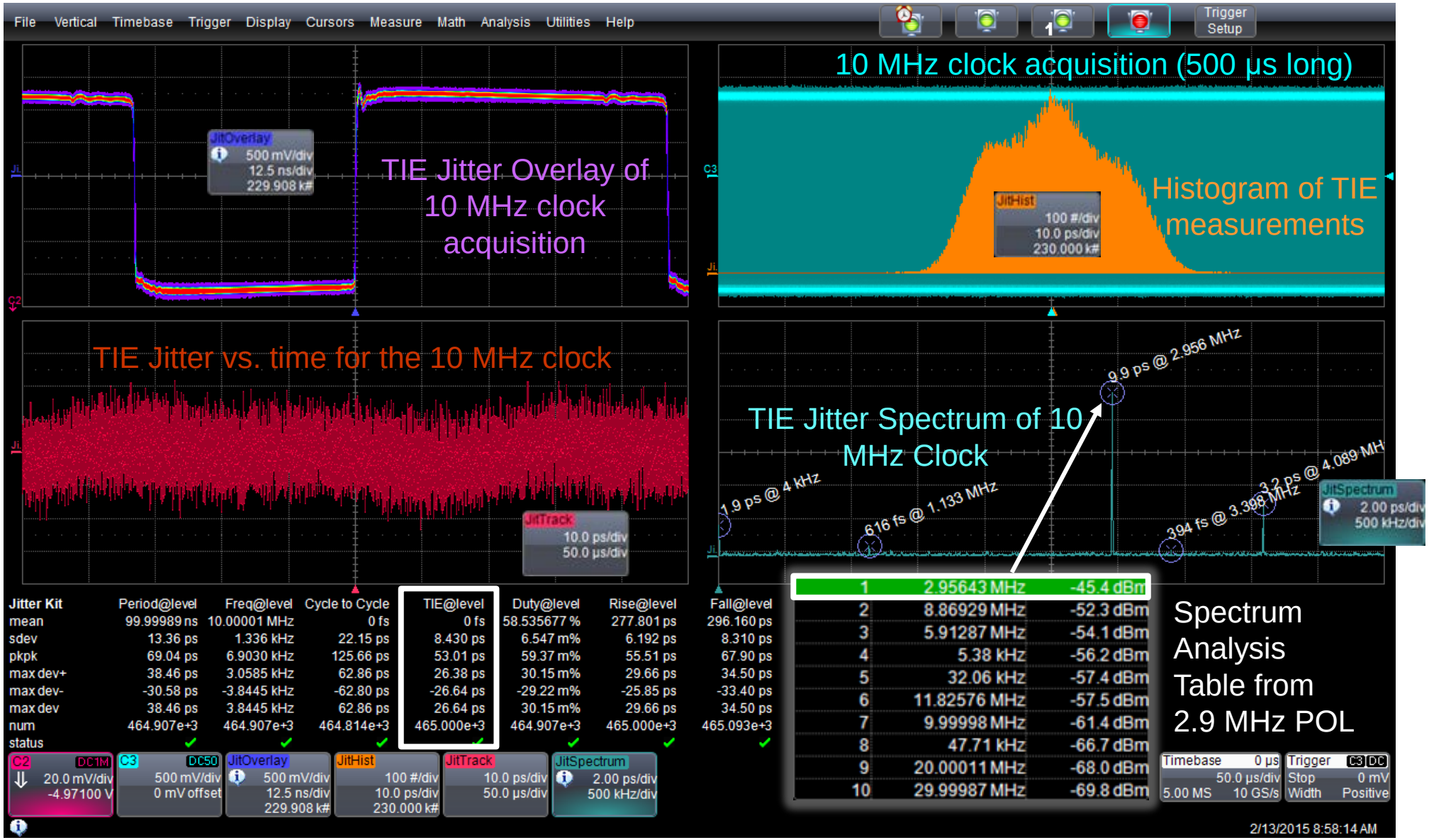
2.9 MHz POL DC-DC Converter Spectral Measurements

The oscilloscope Spectrum Analyzer capability is used to frequency peaks of the POL



POL Ripple Contributes to Clock Jitter

JitterKit can be used to quantify jitter on 10 MHz clock and trace it back to the POL



Power Integrity Measurement Example 2

Understanding the impact of the power delivery network (PDN) impedance on clock jitter coupling

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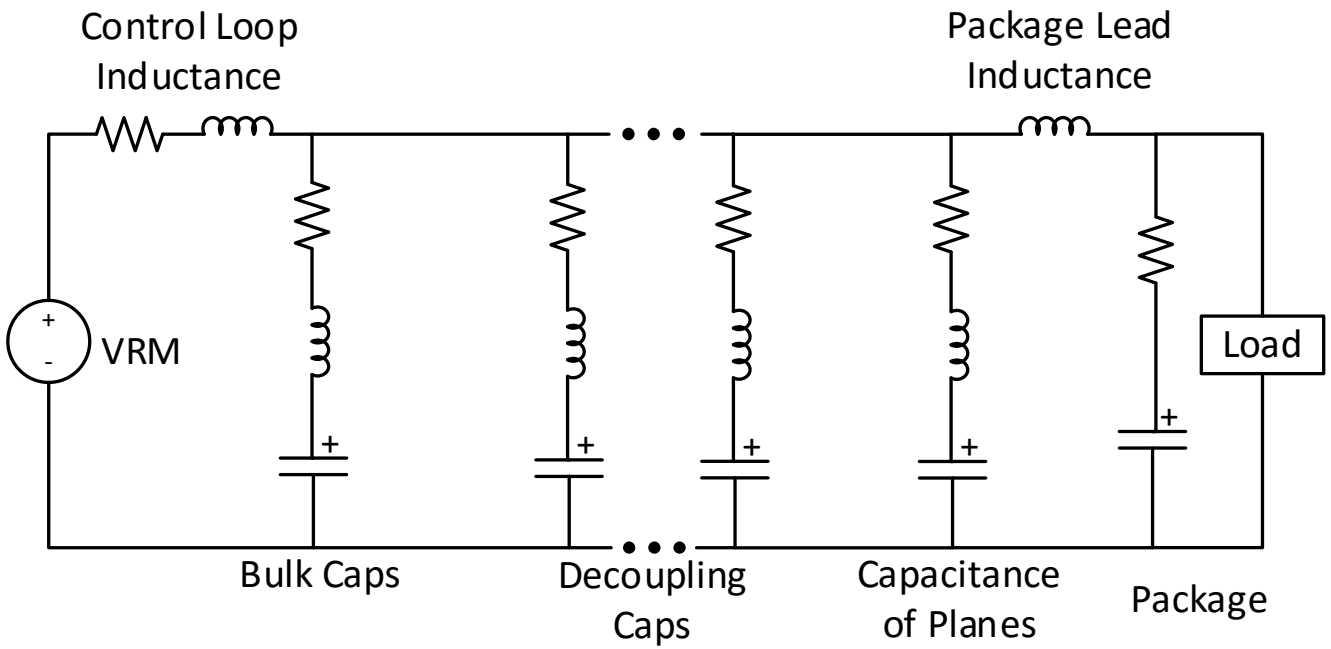
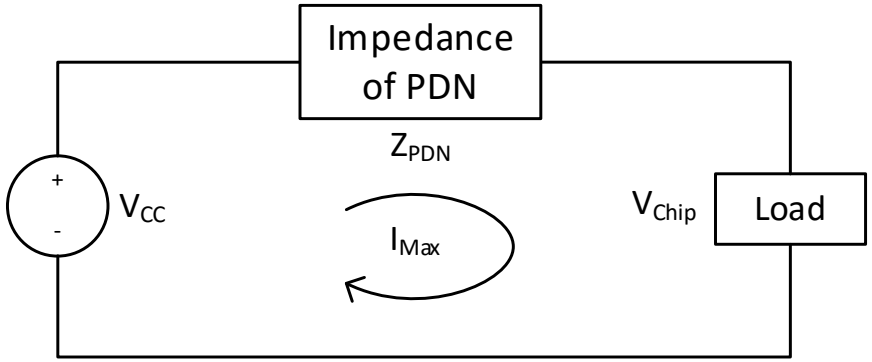
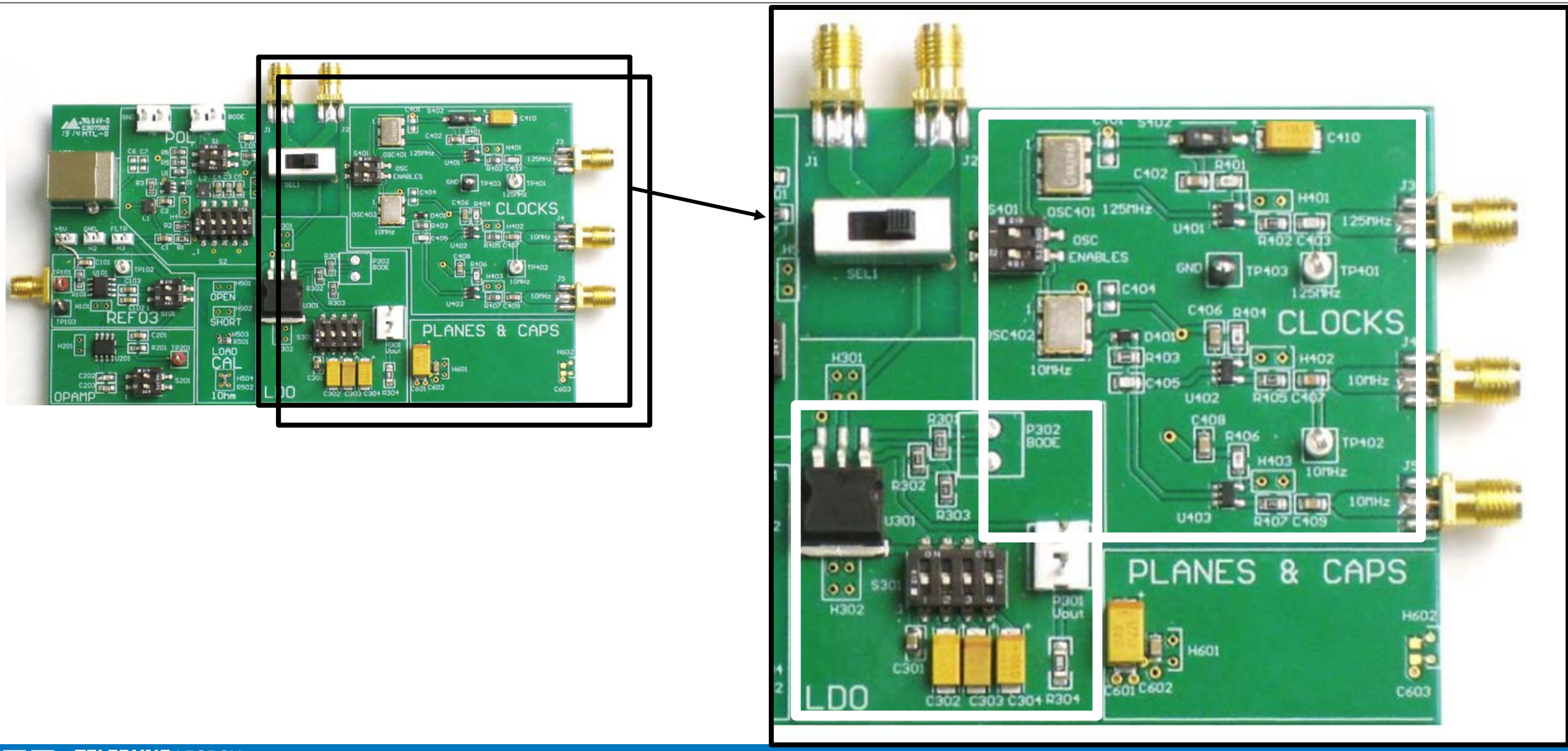
Background - The Importance of Impedance





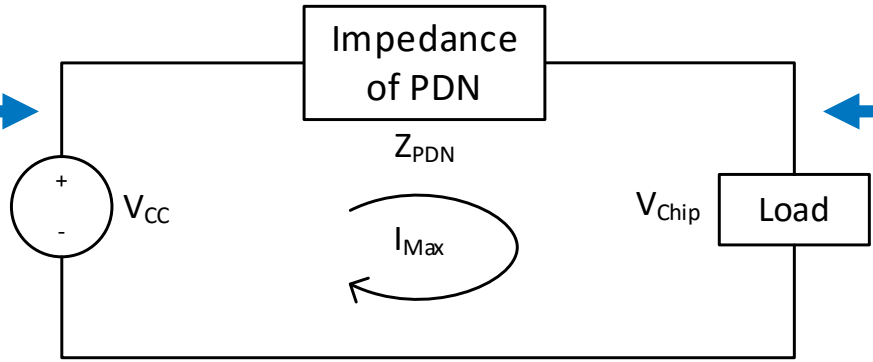
$$V_{cc} \neq V_{Chip}$$

An LDO DC-DC Converter Supplies Power to 10 and 125 MHz Clocks

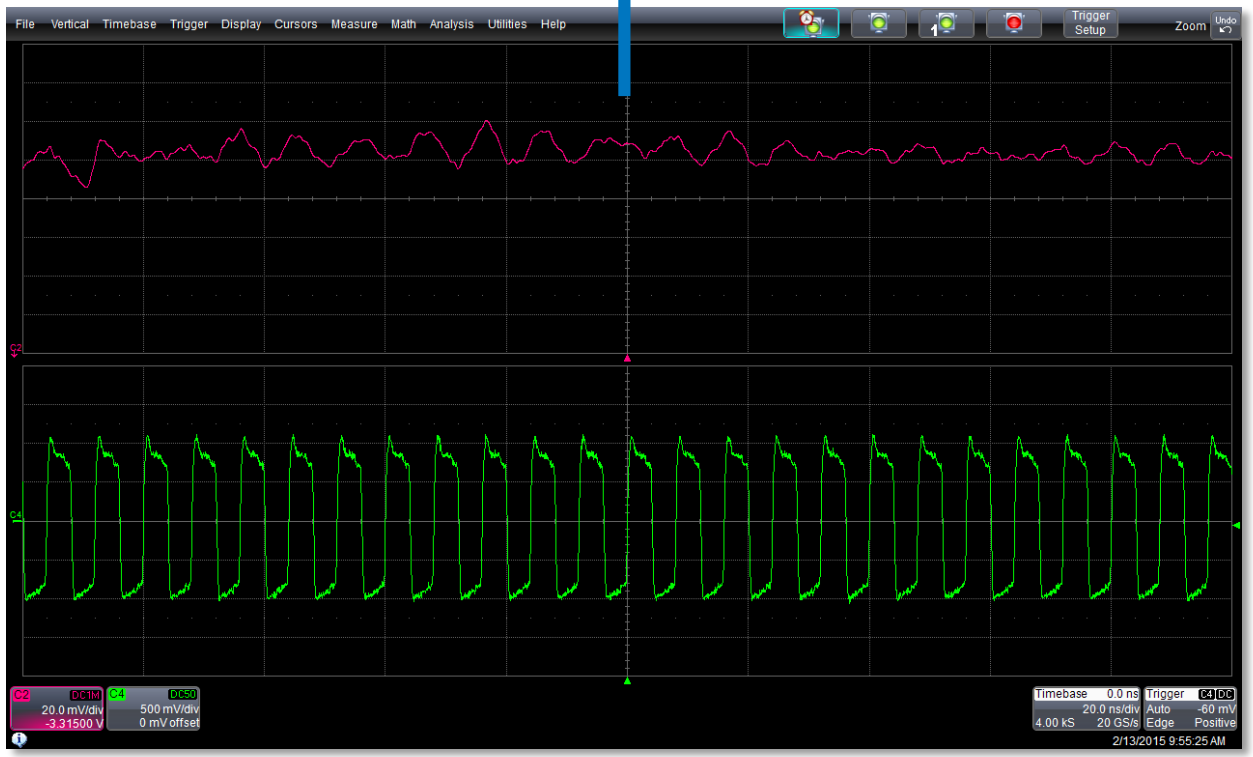


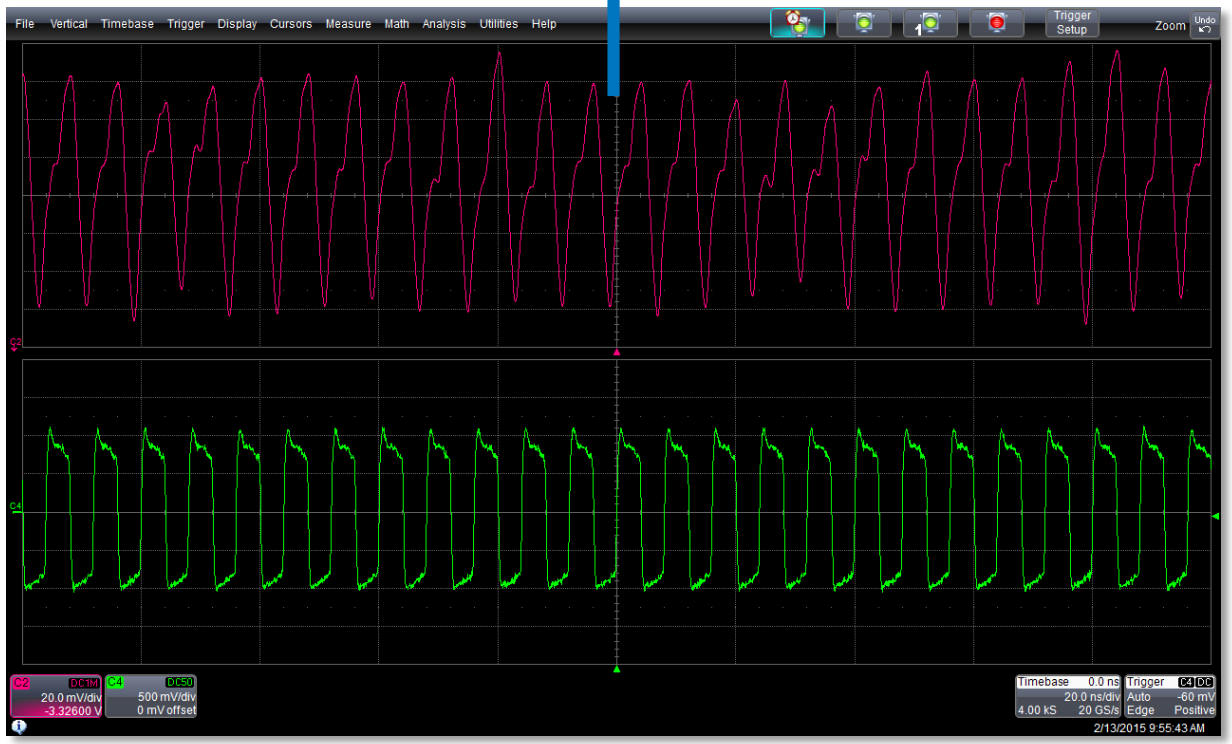
Impedance – Measurement Example

Power Rail Voltage Measured at V_{CC}

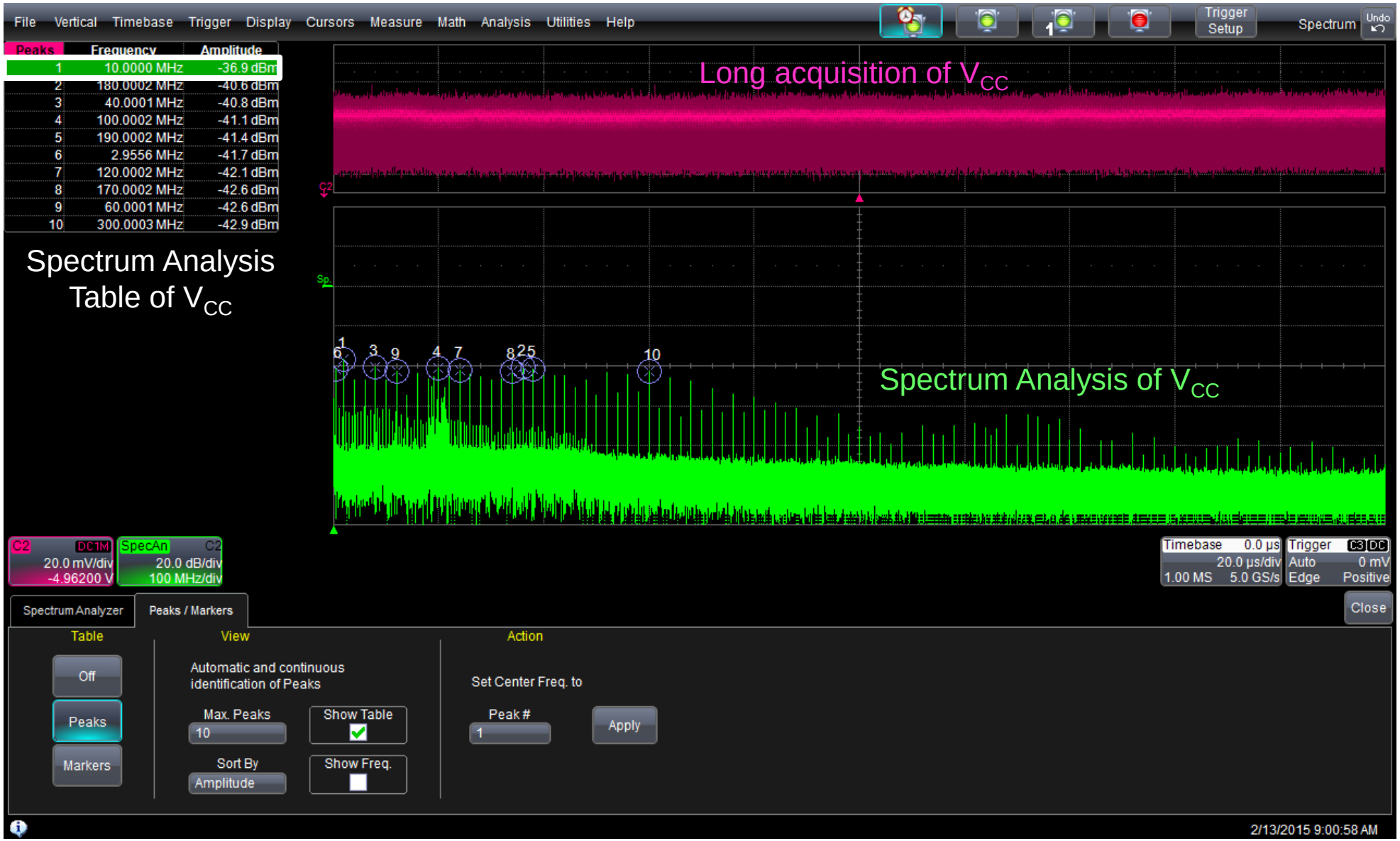


Power Rail Voltage Measured at V_{CHIP}



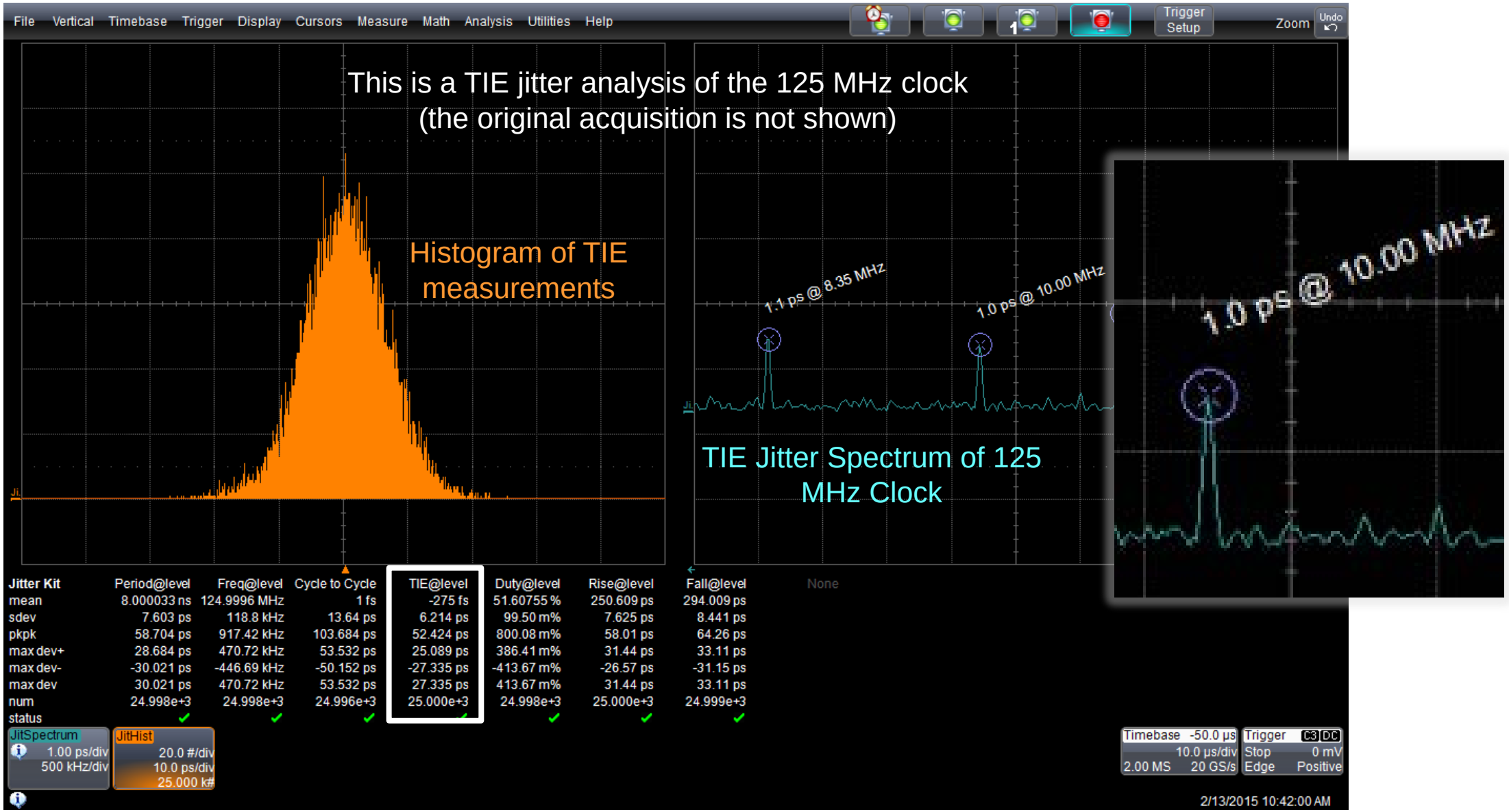


10 MHz Clock Causing Ripple on Input Voltage Rail (V_{CC})



10 MHz Clock Induced Ripple on V_{CC} Impacts 125 MHz Clock

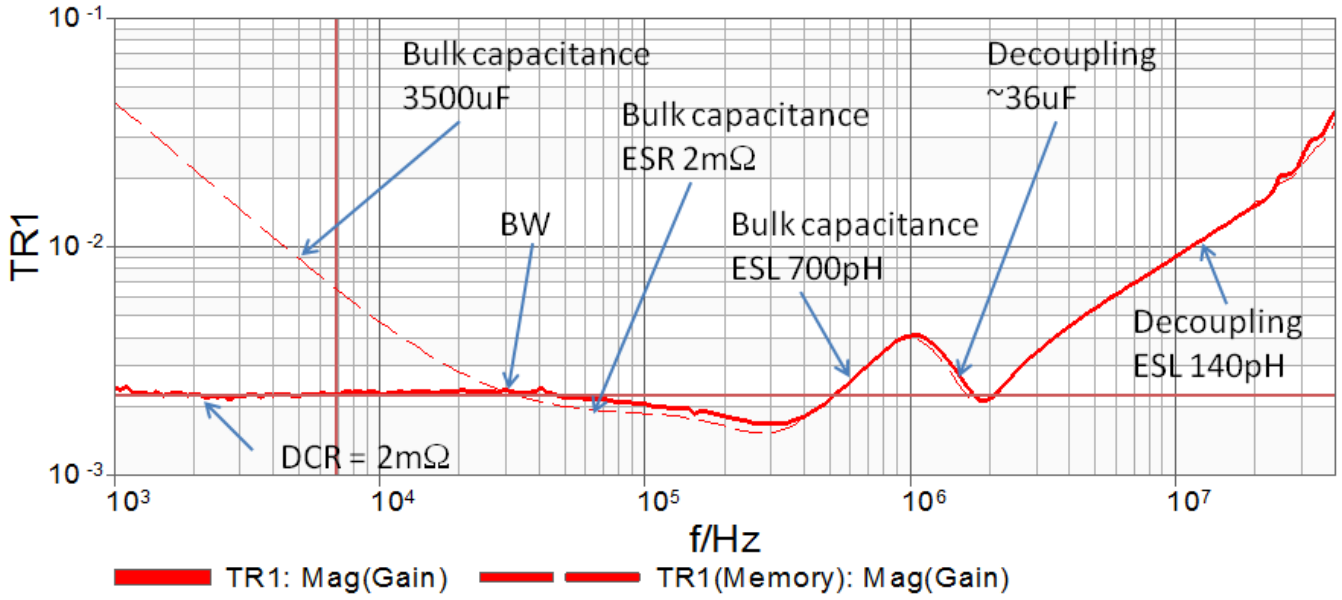
Ripple adds 1ps of jitter on the output of the125 MHz clock



Measuring Impedance of the PDN

The plot indicates the impact of the ESR and ESL on the circuit

Omicron Bode 100
40 MHz Network Analyzer



- Power/Voltage Rail behaviors during load changes correlate to PDN impedance
  - Equivalent series resistance (ESR) and inductance (ESL) for half-bridge output capacitor (C_{Out})
  - Voltage transients at load changes are primarily caused by ESL or impedance of the output cap at very high frequencies.
  - Slew rates impacted by the reactive power of the capacitor (Q_C)

Figure 1. An idealized load-transient plot

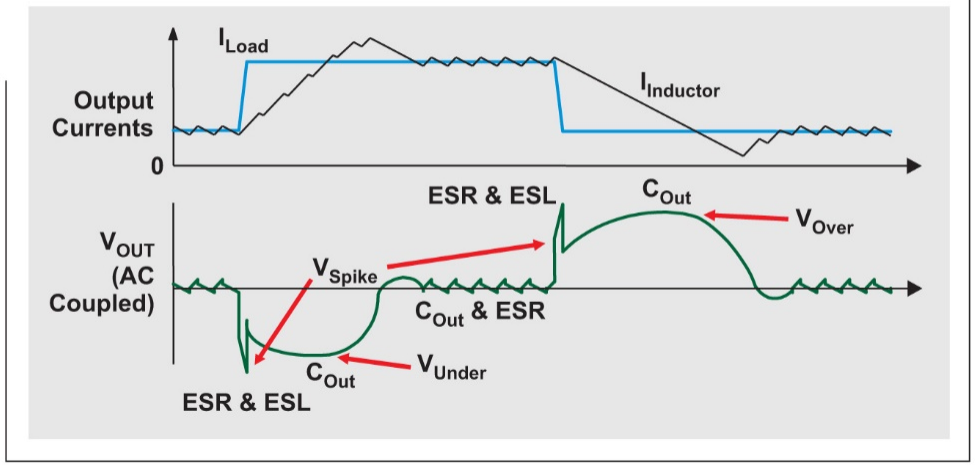
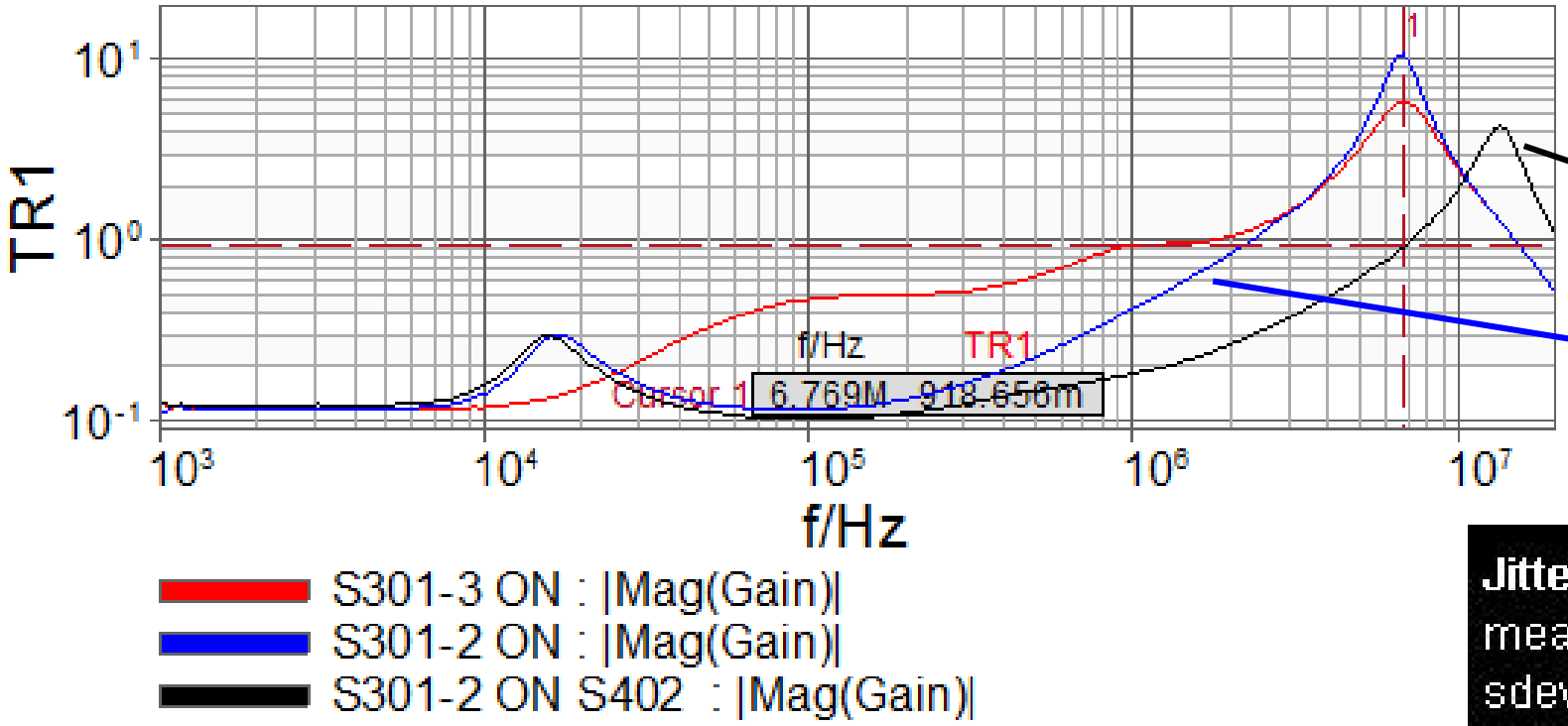


Image source http://www.powerelectronictips.com/ceramic-or-electrolytic-output-capacitors-in-dcdc-converters-why-not-both/

A Decoupling Capacitor Can Be Used to Lower Impedance

TIE jitter is reduced by more than 1ps$_{rms}$ in this example



S301-2 ON w/o decoupling C

S301-2 ON w/ decoupling C

Jitter Kit	TIE@level	TIE@level
	0 fs	0 fs
mean	7.070 ps	5.655 ps
sdev	74.289 ps	52.744 ps
pkpk	35.786 ps	23.470 ps
max dev+	-38.503 ps	-29.275 ps
max dev-	38.503 ps	29.275 ps
max dev	104.958e+3	54.978e+3
num	✔	✔
status		

Power Integrity
Measurement Example 3

High clock jitter and malfunction can be seen to be caused by POL DC-DC converter voltage droop.

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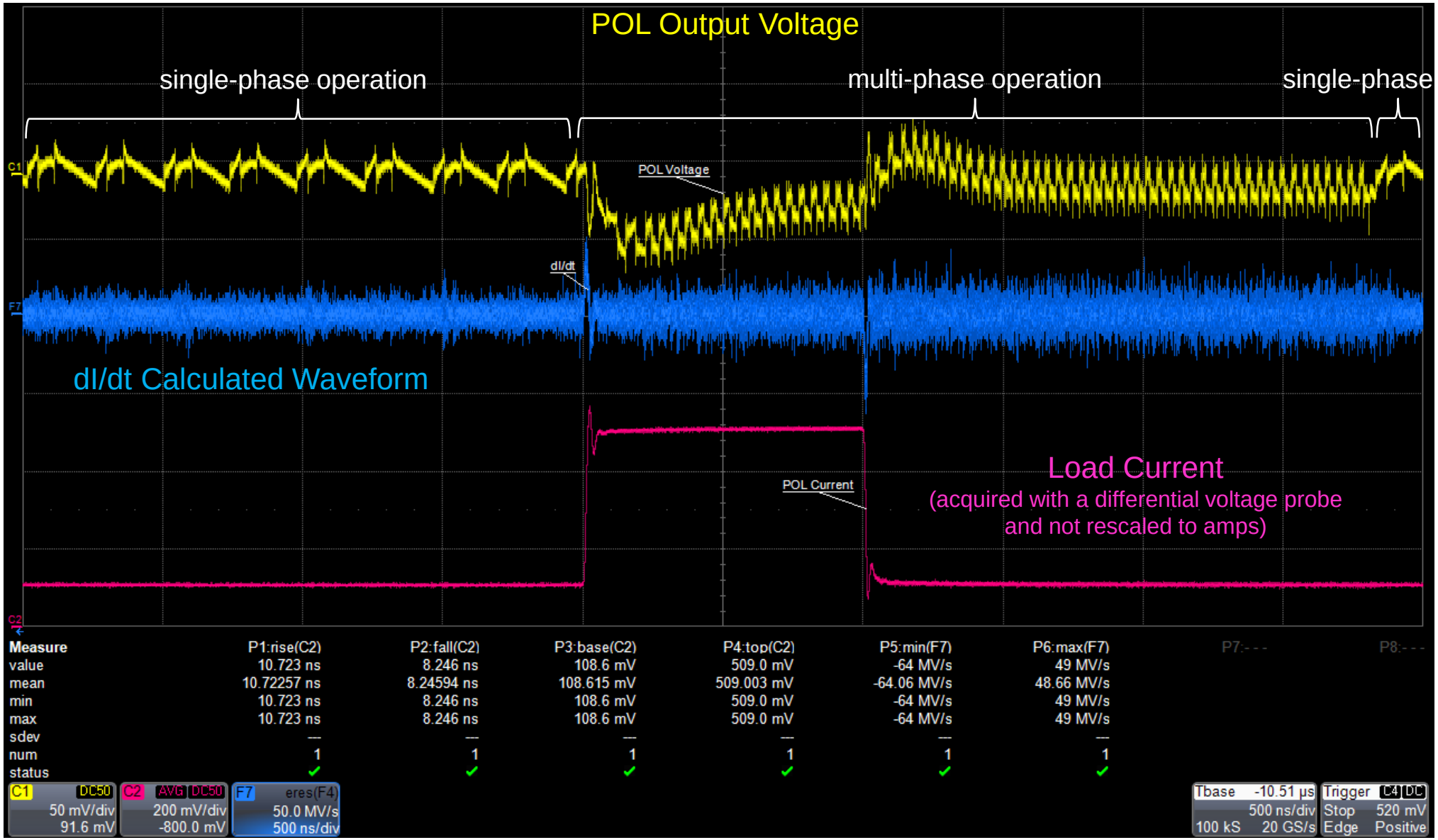
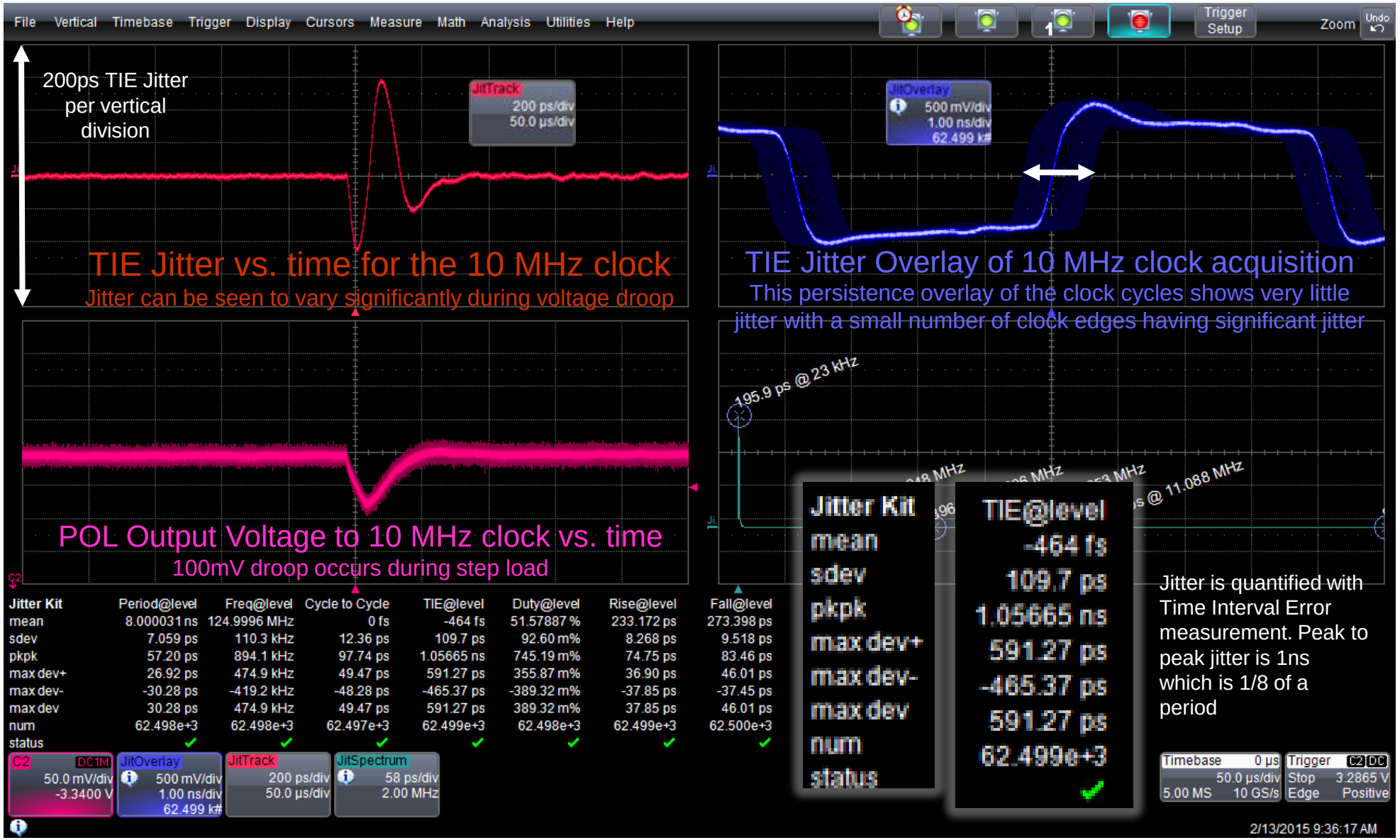
POL DC-DC Converter Transient Load Response



Transient Load Response Jitter Analysis

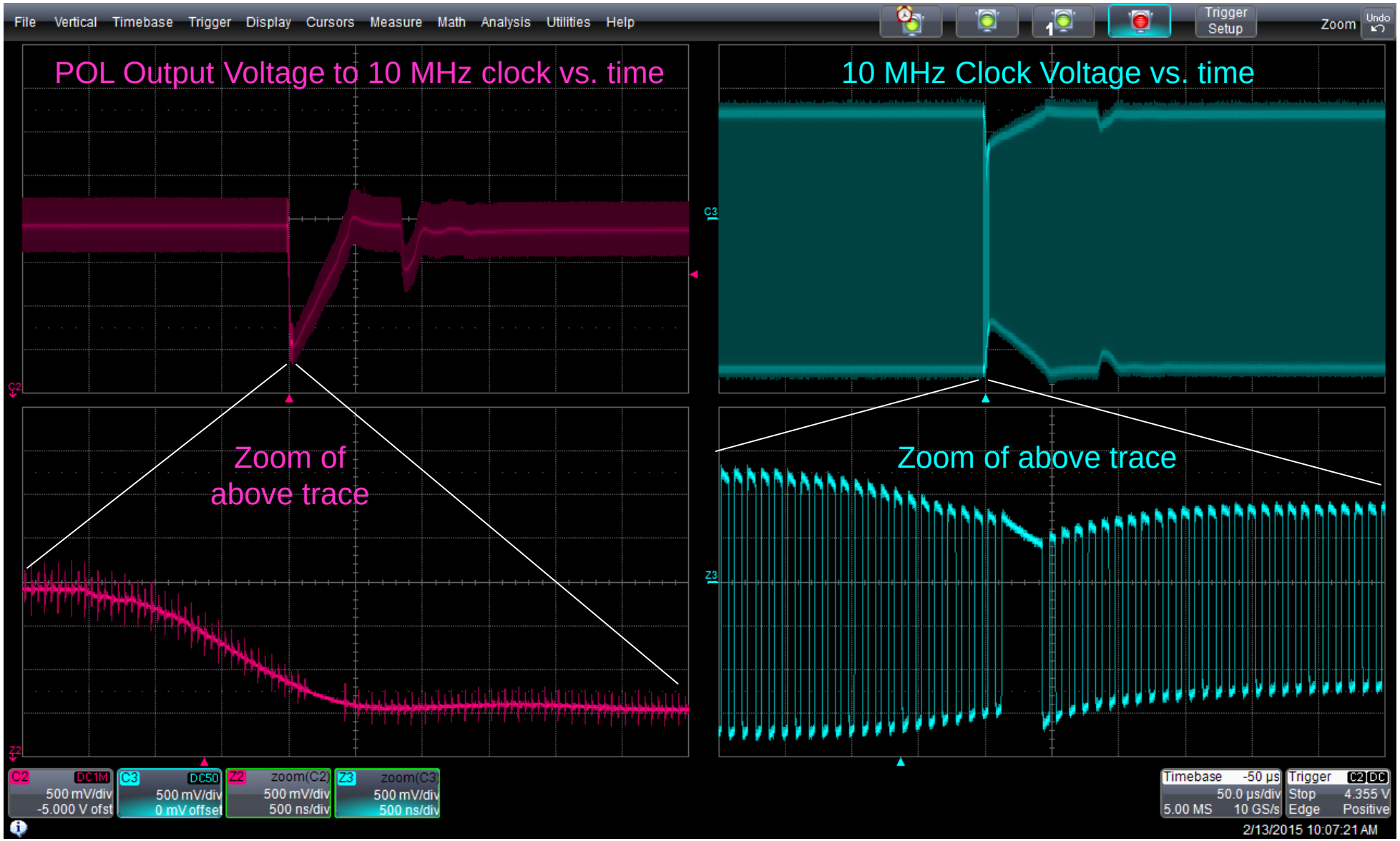
The POL output voltage droop to the clock causes large clock jitter



Jitter Kit	Period@level	Freq@level	Cycle to Cycle	TIE@level	Duty@level	Rise@level	Fall@level
mean	8.000031 ns	124.9996 MHz	0 fs	-464 fs	51.57887 %	233.172 ps	273.398 ps
sdev	7.059 ps	110.3 kHz	12.36 ps	109.7 ps	92.60 m%	8.268 ps	9.518 ps
pkpk	57.20 ps	894.1 kHz	97.74 ps	1.05665 ns	745.19 m%	74.75 ps	83.46 ps
max dev+	26.92 ps	474.9 kHz	49.47 ps	591.27 ps	355.87 m%	36.90 ps	46.01 ps
max dev-	-30.28 ps	-419.2 kHz	-48.28 ps	-465.37 ps	-389.32 m%	-37.85 ps	-37.45 ps
max dev	30.28 ps	474.9 kHz	49.47 ps	591.27 ps	389.32 m%	37.85 ps	46.01 ps
num	62.498e+3	62.498e+3	62.497e+3	62.499e+3	62.498e+3	62.499e+3	62.500e+3
status	✓	✓	✓	✓	✓	✓	✓

Transient Load Response – Power Switched on to a Second Clock

Load of second clock causes POL voltage droop and impacts 10 MHz clock functioning



Summary

Teledyne LeCroy Equipment for Digital Power Management and Power Integrity Analysis and Testing

12-bit, 8 channel, 4 GHz Oscilloscopes

Digital Power Management Analysis Software

Comprehensive Probe Offering

Serial Trigger, Decode, Measure/Graph and Eye Diagram Options

Questions?

Please visit us at Booth 733
in the Exhibition Hall