TELEDYNE LECROY
Everywhereyoulook™

Summit™ T54 Protocol Analyzer
for PCI Express® 5.0

Key Features

Find errors fast
- One button error check
- Fast upload speed
- Large trace memory
- Powerful triggering/filtering

See and understand the traffic
- Get useful information
- More choices of data views
- More ways to analyze data
- Custom decoding and reports

Data capture
- 100% data capture at 32.0 GT/s on all link widths up to x4

Deep memory buffer
- Up to 64 GB depth

PCIe storage protocols supported
- NVM Express
- NVMe-MI
- SATA Express (ATA/AHCI-PCIe)
- SCSI Express (SOP-PQI)

Virtualization protocols
- SRIOV
- MRIOV
- ATS

Sideband signaling
- SMBus
- CLKREQ#
- WAKE#
- PERST#

Supports CXL
Supports Lane Margining
Supports MultiPort™ analysis
BitTracer™
Supports CrossSync™ PHY
Supports PCIe IDE/DOE
Supports CXL IDE

The Summit T54 offers advanced features such as: support for PCI Express® 5.0 Specification; data rates of 2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s and 32.0 GT/s; full data capture on bidirectional link widths of x1, x2, x4; and up to 64GB of trace memory. The product is ideal for high-performance protocol development for add-in boards, servers and workstations, and for customers currently working on PCIe® 3.0, 4.0, 5.0 or CXL.

Flexible Hardware

The Summit T54 protocol analyzer features support for the PCIe 5.0 technology at speeds of up to 32.0 GT/s and up to x4 link widths. It also provides up to 64GB of recording memory which can be expanded to support up to 128GB of recording memory at up to x8 link widths by cascading a second Summit T54 system. The Summit T54 can be controlled through USB or can be remotely networked and controlled through a 1000baseT Ethernet connection. It can also be synchronized with other high-speed protocol analyzers or oscilloscopes from Teledyne LeCroy. Users can get started with the Summit T54 today licensed at PCIe 3.0 or 4.0 speeds and then simply upgrade the system to support PCIe 5.0 specification when the time comes.

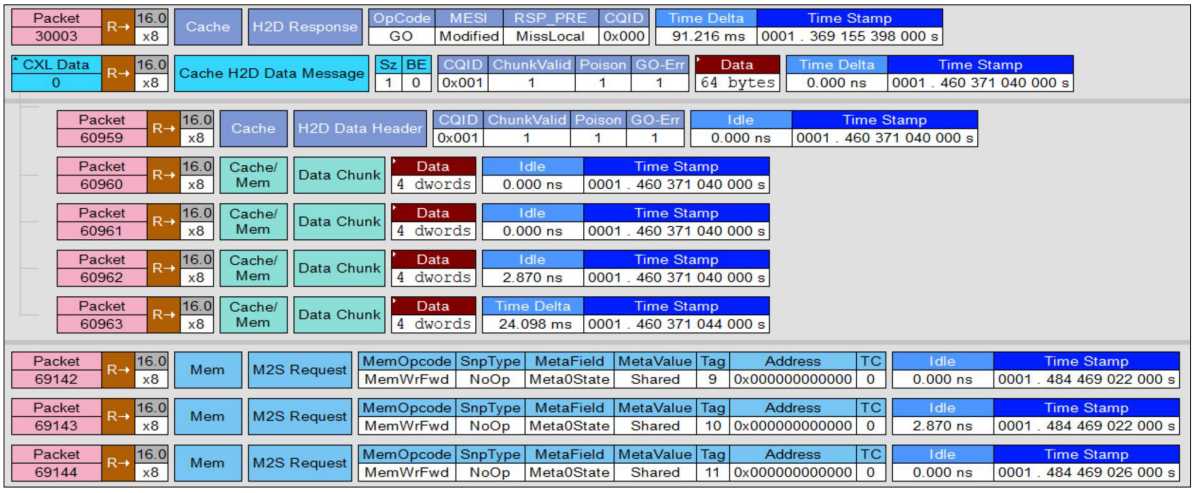
Compute Express Link Analysis

The Summit T54 is also a fully featured Protocol Analyzer for CXL (Compute Express Link) Links. Support is provided for CXL.io, CXL.mem and CXL.cache with full decoding from the FLIT layer to the CXL Message layers. The Summit T54 supports triggering, filtering and decoding of links up to 4 lanes (8 lanes when cascading 2 units) and speeds up to 32GT/s.

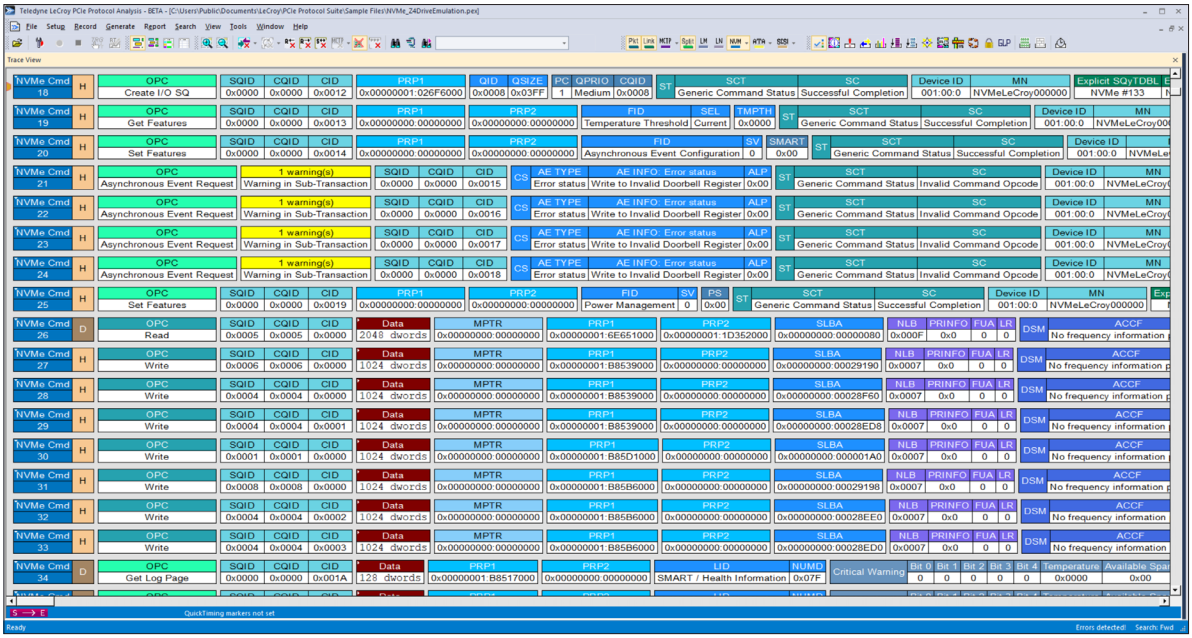
Capturing is performed by connecting a PCIe 5.0 interposer or probe to the Device Under Test (DUT). Interposers are offered in link widths of x1 or x4. Know that your data is accurate through reliable and complete decodes of Transaction Layer Packets (TLPs), Data Link Layer Packets (DLLPs), and all primitives for PCI Express. Setting up and taking a trace is simple to do without the worry of extra plugin platforms or complex networking issues.

Packet				Type	VLSM State	Target	Idle	Time Stamp
2	R→	32.0 x8	ALMP	Request	ACTIVE	CXL.io	10.000 ms	0000 . 030 000 200 000 s

CXL Trace



NVMe Trace



A Wealth of Information

The Summit T54 for PCI Express 5.0 utilizes the CATC Trace™, Spreadsheet View, LTSSM State View, Bit Tracer View and other focused views to assist users in analyzing how PCI Express protocol components work together in diagnosing problems. These various interfaces help find errors fast by using the powerful triggering, filtering and error reporting These diverse views create a powerful and an intuitive expert software system, embedding detailed knowledge of the protocol hierarchy and intricacies as defined in the protocol specification.

Graphical displays have been optimized for fast and easy navigation through a captured traffic session. Users are alerted as violations are detected at all levels of the protocol layering and can easily drill down to areas of interest or collapse and hide fields that are not relevant. Protocol data can be viewed in several ways from logical to chronological, and by events unique to PCI Express.

All Teledyne LeCroy protocol analyzers feature a hierarchical display of protocol traffic summaries, detailed error reports, powerful scripting, and the ability to create user-defined test reports, which allow developers to troubleshoot intricate problems and finish their projects on time. Users of Teledyne LeCroy systems appreciate the rich library of decodes and analysis capabilities that are available on all of Teledyne LeCroy's PCIe test tools.

The Summit™ T54 is up to the challenge by offering decoding for Storage protocols like NVM Express® and SATA Express®. DataCenter monitoring technology such as NVMe queue characterization, NVMe-MI and out-of-band SMBus signaling which is decoded and synchronized with PCI Express can be analyzed for protocol traffic issues. If IO virtualization is important SRIOV and MRIOV is also decoded and analyzed. Two Summit T54 protocol analyzers can be expanded together to support PCIe® 5.0 at 32.0 GT/s at x8 link width applications.

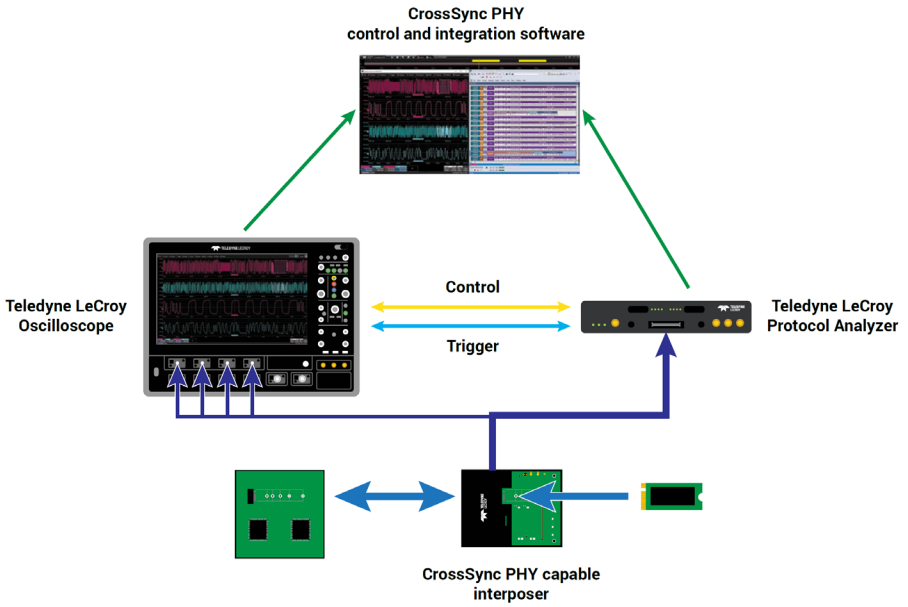
Want to get down to the byte level and see traffic just before lane alignment? BitTracer™ software option records the bytes exactly as they come across the link, allowing debugging of PHY layer problems and combining the features of a logic analyzer format with decoded issues. If IO virtualization is important SRIOV and MRIOV are both fully decoded and analyzed.

CrossSync™ PHY for Deeper Insight into Link Behavior

Interoperability issues can lead to finger-pointing exercises that cost money and time-to-market. Teledyne LeCroy CrossSync PHY software and interposers seamlessly merge the functions of your Teledyne LeCroy protocol analyzer and oscilloscope - giving insight into link behavior that no other instrument can provide. CrossSync PHY enables precise, intuitive navigation between time-correlated protocol analyzer and oscilloscope traces - select a protocol event to see the protocol trace occuring at the same moment and easily measure timing relationships between protocol and electrical domains.

Correlated electrical and protocol views of a link speed change from 8 to 16 GT/s.

- Dynamic Link Behavior
- Power Management Transitions
- Dynamic Power Characterizations



Specifications	
Host Machine Minimum Requirements	64-bit (x64) versions of Windows® 11, Windows 10, Windows Server 2016, and Windows Server 2019. o The latest Service Pack available for the Windows OS in use is required. 4 GB of RAM; storage with at least 2 GB of free space for the installation of the software and additional space for recorded data; display with resolution of at least 1024x768 with at least 16-bit color depth; USB 2.0/3.0/3.1 port and/ or 100/1000 Mbps Ethernet network interface. For optimal performance, please refer to our recommended configuration in the product documentation.
Recording Memory Size	Summit T54 Protocol Analyzer: Up to 64 GB
Data Rates Supported	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s, 32.0 GT/s (PCI Express® 5.0)
Ports	Summit T54 Protocol Analyzer: Downstream and Upstream reference clock inputs, USB 3.0 Type C connector, Trigger in and out, 1 GB/s ethernet port, Sync in/out expansion port
LEDs	Power LED, Status LED, Trigger LED, Two Data Rate Displays (2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s, 32.0 GT/s)
Dimensions and Weight	Summit T54 Protocol Analyzer: 304.48 x 44.45 x 345.6 mm (12" x 1.75" x 13.61"), 4.9 Kg (11 lb)
Power Requirements	90 - 264 VAC, 47 - 63 Hz, 300W
Environmental	Temperature (operating): 5° to 40°C (41° to 104°F) Temperature (non-operating): -20° to 60°C (-4° to 140° F) Humidity (operating): 5% to 80% RH (non-condensing) at <=30°C, 50% max RH (non-condensing) at 40°C Humidity (non-operating): 5% to 95% max RH (non-condensing)

Additional Features

- ✓ Protocol Hierarchical Display
- ✓ Spreadsheet View
- ✓ Queue Utilization
- ✓ NVMe
- ✓ SATA Express
- ✓ NVMe-MI
- ✓ SMBus
- ✓ CXL Decoding
- ✓ ZeroTime™ Search
- ✓ Dword View
- ✓ LTSSM View
- ✓ Header Field Viewer
- ✓ Config Spec Viewer
- ✓ TLP Packet Script Decoding
- ✓ Timing Calculator
- ✓ Trigger/Filter Control
- ✓ Performance Metrics
- ✓ Expert Triggering
- ✓ Trace Expert
- ✓ Expert Graphical Bus Utilization View
- ✓ Verification Script Engine
- ✓ 1 GB/s Ethernet & USB 3.0
- ✓ TCG Decoding
- ✓ CrossSync PHY Capable
- ✓ Supports PCIe Integrity and Data Encryption (IDE)
- ✓ Supports CXL IDE

Ordering Information

Product Description	Product Code
Summit T54 (licensed as a Gen5 x4 analyzer at 8GB, no probes or cables, includes G5 Capable Module)	PE195AAA-X
Summit T54 (licensed as a Gen4 x4 analyzer at 8GB, no probes or cables, includes G5 Capable Module)	PE196AAA-X
Summit T54 (licensed as a Gen3 x4 analyzer at 8GB, no probes or cables, includes G5 Capable Module)	PE197AAA-X

Local sales offices are located throughout the world.
Visit our website to find the most convenient location.

1-800-5-LeCroy • teledynelecroy.com

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