TELEDYNE LECROY
Everywhere**you**look™
quantumdata

quantum**data**™ M41d
DisplayPort HBR3 Video
Analyzer/Generator
Testing up to 8.1Gb/s Link Rates
Entry Level Functional Tester Upgradable to Full Compliance

Key Features

- **Run DisplayPort functional tests upgradable to full protocol compliance tests up to full DP 1.4 specification**
- **Equipped with both DP standard and USB-C ports for Tx and Rx function—all test features supported through either type of connector**
- **View Power Delivery (PD) negotiations for USB-C DP Alt Mode**
- **Run functional tests on displays and monitors up to 8.1 Gb/s link rates with large format and test pattern library**
- **Generate Display Stream Compression (DSC) select patterns and configure slices and video parameters**
- **Configure link training parameters to test display's handling**
- **View EDID and DPCD registers**
- **Access DSC Test CRC registers for automated verification of source DSC compression**
- **Test DP sources up to 8.1 Gb/s link rates; view incoming video and meta-data—including DSC compressed--from a source device in real time**
- **Capture and decode incoming video, protocol and control packets—including Display Stream Compression (DSC)**
- **Run Pixel Error tests on cables and distribution equipment**
- **Monitor Aux Channel transactions as a DP source or sink**
- **Passively monitor Aux Channel between a source & display even at 8.1Gb/s link rates**
- **Run DP 1.4 Link Layer compliance tests on sources and sinks up to 8.1 Gb/s link rates**
- **Run DP 1.4 EDID compliance tests on sink devices**
- **Run DP 1.4 Forward Error Correction (FEC) compliance tests**
- **Run DP 1.4 Display Stream Compression (DSC) compliance tests for sources & sinks**
- **Run HDCP 2.2 compliance tests on DisplayPort sources, sinks and repeaters**
- **Run audio tests using programmable LPCM sine wave audio tones and compressed formats**
- **Run tests on embedded DisplayPort (eDP) 1.4b sources and panels using fast link training and ALPM**
- **Test eDP backlight control functions on panel using either backlight control pins or Aux Channel control commands**

The Teledyne LeCroy quantumdata M41d Video Analyzer/Generator provides an unprecedented combination of functional and compliance testing for video, audio and protocol of DisplayPort devices. The M41d supports HBR3 1.62, 2.7, 5.4 & 8.1 Gb/s data rates on 1, 2 & 4 lanes on its Tx video generator port and its Rx analyzer port for both the standard DP ports and the new USB-C ports with DP Alt Mode. The protocol analyzer provides real time analysis and deep analysis using captures of incoming DisplayPort streams from source devices including DSC/FEC compressed streams. The M41d's video generator can be used for testing displays, USB-C adapters, extenders, etc. The M41d is equipped with all the standard video timings and test patterns necessary for testing modern displays. The M41d supports a full suite of link layer compliance tests for both sources and sinks including compliance tests for forward error correction (FEC). EDID compliance tests are also supported.

The Tx and Rx ports support Auxiliary Channel analysis of the DP aux channel, and the USB-C ports support aux channel analysis of the USB-C Configuration Channel. The adjunct Aux Channel monitoring board supports passive monitoring of the DisplayPort aux channel via full-size DisplayPort connectors, between a source and display. This enables analysis of link training and HDCP interoperability between devices.

For developers of Embedded DisplayPort (eDP), the M41d offers the hardware necessary to support a variety of optional eDP features. Initial support includes fast link training, alternate scrambler seed, Advanced Link Power Management (ALPM) and Tx backlight control. A pin header is available to provide access to the backlight Tx control test feature.

Operation

The M41d supports video generation and analysis of the FRL/FEC HDMI data streams through the user friendly ATP Manager which presents the data in an easy to understand way. The ATP Manager can be controlled either via a laptop connected to the M41d RJ45 LAN port or through a USB keyboard and mouse and a connected UHD HDMI admin display.

Admin display for ATP Manager

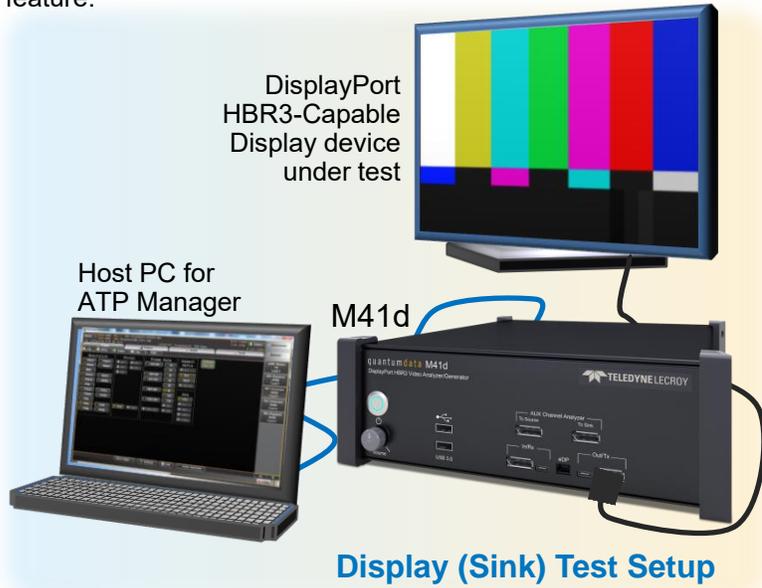**M41d** DP Video
Analyzer/Generator

Keyboard & mouse
for M41d ATP
Manager Control

DISPLAY TESTS – VIDEO/AUDIO TESTING

Video Generation

The quantumdata M41d supports video and audio functional testing at link rates up to 8.1 Gb/s on 1, 2 and 4 lanes to support high resolution formats. The M41d has an extensive set of video formats and library of test patterns. You can set any pattern in motion to test motion artifacts with the Image Shift feature.

DisplayPort HBR3-Capable Display device under test

Host PC for ATP Manager

M41d

Display (Sink) Test Setup

Link Training Control and Configuration

The M41d 's link training control feature enables you to configure the link training parameters. You can set limits on the lane count and link rate and allow the link training engine to establish link training based on those limitations or you can force link training parameters—lane count, link rate, voltage swing, pre-emphasis.

Link Training Control and Configuration

Alt Mode Negotiation

The USB Type C Transmit connector participates in discovery, power contract negotiation, and DP Alt Mode negotiation. The protocol messages can be monitored on the Auxiliary Channel Analyzer (right).

Format Selection
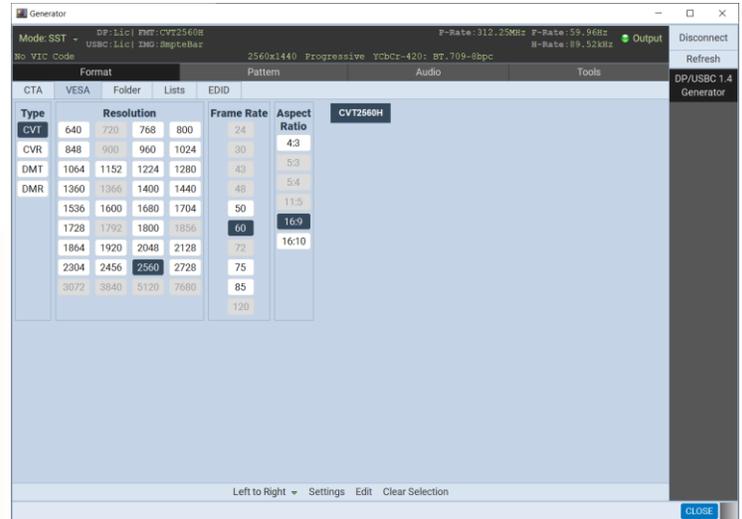
Audio Testing

The M41d offers a programmable LPCM audio sine wave generator enabling you to set the number of channels (up to 8), the amplitude, frequency, sampling rate and bit depth for uncompressed formats.

LPCM Audio Testing
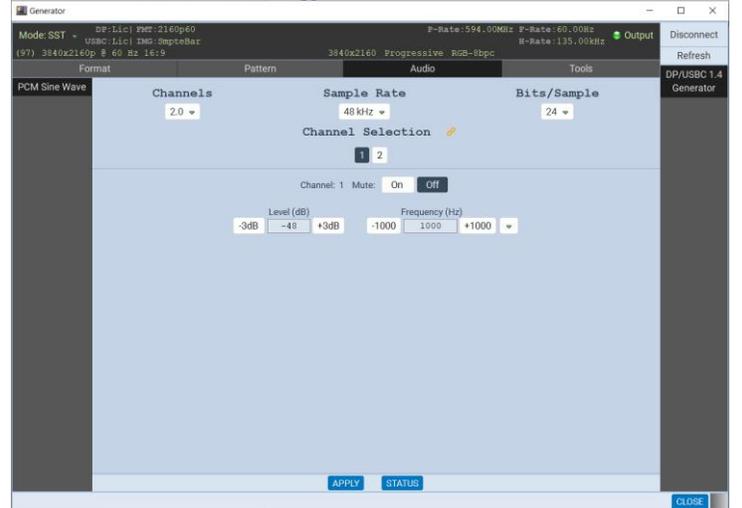
Aux Channel Analyzer – DP Alt Mode Negotiation
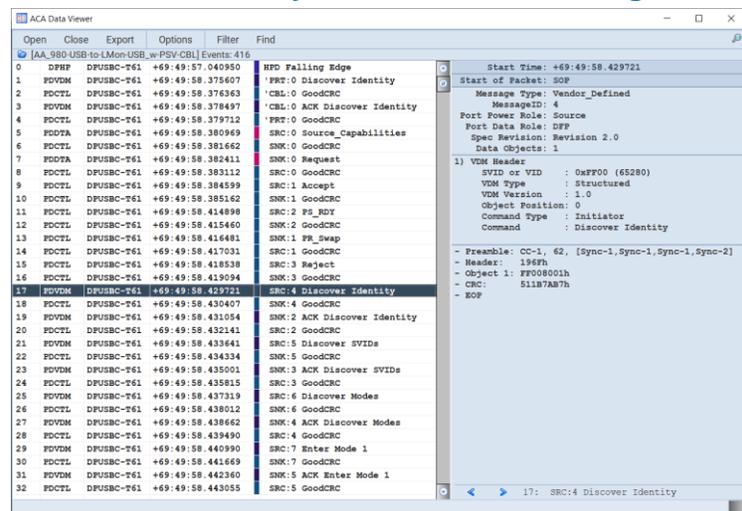
Protocol Testing

The quantumdata M41d offers a variety of features for testing DisplayPort protocols. You can verify HDCP 2.2 authentication transactions between the module's Tx port and a DP display. The M41d's EDID Decode feature enables you to examine the EDID of the connected display in text. The DPCD Decode feature enables you to examine the DPCD registers of the connected display. You can read the EDID and/or the DPCD of downstream MST nodes.

Display (Sink) Test Setup

Multi-Stream Transport

The M41d emulates an MST source for testing an MST branch device or MST-capable monitor. Up to four (4) streams are supported with a depth of one. The Auxiliary Channel Analyzer (ACA) utility depicts the MST negotiations with the connected MST Rx device.

Auxiliary Channel Analyzer

The M41d 's Auxiliary Channel Analyzer (ACA) feature enables you to monitor the DP Aux Channel for link training and MST negotiations, HDCP transactions and EDID exchanges between the M41d and a connected display. The ACA logs these events and assigns precise timestamps to them. You can view the details of each transaction. These ACA logs can be saved and disseminated for further analysis by colleagues and other subject matter experts.

Aux Channel Analyzer – Link Training
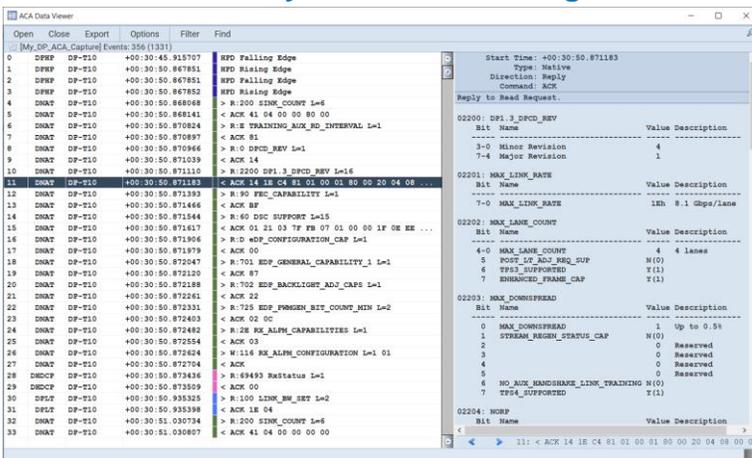
EDID Decode View
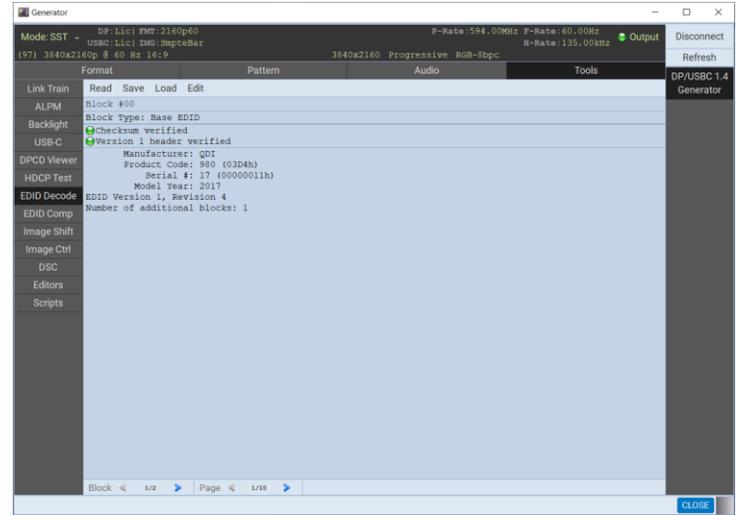
## DPCD Register View
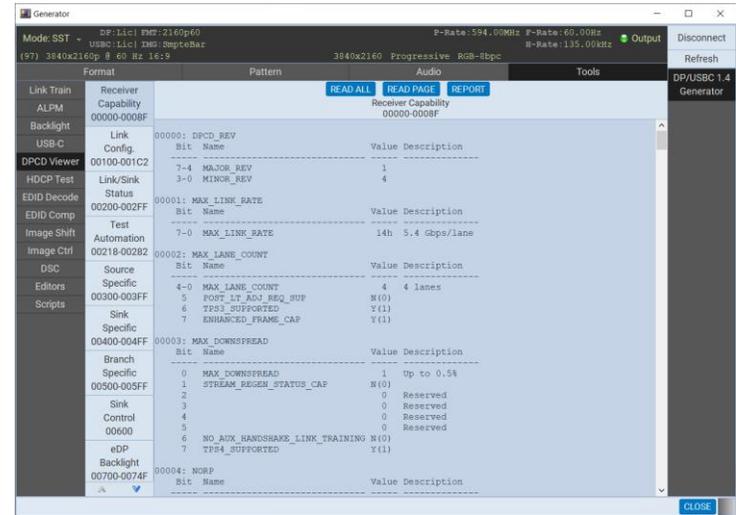
HDCP 2.2 Test
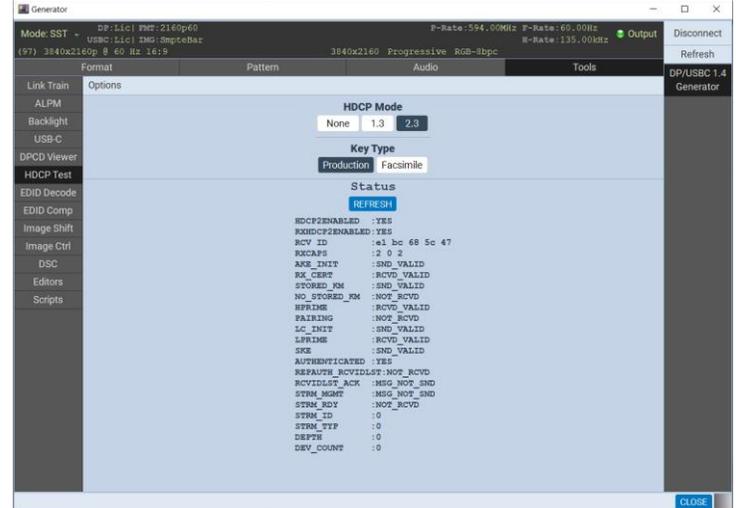
SOURCE TESTS – CAPTURE & DECODE FOR DEEP ANALYSIS

Capture and Decode

The M41d captures and decodes the main link attributes in order to diagnose interoperability issues related to them. The Protocol Analyzer captures & stores main link data and provides visibility into main stream attributes, second-ary data elements, K-Characters and protocol errors. The Protocol Analyzer presents these elements on a graphical timeline and in a table. You can search for data and select any transaction in the table to view its details. The capture utility also enables you to capture specific MST streams from the source.

Capture and Decode (Filter View showing only Audio Packets)

Source Test Setup
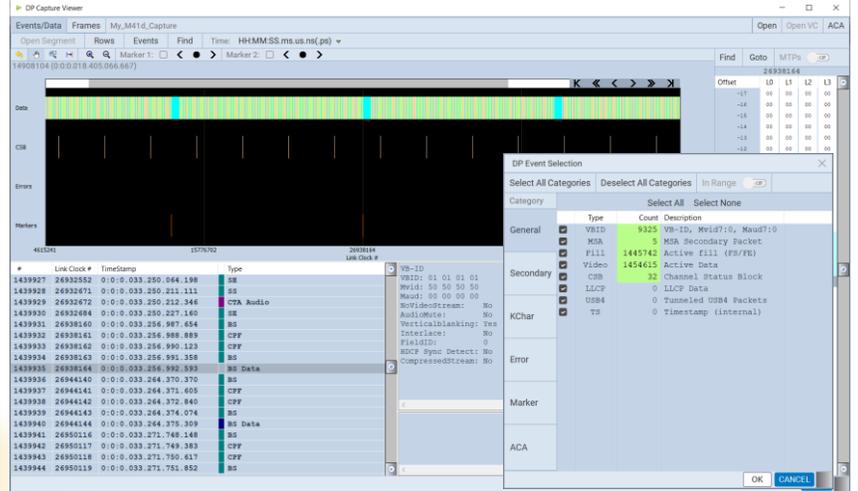
DP Alt Mode Negotiation

The M41d's USB-C Rx connector participates in discovery, power contract negotiation, and DP Alt Mode negotiation. The protocol messages can be monitored on the Auxiliary Channel Analyzer.
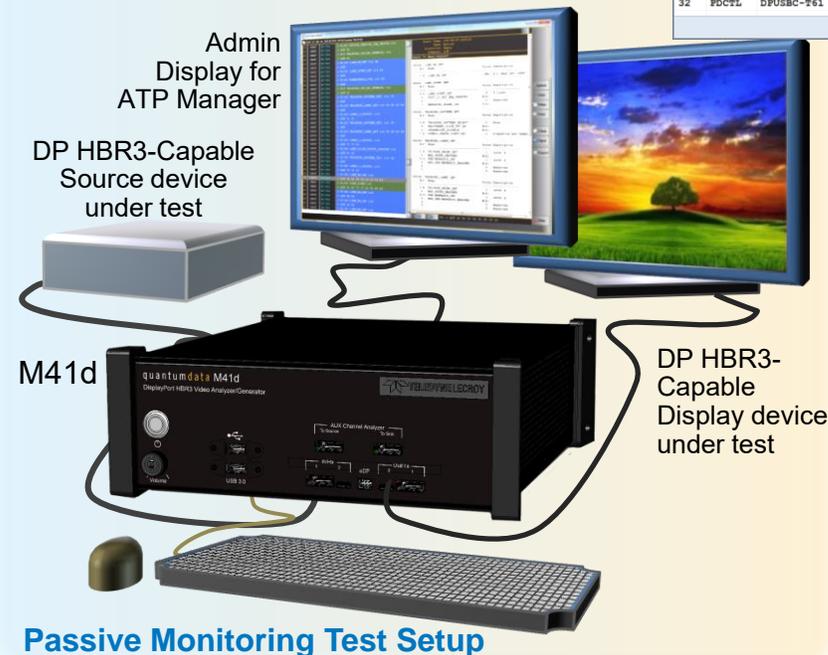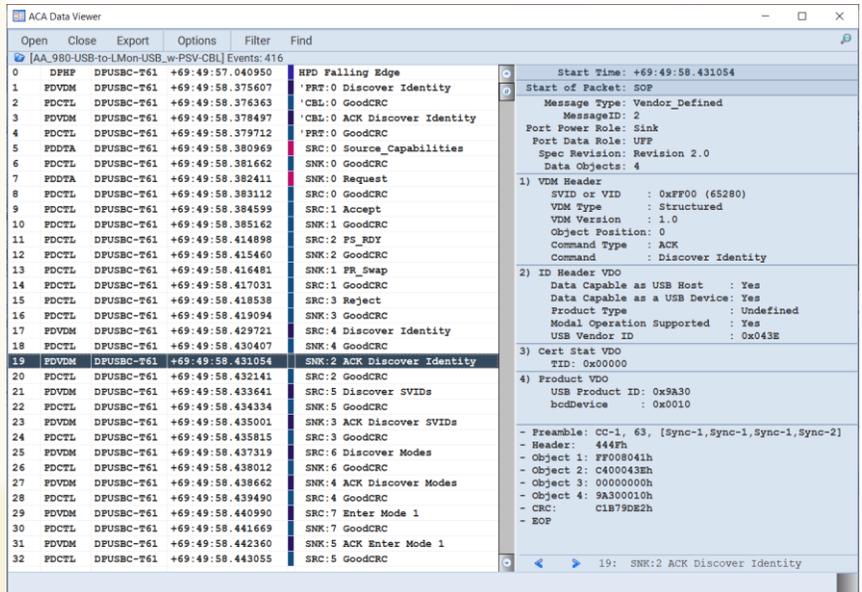
(Passive) Auxiliary Channel Analyzer

The M41d 's Adjunct Auxiliary Channel Analyzer board enables you to monitor the DP Aux Channel for link training and MST negotiations, HDCP trans-actions and EDID exchanges between a DisplayPort source and display device. This enables developers to investigate interoperability problems between DP devices involving link training, HDCP and EDID. Solution is provided using a custom cable (provided).. The ACA logs these events and assigns precise timestamps to them. You can view the details of each transaction.

Passive Monitoring Test Setup

Analyzer

The M41d 's Analyzer enables you to view the incoming video, link rate, timing, colorimetry and various other metadata at a glance. The Analyzer provides a basic confidence test to verify that the incoming video is essentially correct. The Rx port emulates any EDID to test a source devices handling of various EDIDs. You can also configure DPCD registers for emulating on the DP Rx port using the DPCD Editor (below).

Admin Display for ATP Manager

DP HBR3-Capable Source device under test

M41d

Source Test Setup

Real Time Analysis

Aux Channel Analyzer (ACA)

The M41d 's Auxiliary Channel Analyzer (ACA) feature enables you to monitor the DP Aux Channel for link training, MST negotiations, HDCP transactions and EDID exchanges between the M41d Rx port and a source device. The ACA logs the events and assigns precise timestamps to them. You can view the details of each transaction. These ACA logs can be saved and disseminated for further analysis by colleagues and other subject matter experts.

Auxiliary Channel Analyzer Showing Link Training
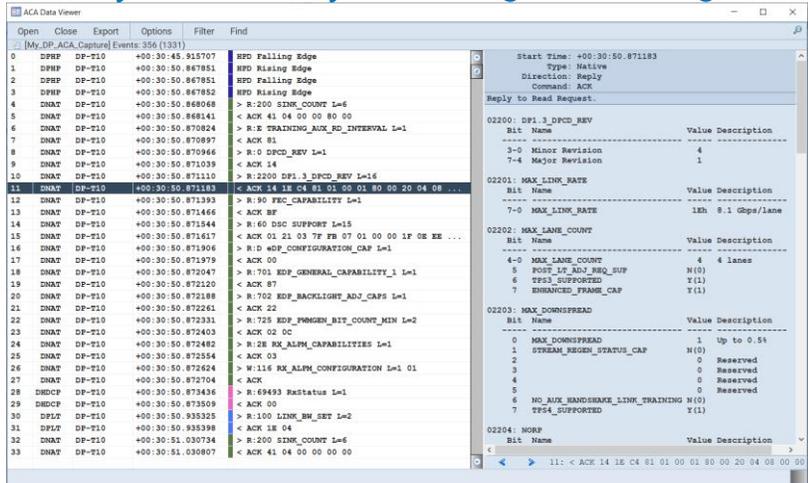
DPCD Editor
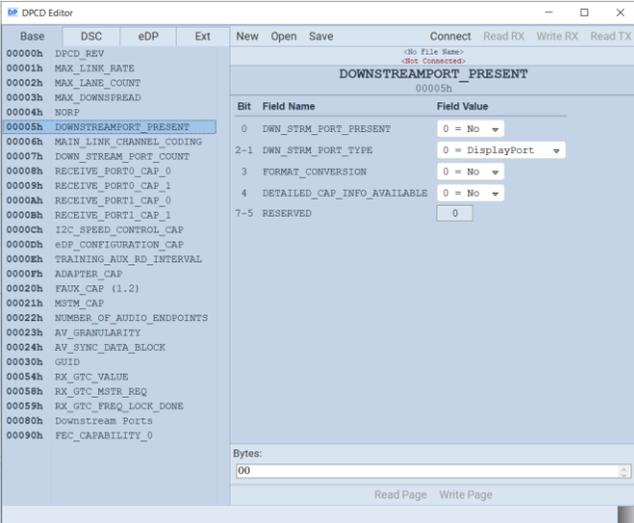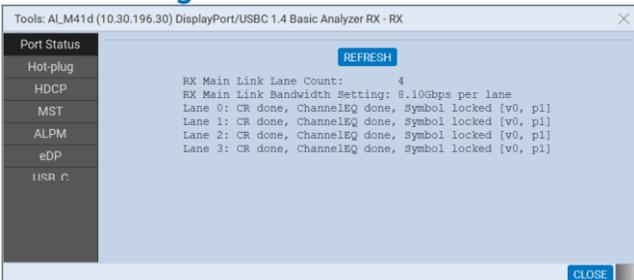
Pixel Error Test for Cables and Distribution Devices

The M41d support a Pixel Error test (or a Pseudo-Random Noise tests for verifying cables and distribution equipment, The test is run in a loopback configuration (not shown).

Link Training Status
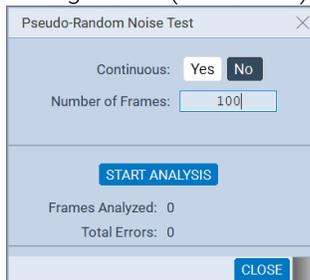
DISPLAY STREAM COMPRESSION (DSC) SOURCE

DSC Analysis

The M41d 's DSC analysis feature enables developers to view the DisplayPort DSC related protocol elements such as the picture parameter set, end of chunk packets and compression flag settings in the VBID to ensure that these elements are occurring in the video stream and that they are occurring in the proper sequence. The DSC analysis feature also captures and decompresses the video frames enabling developers to examine them for compression artifacts. The Forward Error Correction (FEC) transport mechanism, which ensures reliable, error free video transport, can also be verified.

Admin Display for ATP Manager

DP HBR3-Capable Source device under test

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Source Test Setup

DSC Source Compliance Tests

DSC Analysis showing Picture Parameter Set (PPS)

DSC Source Compliance

The DSC source compliance tests are ideal for pre-testing your DisplayPort source product prior to submission to an Authorized Test Center for approval. Pre-testing provides assurance that your product will pass at the ATC when submitted. The compliance tests enable you to view the auxiliary channel analyzer traces logged during the test to help diagnose the cause of compliance test failures.

DSC Source Tests - Test Results

DISPLAY STREAM COMPRESSION (DSC) SINK TESTING

Video Generation (DSC/FEC)

The M41d's DSC/FEC video generator enables display developers to transmit DSC/FEC streams. Users can select from several test patterns and configure the colorimetry, bits per component, bits per pixel, line buffer bit depth and DSC slice configurations.

DSC / FEC Video Generation
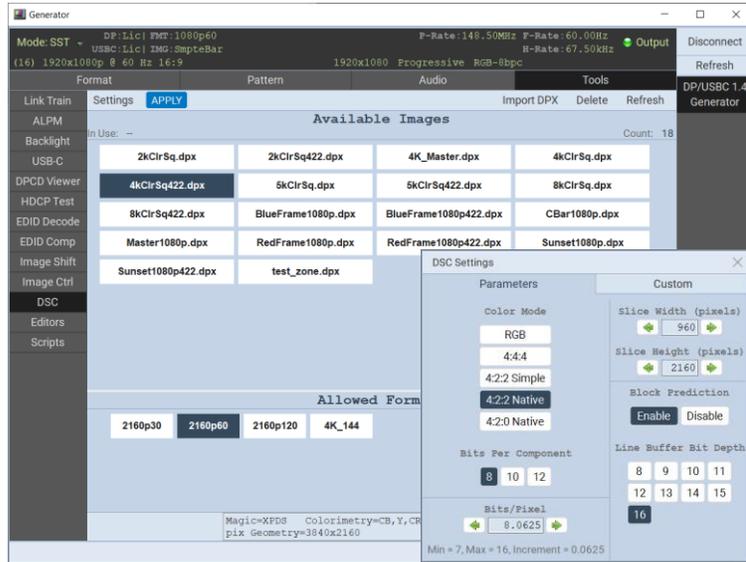
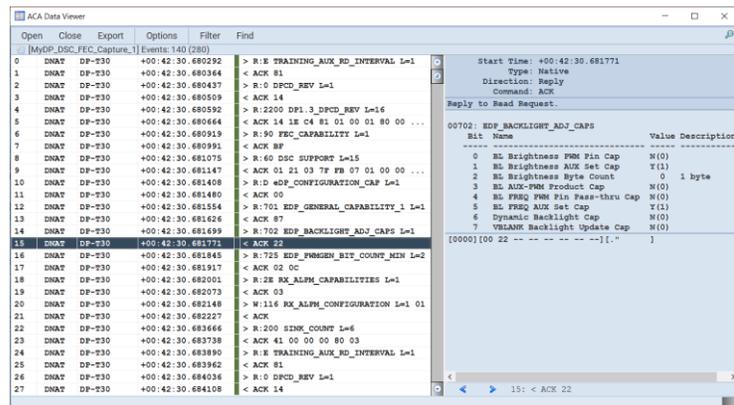**DisplayPort HBR3-Capable Display device under test**

Host PC for ATP Manager

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Display (Sink) Test Setup

ACA showing DPCD reads for DSC capabilities

DSC Sink Compliance

The DSC sink compliance tests are ideal for pre-testing your DisplayPort sink product prior to submission to an Authorized Test Center for approval. Pre-testing provides assurance that your product will pass at the ATC when submitted. The compliance tests enable you to view the auxiliary channel analyzer traces logged during the test to help diagnose the cause of compliance test failures.

DSC Sink Tests

DSC Sink Tests – Test Results
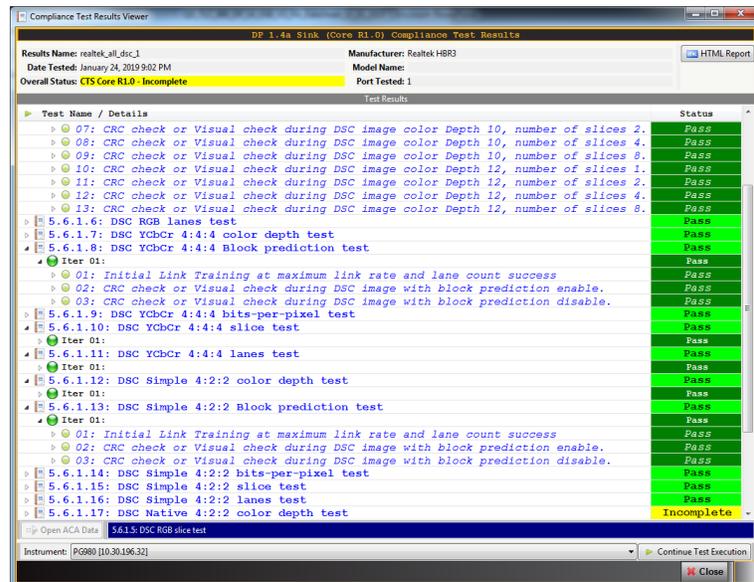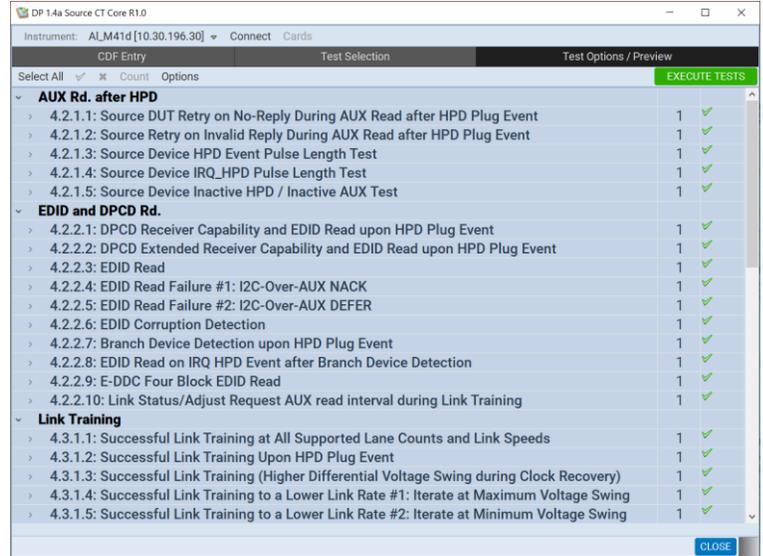

ACA DPCD Reads for DSC Capabilities

The M41d 's ACA utility provides a log of the Aux Channel transactions. The link training can be viewed as well as the DPCD register reads and writes involved in the setup and maintenance of Display Stream Compression (DSC) and Forward Error Correction (FEC).

DP 1.4 LINK LAYER SOURCE COMPLIANCE

Source Link Layer Compliance

The DP source HBR3 link layer compliance are ideal for self-testing or pre-testing your HBR3-capable DisplayPort 1.4 source product prior to submission to an Authorized Test Center for approval. Pre-testing provides added assurance that your product will pass at the ATC when submitted. The compliance tests (below right) enable you to view the captured data and detailed test results which help pinpoint the cause of compliance test failures. The link layer compliance test suite now includes tests for forward error correction (FEC). You can link to the aux channel traces in the Aux Channel Analyzer (ACA) to view the root cause of failures (below).

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DP HBR3-Capable Source device under test

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Source Test Setup

DP 1.4 Source Link Layer Compliance - Test Selection

DP 1.4 Source Link Layer Compliance Test

DP Aux Channel Traces – From LLC Test

DP 1.4 LINK LAYER SOURCE COMPLIANCE

Source Link Layer Compliance

The DP source HBR3 link layer compliance are ideal for self-testing or pre-testing your HBR3-capable DisplayPort 1.4 source product prior to submission to an Authorized Test Center for approval. Pre-testing provides added assurance that your product will pass at the ATC when submitted. The compliance tests (below right) enable you to view the captured data and detailed test results which help pinpoint the cause of compliance test failures. The link layer compliance test suite now includes tests for forward error correction (FEC). You can link to the aux channel traces in the Aux Channel Analyzer (ACA) to view the root cause of failures (below).

Admin Display for ATP Manager

DP HBR3-Capable Source device under test

M41d

Source Test Setup

DP 1.4 Source Link Layer Compliance - Test Selection

DP 1.4 Source Link Layer Compliance Test

DP Aux Channel Traces – From LLC Test

HDCP 2.2 SOURCE, SINK & REPEATER COMPLIANCE

HDCP 2.3 Compliance

The HDCP 2.3 compliance tests are ideal for pre-testing or self-testing your DisplayPort source, sink or repeater product prior to submission to an Authorized Test Center for approval. Pre-testing provides assurance that your product will pass at the ATC when submitted. The compliance tests enable you to view the auxiliary channel analyzer traces logged (not shown) during the test to help diagnose the cause of compliance test failures.
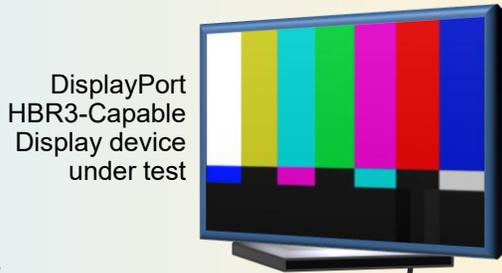
DisplayPort HBR3-Capable Display device under test

Host PC for ATP Manager

M41d

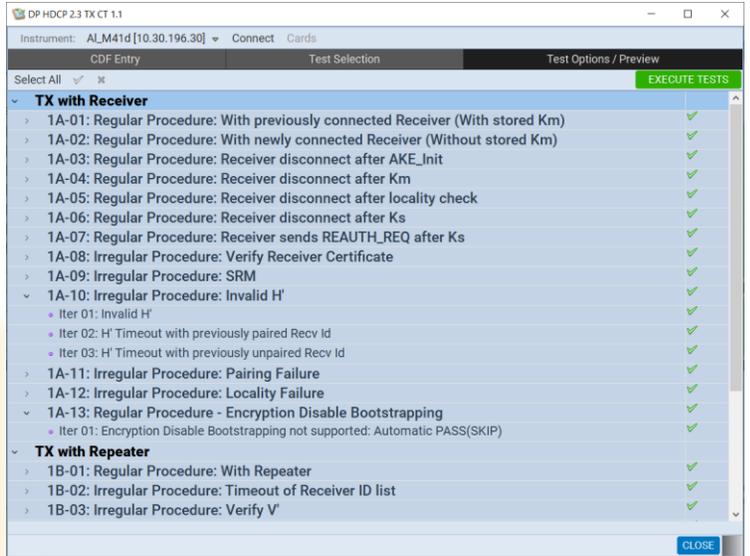**Display (Sink) Test Setup**

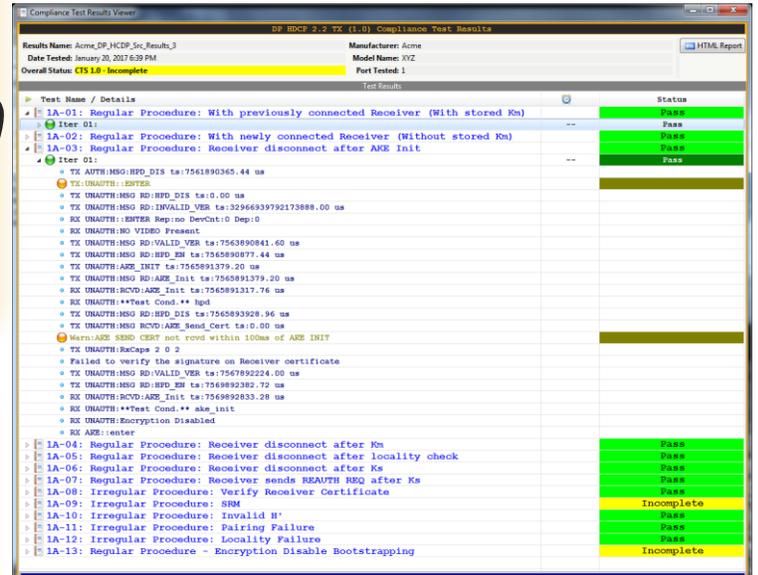Admin Display for ATP Manager

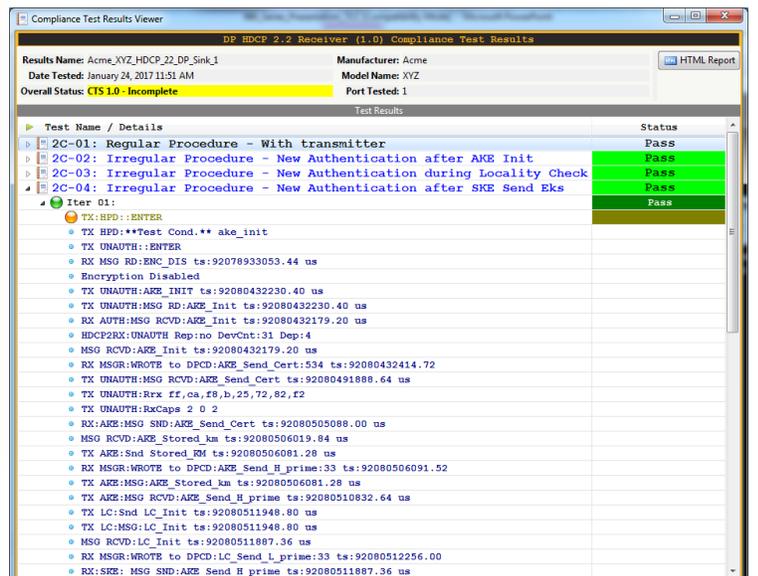DP HBR3-Capable Source device under test

M41d

Source Test Setup

HDCP 2.3 Source Tests - Test Selection
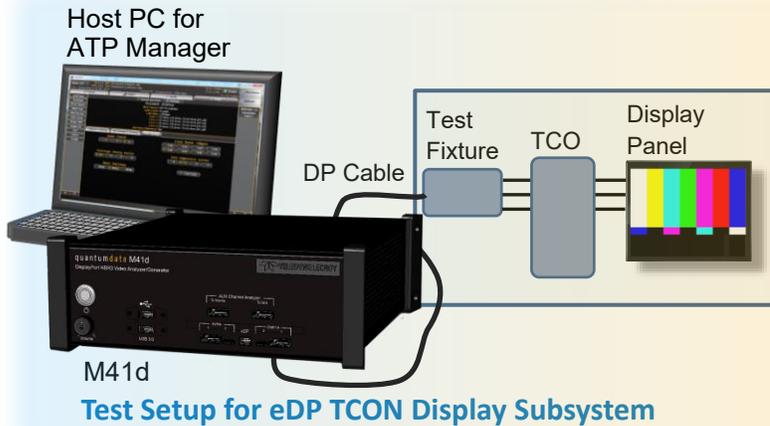

HDCP 2.3 Source Tests - Test Results
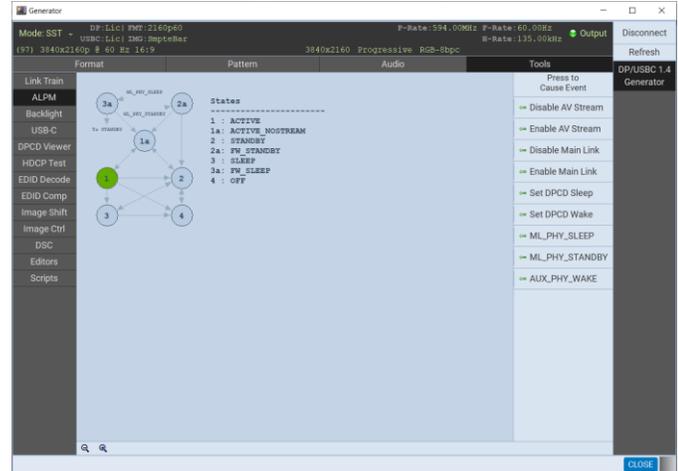

HDCP 2.3 Sink Tests – Test Results

Embedded DisplayPort eDP - ALPM

The M41d supports testing of both eDP source and display sub-systems. A standard DP connection from the M41d to a test fixture is required to enable connection to the eDP subsystem. For display panel TCON testing, once the connection is made, you can use the Advanced Link Power Management (ALPM) feature to test the display's ALPM function (right) and run any other video tests using the M41d's Video Generation function. For eDP source subsystem testing, you can monitor the link training and ALPM state and run captures for analysis, etc. The test setups are depicted below.

Test Setup for eDP TCON Display Subsystem

Test Setup for testing eDP source Subsystem

eDP Fast Link Training

The M41d supports fast link training acting either as an eDP source subsystem or an eDP display subsystem. The module emulates the necessary Fast Link training DPCD registers When testing a display you can select the Lane Count, Link rate (including "intermediate "eDP lane rates), Voltage Swing, Pre-Emphasis and Training Test Pattern. You can monitor the Aux Channel transactions with the Aux Channel Analyzer utility. (eDP Fast Link Training Source test not shown.)

eDP Tx Backlight Control

The M41d supports testing of the eDP backlight control function on eDP TCON display subsystems. Backlight control is supported through the Aux Channel and the backlight control lead. The connection is made through the module's eDP header pins on the faceplate. You can select between High and Low backlight enable, set the PWM duty cycle, pre-scaling and PWM generator divider.
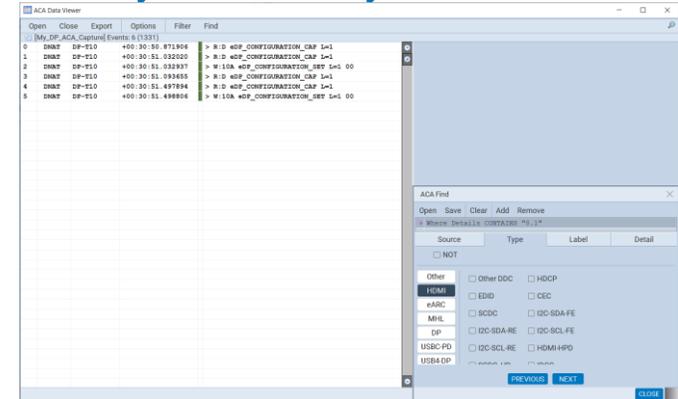
Advanced Link Power Management (ALPM)
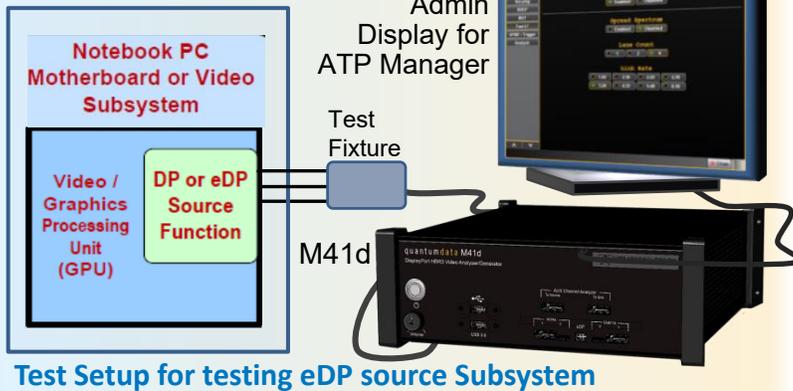

Link Training Control and Configuration

Auxiliary Channel Analyzer – Fast Link Train

eDP Tx Backlight Control

SPECIFICATIONS

DisplayPort 1.4 / USB-C/ eDP Capabilities

Version	DisplayPort 1.4a
Standard Formats	VESA, CTA
Video Data Rates	1.62, 2.7, 5.4, 8.1 Gb/s Link rates 1, 2, 4 Lanes
Color Depths	8, 10, 12, 16 bits
Video Encoding	RGB, YCbCr
Video Sampling Modes	4:4:4, 4:2:2, 4:2:0
HDCP	Versions 2.2 & (1.3 on 1 & 2 lanes only)
Audio	8 Channel LPCM programmable sine wave
Capture memory	8 GBytes

Connectors - Front

DP Full-Size	Tx (1) DP Full-size; Rx (1) DP Full-size
USB-C	Tx (1) USB-C with DP Alt Mode; Rx (1) USB-C with DP Alt Mode
Aux Chan Adjunct Board	Tx (1) DP Full-size; Rx (1) DP Full-size
eDP Header	Pins to access eDP Tx backlight controls
USB (2)	For connecting keyboard and mouse for ATP Manager control

Connectors - Back

HDMI - Admin Connector	HDMI Port for ATP Manager
USB (2); USB-C (2)	Keyboard / mouse connected to USB ports; External 4K UHDTV at Admin HDMI port
RJ45 E1	For admin control over LAN from computer running ATP Manager
All other connectors	Not used

Physical / Electrical / Admin

Power	100-240 VAC, 50-60 Hz, 200 Watts
Weight	11.15 LBS; 5.057 Kg
Size	Height: 3.44 in. (8.74 cm) Width: 9.57 in. (24.30 cm) Depth: 10.94 in. (27.79 cm)
Rack mountable	2 RU mounts in 19 inch rack with rack mounting brackets (provided)
Internal speaker	Speaker with volume control for monitoring incoming audio
Command Line Control	Ethernet (RJ-45) for external GUI and telnet
GUI Control	Either through External PC connected over LAN to Ethernet RJ45 or:
	Keyboard / mouse connected to USB ports; External 4K UHDTV at Admin HDMI port
Environmental	Operating Temp: 32 to 104 (F); 0 to 40 (C)

Ordering - Product Code

Product Code	Description
00-00260	M41d hardware and base functional unit – Entry Level with full sized DP connectors activated
95-00209	M41x rack-mount kit
95-00211	USB-C Port activation for DP Alt Mode function
95-00219	Source enhanced functional test – Includes Capture Analysis, Passive Monitoring, DSC Source Analysis
95-00220	Sink enhanced functional test - Includes Passive Monitoring, DSC Sink Analysis
95-00213	Source Link Layer compliance (requires 95-00219)
95-00216	Sink Link Layer compliance (requires 95-00220)
95-00227	Sink EDID compliance (requires 95-00220)
95-00215	DSC/FEC Source functional test (requires 95-00219)
95-00218	DSC/FEC Sink functional test (requires 95-00220)
95-00214	HDCP 2.2 Source compliance (requires 95-00213)
95-00217	HDCP 2.2 Sink compliance (requires 95-00218)
95-00212	Embedded DisplayPort (eDP)

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