Accurate Burst Separation
Read and Write bursts can be separated based on DQ-DQS phase or based on the command bus when used in conjunction with the HDA125 High-speed Digital Analyzer. The HDA125 enables bursts to be separated using the commands sent from the controller, allowing for accurate burst separation even in situations with non-ideal signal integrity, such as reflections.

Measurement Confidence
Due to the high level of variability in DDR measurements, it is important to make statistically relevant measurements to fully characterize DDR4 and LPDDR4/4X interfaces. By measuring thousands of cycles in one acquisition, the user can be more confident that they are catching the true maximum and minimum points for their measurement.

Best-In-Class Debug Toolkit
QPHY-DDR4 uses the DDR Debug Toolkit to perform all compliance testing. Using the “Stop on Test” feature, the user can pause testing after each individual test and clearly see where the worst case measurement occurred. At that point the DDR Debug toolkit can be leveraged for further debug and upon completion, testing can be seamlessly resumed with one click of a button.

De-embedding and Virtual Probing
Teledyne LeCroy provides software tools which can be used to maximize signal integrity with DDR probing. The VirtualProbe package can virtually move the probe to the DRAM BGA, where it cannot be physical placed, and it will remove any effects of the probe or interposers through de-embedding. The VP@Rcvr (Virtual Probe at Receiver) math function can be used to model the circuit of the DIMM to reduce reflections.

Key Features
- Complete DDR4 and LPDDR4/4X test coverage as described by JESD79-4D, JESD209-4D and JESD209-4-1A
- Support for all standard and custom speed grades
- Separate bursts using DQ-DQS phase or command bus
- Statistically relevant results achieve measurement confidence
- Report generation with pass/fail results and fully annotated worst case measurement screenshot
- DDR Debug Toolkit integration for easy and flexible debug
- Maximize signal integrity with Interposer de-embedding and Virtual Probing
**DQ Input Receiver Compliance Mask** — The DDR4 and LPDDR4/4X specifications include a compliance mask for the DQ input signal which replaces the traditional DQ setup and hold time measurements. QPHY-DDR4 automatically centers the mask in the DQ eye to test for any mask hits and reports the required shift from the DQS crossing to test tDQS2DQ. This eye diagram is also used to calculate the VIHL_AC peak to peak requirement.

**Clock Tests** — The DDR4 specification requires clock jitter to be separated into random and deterministic components, which is a first for DDR specifications. QPHY-DDR4 leverages industry leading serial data algorithms to perform the jitter breakdown for tJIT(per). In addition to these tests, QPHY-DDR4 will test average clock period, absolute clock period, average high/low pulse width, absolute high/low pulse width, cycle-cycle jitter, duty cycle jitter, and cumulative error over n period tests.

**Timing Tests** — tDQSQ verifies the skew between DQS and the associated DQ within a read burst. QPHY-DDR4 will perform this measurement on every DQ transition within a read burst. Upon completion each test will display a fully annotated “worst case measurement” screenshot which includes trace labels for the signals under test and relevant voltage levels.

**Electrical Tests** — SRI diff, the DDR4/LPDDR4/4X definition for input slew rate on DQS, measures the slew rate on every rising and falling edge within a write burst. QPHY-DDR4 will measure every transition within each write burst in the acquisition providing statistically meaningful results in a short period of time. In this case over 3,000 slew rate measurements were performed which ensures that the true maximum and minimum points have been caught without requiring multiple acquisitions.
QualiPHY is designed to reduce the time, effort, and specialized knowledge needed to perform compliance testing on high-speed serial buses.

- Guides the user through each test setup
- Performs each measurement in accordance with the relevant JEDEC specified test procedure
- Compares each measured value with the applicable specification limits
- Saves documented Pass/Fail PDF Reports
- QualiPHY helps the user perform testing the right way—every time!

QualiPHY has many preset compliance configurations but also enables users to create their own configuration and limit sets.

Connection Diagrams prompt the user to make the necessary connections.

Compliance Reports contain all of the tested values, the specific test limits and screen captures. Compliance Reports can be created as HTML, PDF or XML.
**DDR4 & LPDDR4 Test Coverage**

### Clock Tests
- tCK(avg) Average Clock Period
- tCH(avg) Average High Pulse Width
- tCL(avg) Average Low Pulse Width
- tCK(abs) Absolute Clock Period
- tCH(abs) Absolute Clock High Pulse Width
- tCL(abs) Absolute Clock Low Pulse Width
- tJIT(per)_total * Clock Period Jitter - Total
- tJIT(per)_dj Cycle to Cycle Period Jitter
- tJIT(duty) * Duty Cycle Jitter
- tERR(nper) * Cumulative Error

### Timing Tests
- tDIPW DQ Input Pulse Width
- tCIPW † CA/CS Input Pulse Width
- tQH DQ Output Hold Time from DQS
- tDQSQ DQS to DQ Skew
- tDQSCK DQS Output Rising Edge from Clock Rising Edge
- tDQSS * DQS Input Rising Edge to Clock Rising Edge
- tDSS DQS Falling Edge to CK Setup Time
- tDQSH DQS Falling Edge Hold Time from CK
- tDQSL DQS Input High Pulse Width
- tDIQL DQS Input Low Pulse Width
- tQSL DQS Output High Pulse Width
- tQSL DQS Output Low Pulse Width
- tHZ(QQS)/tHZ(QQ) * DQS & DQ High Impedance Time from CK
- tLZ(QQS)/tLZ(QQ) * DQS & DQ High Impedance Time from CK
- tRPRE Read Preamble Pulse Width
- tRPST Read Postamble Pulse Width
- tWPRE Write Preamble Pulse Width
- tWPST Write Postamble Pulse Width
- tIS * ADD/CTRL Input Setup Time
- tIH * ADD/CTRL Input Hold Time

### Electrical Tests
- tDVAC * Allowed Time Before Ringback
- srr1, srr2 * Rising Input Slew Rate
- srfl, srfl2 * Falling Input Slew Rate
- SRIdiff Differential Input Slew Rate
- SRQse Single-ended Output Slew Rate
- SRQdiff Differential Output Slew Rate
- VIX * Differential Input Cross Point Voltage
- VSEL * Single-ended Low Level
- VSEH * Single-ended High Level
- Vindiff, VIHdiff, VILdiff, VINSE † Amplitude and Levels

### Eye Diagram Tests
- Eye Diagram of Data and Strobe on Read Burst
- Eye Diagram of Data and Strobe on Write Burst

### Ordering Information

**Debug and Compliance (All DDR4/LPDDR4/4X Speeds)**

- Oscilloscope: WaveMaster (SDA 813 Zi-B 13 GHz)
- Probe Tips: 3-4x DH13-PL (13 GHz)
- Interposers**: Nexus or EyeKnowHow
- Decode, Trigger, R/W Separation using Logic Analysis**: HDA125 (Logic Analysis)
- Software: WM821-VIRTUALPROBE** (De-embedding), WM821-DDR4-TOOLKIT (Debug), OPHY-DDR4 (Automated Compliance)

**Recommended Equipment & Options**

- Oscilloscope: WavePro (404HD 4 GHz) or WaveMaster (808 Zi-B 8 GHz)
- Probe Tips: 3-4x DH08-PB2 (8 GHz)
- Interposers**: Nexus or EyeKnowHow
- Software: Wxxxx-DDR4-TOOLKIT (Debug)

**Testing, Training Labs, and Consulting Services**

- DDR4 PHY Testing and Training: Teledyne LeCroy Austin Labs
- Europe Memory Design Consulting: EyeKnowHow

---

© 2023 by Teledyne LeCroy, Inc. All rights reserved. Specifications, prices, availability, and delivery subject to change without notice. Product or brand names are trademarks or requested trademarks of their respective holders.