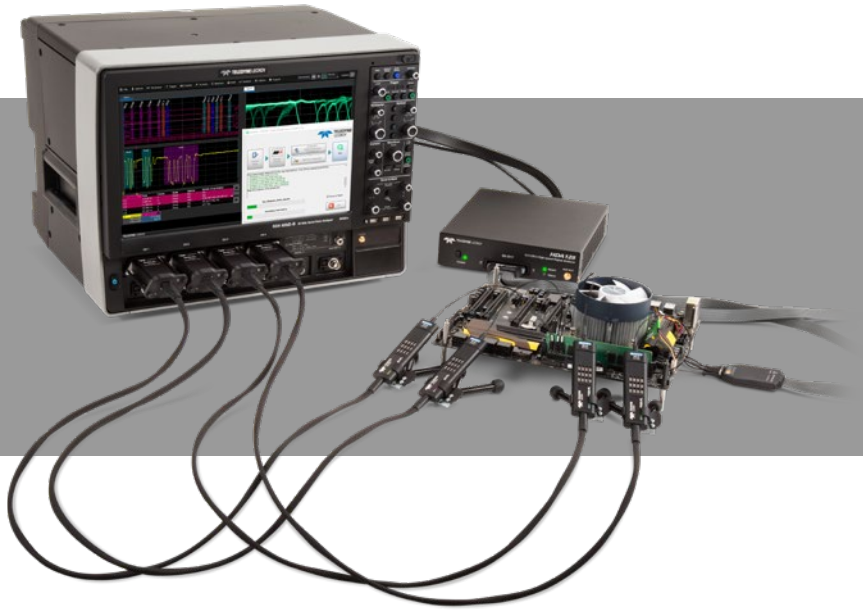
TELEDYNE LECROY
Everywhereyoulook™

Automated DDR4 & LPDDR4/4X Compliance Testing

QPHY-DDR4



Key Features

Complete DDR4 and LPDDR4/4X test coverage as described by JESD79-4D, JESD209-4D and JESD209-4-1A

Support for all standard and custom speed grades

Separate bursts using DQ-DQS phase or command bus

Statistically relevant results achieve measurement confidence

Report generation with pass/fail results and fully annotated worst case measurement screenshot

DDR Debug Toolkit integration for easy and flexible debug

Maximize signal integrity with Interposer de-embedding and Virtual Probing

Accurate Burst Separation

Read and Write bursts can be separated based on DQ-DQS phase or based on the command bus when used in conjunction with the HDA125 High-speed Digital Analyzer. The HDA125 enables bursts to be separated using the commands sent from the controller, allowing for accurate burst separation even in situations with non-ideal signal integrity, such as reflections.

Best-In-Class Debug Toolkit

QPHY-DDR4 uses the DDR Debug Toolkit to perform all compliance testing. Using the "Stop on Test" feature, the user can pause testing after each individual test and clearly see where the worst case measurement occurred. At that point the DDR Debug toolkit can be leveraged for further debug and upon completion, testing can be seamlessly resumed with one click of a button.

Measurement Confidence

Due to the high level of variability in DDR measurements, it is important to make statistically relevant measurements to fully characterize DDR4 and LPDDR4/4X interfaces. By measuring thousands of cycles in one acquisition, the user can be more confident that they are catching the true maximum and minimum points for their measurement.

De-embedding and Virtual Probing

Teledyne LeCroy provides software tools which can be used to maximize signal integrity with DDR probing. The VirtualProbe package can virtually move the probe to the DRAM BGA, where it cannot be physical placed, and it will remove any effects of the probe or interposers through de-embedding. The VP@Rcvr (Virtual Probe at Receiver) math function can be used to model the circuit of the DIMM to reduce reflections.

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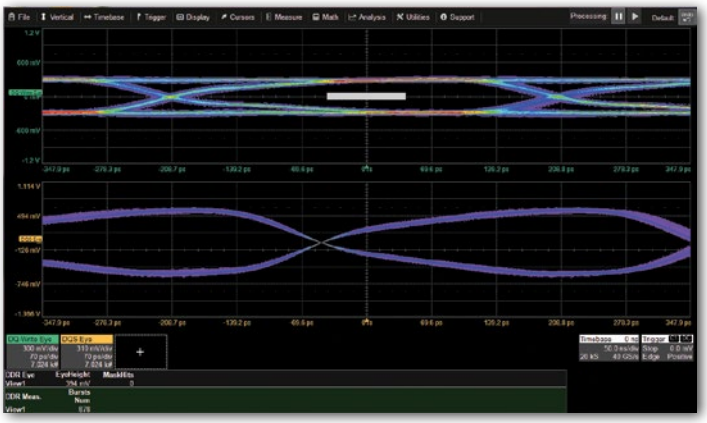
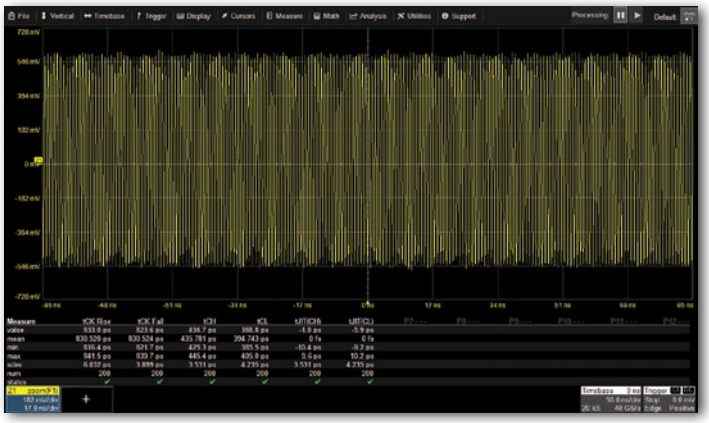
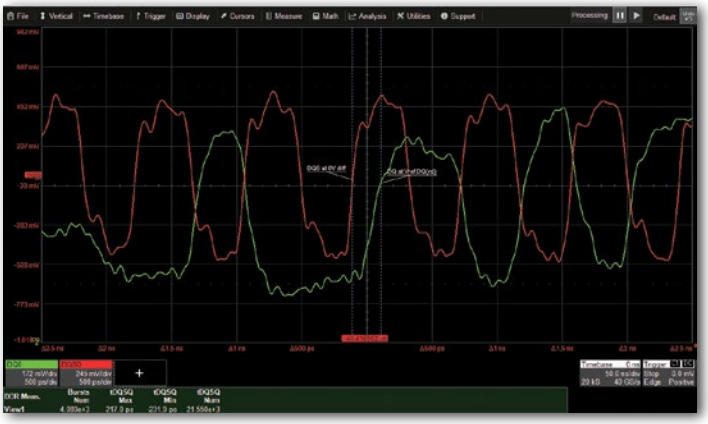
COMPREHENSIVE DDR4 AND LPDDR4/4X TEST COVERAGE



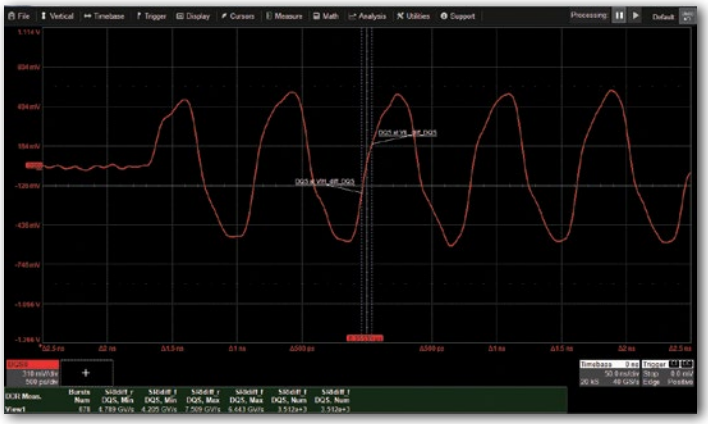
DQ Input Receiver Compliance Mask — The DDR4 and LPDDR4/4X specifications include a compliance mask for the DQ input signal which replaces the traditional DQ setup and hold time measurements. QPHY-DDR4 automatically centers the mask in the DQ eye to test for any mask hits and reports the required shift from the DQS crossing to test tDQS2DQ. This eye diagram is also used to calculate the VIHL_AC peak to peak requirement.



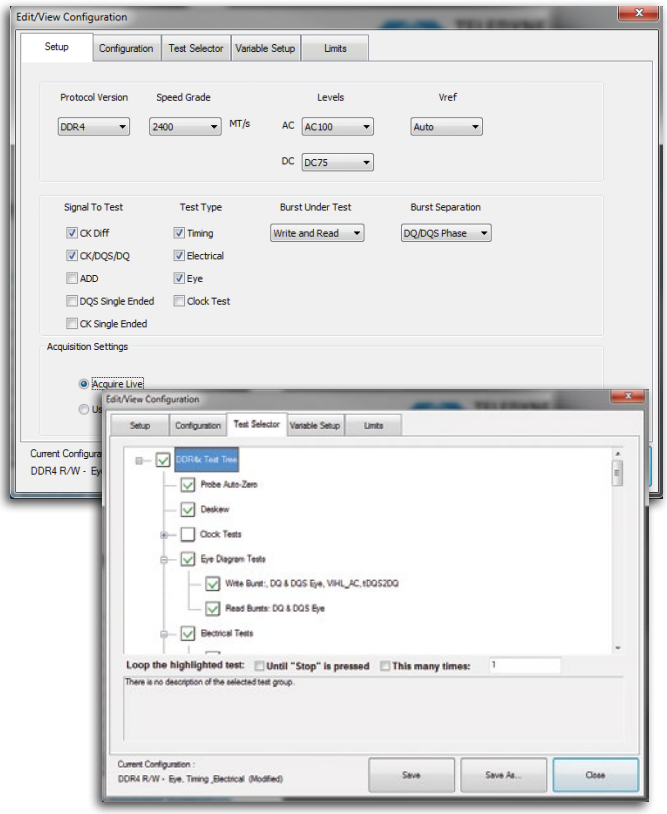
Clock Tests — The DDR4 specification requires clock jitter to be separated into random and deterministic components, which is a first for DDR specifications. QPHY-DDR4 leverages industry leading serial data algorithms to perform the jitter breakdown for tJIT(per). In addition to these tests, QPHY-DDR4 will test average clock period, absolute clock period, average high/low pulse width, absolute high/low pulse width, cycle-cycle jitter, duty cycle jitter, and cumulative error over n period tests.



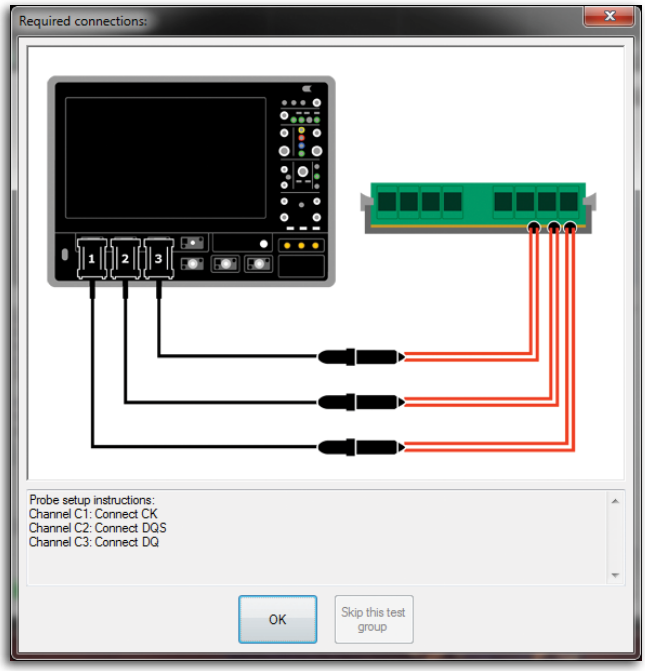
Timing Tests — tDQSQ verifies the skew between DQS and the associated DQ within a read burst. QPHY-DDR4 will perform this measurement on every DQ transition within a read burst. Upon completion each test will display a fully annotated “worst case measurement” screenshot which includes trace labels for the signals under test and relevant voltage levels.



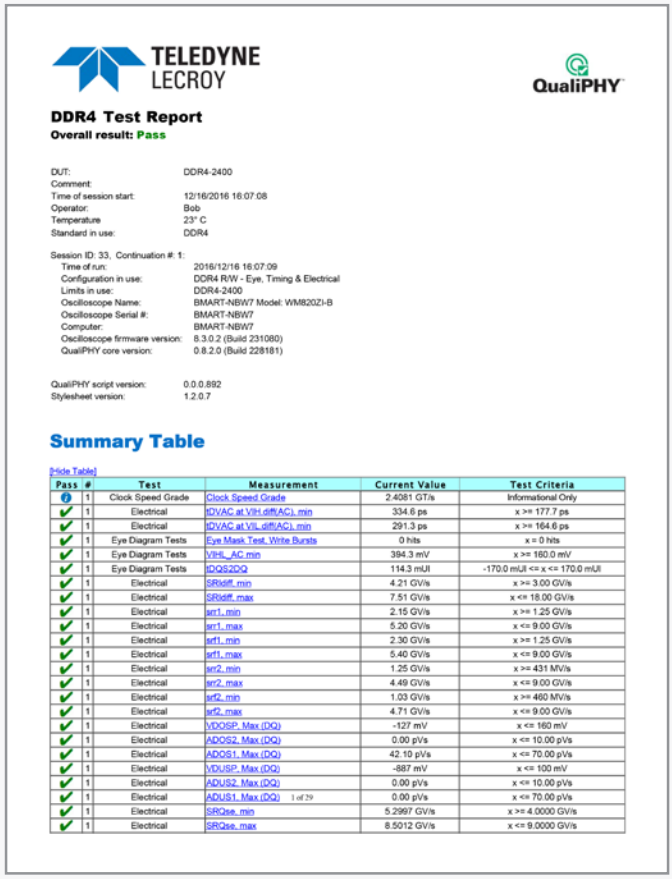
Electrical Tests — SRI diff, the DDR4/LPDDR4/4X definition for input slew rate on DQS, measures the slew rate on every rising and falling edge within a write burst. QPHY-DDR4 will measure every transition within each write burst in the acquisition providing statistically meaningful results in a short period of time. In this case over 3,000 slew rate measurements were performed which ensures that the true maximum and minimum points have been caught without requiring multiple acquisitions.



QualiPHY has many preset compliance configurations but also enables users to create their own configuration and limit sets.



Connection Diagrams prompt the user to make the necessary connections.



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DDR4 Test Report

Overall result: Pass

DUT: DDR4-2400
Comment:
Time of session start: 12/16/2016 16:07:08
Operator: Bob
Temperature 23° C
Standard in use: DDR4

Session ID: 33, Continuation #: 1:
Time of run: 2016/12/16 16:07:09
Configuration in use: DDR4 R/W - Eye, Timing & Electrical
Limits in use: DDR4-2400
Oscilloscope Name: BMART-NBW7 Model: WM820ZI-B
Oscilloscope Serial #: BMART-NBW7
Computer: BMART-NBW7
Oscilloscope firmware version: 8.3.0.2 (Build 231080)
QualiPHY core version: 0.8.2.0 (Build 228181)

QualiPHY script version: 0.0.0.892
Stylesheet version: 1.2.0.7

Summary Table

[Hide Table]

Pass	#	Test	Measurement	Current Value	Test Criteria
ℹ	1	Clock Speed Grade	Clock Speed Grade	2.4081 GT/s	Informational Only
✔	1	Electrical	tDVAC at VIH.diff(AC), min	334.6 ps	x >= 177.7 ps
✔	1	Electrical	tDVAC at VIL.diff(AC), min	291.3 ps	x >= 164.6 ps
✔	1	Eye Diagram Tests	Eye Mask Test, Write Bursts	0 hits	x = 0 hits
✔	1	Eye Diagram Tests	VIHL_AC min	394.3 mV	x >= 160.0 mV
✔	1	Eye Diagram Tests	tDQS2DQ	114.3 mUI	-170.0 mUI <= x <= 170.0 mUI
✔	1	Electrical	SRdiff, min	4.21 GV/s	x >= 3.00 GV/s
✔	1	Electrical	SRdiff, max	7.51 GV/s	x <= 18.00 GV/s
✔	1	Electrical	sr1, min	2.15 GV/s	x >= 1.25 GV/s
✔	1	Electrical	sr1, max	5.20 GV/s	x <= 9.00 GV/s
✔	1	Electrical	sf1, min	2.30 GV/s	x >= 1.25 GV/s
✔	1	Electrical	sf1, max	5.40 GV/s	x <= 9.00 GV/s
✔	1	Electrical	sr2, min	1.25 GV/s	x >= 431 MV/s
✔	1	Electrical	sr2, max	4.49 GV/s	x <= 9.00 GV/s
✔	1	Electrical	sf2, min	1.03 GV/s	x >= 460 MV/s
✔	1	Electrical	sf2, max	4.71 GV/s	x <= 9.00 GV/s
✔	1	Electrical	VDQSP, Max (DQ)	-127 mV	x <= 160 mV
✔	1	Electrical	ADQS2, Max (DQ)	0.00 pV/s	x <= 10.00 pV/s
✔	1	Electrical	ADQS1, Max (DQ)	42.10 pV/s	x <= 70.00 pV/s
✔	1	Electrical	VDUSP, Max (DQ)	-887 mV	x <= 100 mV
✔	1	Electrical	ADUS2, Max (DQ)	0.00 pV/s	x <= 10.00 pV/s
✔	1	Electrical	ADUS1, Max (DQ)	0.00 pV/s	x <= 70.00 pV/s
✔	1	Electrical	SRQse, min	5.2997 GV/s	x >= 4.0000 GV/s
✔	1	Electrical	SRQse, max	8.5012 GV/s	x <= 9.0000 GV/s

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Compliance Reports contain all of the tested values, the specific test limits and screen captures. Compliance Reports can be created as HTML, PDF or XML.

QualiPHY

QualiPHY is designed to reduce the time, effort, and specialized knowledge needed to perform compliance testing on high-speed serial buses.

- Guides the user through each test setup
- Performs each measurement in accordance with the relevant JEDEC specified test procedure
- Compares each measured value with the applicable specification limits
- Saves documented Pass/Fail PDF Reports
- QualiPHY helps the user perform testing the right way—every time!

SPECIFICATIONS AND ORDERING INFORMATION

DDR4 & LPDDR4 Test Coverage

Clock Tests

tCK(avg)	Average Clock Period
tCH(avg)	Average High Pulse Width
tCL(avg)	Average Low Pulse Width
tCK(abs)	Absolute Clock Period
tCH(abs)	Absolute Clock High Pulse Width
tCL(abs)	Absolute Clock Low Pulse Width
tJIT(per)_total *	Clock Period Jitter - Total
tJIT(per)_dj	Clock Period Jitter - Deterministic
tJIT(cc)	Cycle to Cycle Period Jitter
tJIT(duty) *	Duty Cycle Jitter
tERR(nper) *	Cumulative Error

Eye Diagram Tests

Eye Diagram of Data and Strobe on Read Burst	
Eye Diagram of Data and Strobe on Write Burst	
VdIVW	DQ Rx Mask Voltage - pk-pk
TdIVW	DQ Rx Timing Window
VIHL_AC	DQ & CA/CS AC Input Swing pk-pk
tDQS2DQ	Rx Mask DQS to DQ Offset
tQW_total †	Eye Diagram of Command Address
VcIVW †	CA/CS Rx Mask Voltage - pk-pk
tcIVW †	CA/CS Rx Timing Window

Timing Tests

tDIPW	DQ Input Pulse Width
tCIPW †	CA/CS Input Pulse Width
tQH	DQ Output Hold Time from DQS
tDQSQ	DQS to DQ Skew
tDQSCK	DQS Output Rising Edge from Clock Rising Edge
tDQSS *	DQS Input Rising Edge to Clock Rising Edge
tDSS	DQS Falling Edge to CK Setup Time
tDSH	DQS Falling Edge Hold Time from CK
tDQSH	DQS Input High Pulse Width
tDQSL	DQS Input Low Pulse Width
tQSH	DQS Output High Pulse Width
tQSL	DQS Output Low Pulse Width
tHZ(DQS)/ tHZ(DQ) *	DQS & DQ High Impedance Time from CK
tLZ(DQS)/ tLZ(DQ) *	DQS & DQ High Impedance Time from CK
tRPRE	Read Preamble Pulse Width
tRPST	Read Postamble Pulse Width
tWPRE	Write Preamble Pulse Width
tWPST	Write Postamble Pulse Width
tIS *	ADD/CTRL Input Setup Time
tIH *	ADD/CTRL Input Hold Time

Electrical Tests

tDVAC *	Allowed Time Before Ringback
srr1, srr2 *	Rising Input Slew Rate
srf1, srf2 *	Falling Input Slew Rate
SRIdiff	Differential Input Slew Rate
SRQse	Single-ended Output Slew Rate
SRQdiff	Differential Output Slew Rate
VIX *	Differential Input Cross Point Voltage
VSEL *	Single-ended Low Level
VSEH *	Single-ended High Level
Vindiff, VIHdiff, VILdiff Vinse †	Amplitude and Levels
VDOSP, VCOSP, VASOP	Maximum peak amplitude above VDOS
VDUSP, VUS, VAUS	Maximum peak amplitude below VDUS
ADOS1, ACOS1, AAOS1	Maximum overshoot area per 1 UI between VDDQ and VDOS
ADOS2, ACOS2, AAOS2	Maximum overshoot area per 1 UI above VDOS
ADUS1	Maximum undershoot area per 1 UI between VSSQ and VDUS1

† LPDDR4/4X only
** DDR4 only*

Ordering Information

Debug and Compliance (All DDR4/LPDDR4/4X Speeds)	Recommended Equipment & Options
Oscilloscope	WaveMaster (SDA 813 Zi-B 13 GHz)
Probing (CK, DQ, DQS or CA Signals)	3-4x DH13-PL (13 GHz)
Probe Tips	3-4x DH-SI (Solder Tips)
Interposers**	Nexus or EyeKnowHow
Decode, Trigger, R/W Separation using Logic Analysis**	HDA125 (Logic Analysis) HDA-DLS-09QL (tips)
Software	WM8ZI-VIRTUALPROBE** (De-embedding) WM8ZI-DDR4-TOOLKIT (Debug) QPHY-DDR4 (Automated Compliance)

Debug Only (LPDDR4/4X <1200 MT/s)	Recommended Equipment & Options
Oscilloscope	WavePro (404HD 4 GHz) or WaveMaster (808 Zi-B 8 GHz)
Probing (CK, DQ, DQS or CA Signals)	3-4x DH08-PB2 (8 GHz)
Probe Tips	3-4x DH-SI (Solder Tips)
Interposers**	Nexus or EyeKnowHow
Software	Wxxxx-DDR4-TOOLKIT (Debug)

***Optional items, but are highly recommended to improve signal quality and measurement accuracy.*

Testing, Training Labs, and Consulting Services	
DDR4 PHY Testing and Training	Teledyne LeCroy Austin Labs
Europe Memory Design Consulting	EyeKnowHow

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Local sales offices are located throughout the world.
Visit our website to find the most convenient location.