TELEDYNE LECROY
Everywhereyoulook™

Austin Labs Testing and Training

In-Depth PCIe® 6.0 Protocol

(TLC-PCIe_6.0.2023.08)

4 Day Course Outline

Introduction to PCIe

Components and Terminology

PCIe Architecture

PCIe Link Training and Initialization

Alternate Protocol Negotiation

Introducing Flit Mode

PCIe ACK / NAK and Flow Control

PCIe Enumeration and Configuration

Analyzer Operation and Configuration

What to Expect

Never pay extra to look at trace captures

Insight into the standard based on our real world testing experience

Instruction from experts with over 20 years of experience in storage and networking

Investigate the inner workings of the PCIe protocol, an architectural staple in server and storage engineering. *To get the most out of this course, you should already be familiar with at least PCIe 4.0.*

Get concrete, detailed answers to your questions:

- Why is PCIe 6.o so different?
- What are Flits and why are they needed?
- What are the different communication layers for PCIe?
- How does PCIe initialize a link?
- How are QoS and Flow Control different in PCIe 6?
- How does a link negotiate to 64GT/s?
- How do L0p negotiations work?

Learn these things and more in Austin Labs comprehensive PCIe 6.0 Protocol training. Based on the latest PCIe specifications as well as real world test findings from Austin Labs Testing Services, our PCIe protocol training covers the PCIe protocol as well as a guided walk-through of best practices for analyzer configuration and installation.

Our classes are designed for engineering-minded individuals such as test engineers, design engineers, technical/product field support, and storage/system administrators who address low-level protocol issues.

Lab time included in every class.
Outlines are fully customizable for private classes!

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For more information
please contact:
Austin_Labs_Training@Teledyne.com

Austin Labs is a leading provider of testing and training services. We focus on server, storage, and networking interfaces and protocols. Our engineers and trainers are experts in SCSI, RAID, iSCSI, SATA, SAS, FC, FCoE, PCIe, NVMe, USB, CXL and networking protocols.

Our engineers helped develop some of the industry's key technologies and continue to have a vigorous passion for improving products and sharing their knowledge. This experience and enthusiasm translates into the highest quality testing and training services possible.

Introduction to PCIe®

An introduction to PCIe as a protocol as well as the specifications and organization that govern it. Also deals with the marketing aspects that drive PCIe in the current product landscape by addressing the following questions:

- What is PCIe?
- Why do we need PCIe?
- What is the governing organization for PCIe?
- What are the relevant specifications for PCIe and where can they be found?

Components and Terminology

A discussion of concepts, terms, and devices that are integral to the understanding and functionality of PCIe. Students will be given a vocabulary to effectively communicate ideas throughout the learning process by exploring such concepts as:

- Differential Signaling
- Lanes vs. Links
- PAM-4, FEC and Flit Mode
- Scrambling and Encoding
- Switches and Bridges

PCIe Architecture

An examination of the PCIe protocol, its layering, and functionality. This section contains the framework on which the details of the other sections will rest. It covers basic layout of a PCIe system as well as such topics as:

- PCIe Architecture
- Generations and Speeds
- Connectors and Form Factors
- Layering and Functionality

Introducing Flit Mode

A discussion about the changes made to PCIe in version 6, its signaling, error correction and manifold protocol changes made to accommodate the new speed and signal strength inherent in PCIe Gen6. These changes have made a big difference in how PCIe signaling takes place.

PCIe ACK/NAK and Flow Control

This section deals with the functions of reliability and overflow prevention by discussing such subjects as:

- ACK/NAK
- TLP Sequencing
- TLP Buffers
- Scaled Flow Control
- Selective and Bulk replay

PCIe Configuration and Enumeration

A step-by-step look at the PCIe configuration and enumeration process that discusses the following items:

- PCIe Configuration Space
- Base Address Registers (BAR)
- Bus Enumeration

Analyzer Operation and Configuration

A guided walk-through of the best practices for analyzer configuration and insertion into the test environment.

- How to setup for capture
- What to capture
- How to effectively trigger for capture

Austin Labs Testing Services

We test customers' products quickly and thoroughly in an enterprise environment to ensure that products will survive the rigorous demands of mission-critical applications. Customers come to us for our fast turnaround, superior analysis, excellent results, competitive prices, and, of course, 100% confidentiality. We work hand-in-hand with our customers' engineers to provide solutions, not just information. We provide not only the results of our tests, but also the debug, analysis, and regression testing that is needed to ensure that the products we test perform as expected—not for our customers, but for your customers.

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