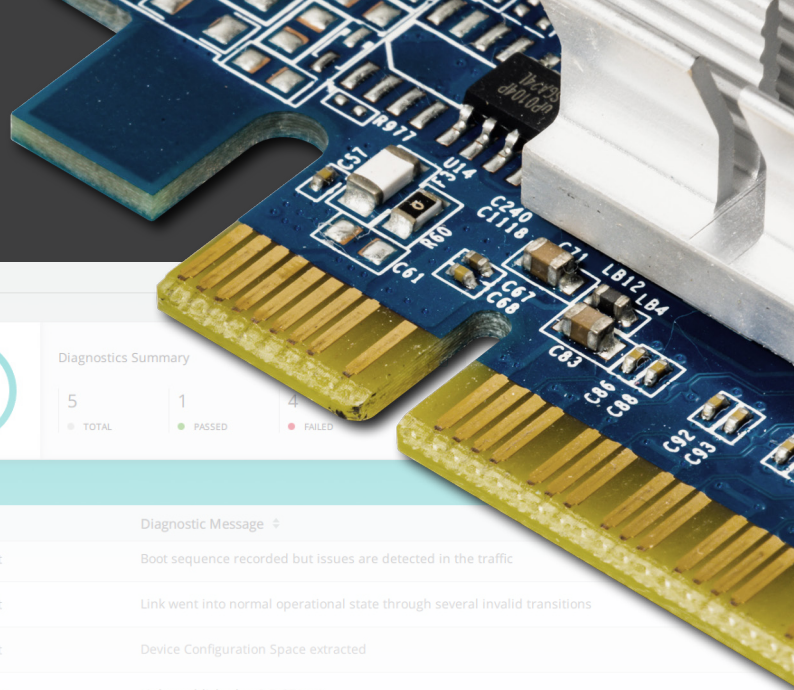




TELEDYNE LECROY
Everywhere you look™



Diagnostics

Run Options

Select Tests

Run All

Diagnostic	Status	Action
System Level Tests		
Link Establishment	PASSED	▶ ✕
Boot Recording	WARNING	
LTSSM Analysis	WARNING	
Configuration Space	PASSED	
Link Speed/Width Parameters	WARNING	
Link Maintenance	FAILED	▶ ✕
System activity recording check	PASSED	
Traffic errors check	PASSED	
Retries check	PASSED	
Timings check	PASSED	

Analyzer Device

Analyzer: Summit T34-2N-16508

1.5 GHz

Status: Connected

Analysis Results

Device Under Test
PCIe Data Center SSD

CONFIGURATION SPACE: SHOW

100%
10min 29sec

Diagnostics Summary
5 TOTAL
1 PASSED
4 FAILED

✓ Diagnostics Completed!

Severity	Test	Diagnostic Message
Warning	Link Establishment	Boot sequence recorded but issues are detected in the traffic
Warning	Link Establishment	Link went into normal operational state through several invalid transitions
Passed	Link Establishment	Device Configuration Space extracted
Warning	Link Establishment	Link established at 2.5 GT/s x1
Passed	Link Maintenance	System activity successfully recorded
Passed	Link Maintenance	No errors found in the traffic
Passed	Link Maintenance	No retries found in traffic
Passed	Link Maintenance	All timings are within acceptable range
Passed	Link Maintenance	There were no transitions to Recovery state during system activity
Passed	Link Maintenance	No NAK DLLPs found in traffic
Failed	Link Maintenance	Downstream data is missing
Failed	Link Maintenance	Traffic was not recorded
Failed	Performance	Both channels data is missing
Failed	Performance	Both channels data is missing

Austin Labs

PCI Express® Protocol Compliance Testing Services



About Austin Labs

Teledyne LeCroy's Austin Labs is the premier third-party test and validation center for servers, storage, and network devices. With decades of testing experience, the lab provides customized services to help our customers deliver fully tested products to market on time and within budget. Experience the best test equipment available including Oscilloscopes, Protocol Analyzers, Jammers, Exercisers, BERT's, and protocol compliance test suites.

Teledyne LeCroy's Austin Labs provides pre-compliance testing for PCI-SIG Protocol (Link/Transaction Layer) and Electrical (PHY Layer) compliance testing requirements. The testing included in this proposal is to outline the test cases that will be attempted as part of the Protocol testing plan. Austin Labs can provide full debug and analysis to help you root cause your issues. Preparation in advance for PCI-SIG compliance testing is critical for vendors to ensure a smooth and successful experience when attempting to be listed on the PCI-SIG Integrators List at Compliance Workshops. Devices (Systems and Add-In cards) are required to pass all tests in all sections to be considered for inclusion on the Integrators List.

Austin Labs uses exactly the same test hardware that is used by PCI-SIG at Compliance workshops to provide the highest level of confidence for pre-compliance testing.



		 Fundamental technology blocks IP/Silicon	 Discrete, application-specific product Device	 Product of components interoperating in one board-level design System (Embedded)	 System built by integrating multiple off-the-shelf and/or custom devices System (Integrated)
	Base Electrical Test	To verify performance relative to the Base specification	To verify component when integrated into device	To verify component when integrated into system	Verified upstream
	Electrical Debug	To find root cause of problems at the component/package level	To find root cause of problems at the board/module level	For dealing with interoperability issues	For dealing with interoperability issues
	Electrical Compliance Test	To verify that component can enable compliant devices	For proving compliance to standard or specification	For providing compliance to standard or specification	To qualify system level building blocks
	Protocol Stimulus	For early component development when ecosystem is not yet complete	For error injection, performance, corner case and regression testing	For error injection testing and component emulation	For testing error handling, also provides Host and Device emulation
	Protocol Analysis	Provides ability to identify, understand, and debug communication issues	Ensures error-free operation while allowing for debugging and performance tuning	Ensures error-free operation while allowing for debugging and performance tuning	For resolving interoperability issues and providing performance analysis
	Protocol Compliance	Validate link and logical communication layers are functioning within specification	Provides for full compliance testing for link and transaction layers	For ensuring system operation aligns with specification requirements	For ensuring interoperability with various compliant devices

Pre-Compliance Testing Services up to PCI Express® Gen 5 plus Gen 6 FYI Testing

Link Layer and Transaction Layer Tests

The tests below are defined in the PCI-SIG document "PCI Express Architecture Link and Transaction Layer Test Specification" and passing results are required for all tests. These tests address the Logical PHY Layer, the Data Link Layer and the Transaction Layer. Tests will be run at all speeds defined by the test specification.

Link 41-20	ReservedFieldsDLLPReceive	Link 61-10	FLR 1	Link 65-10	L1forD3State-C4-16_0
Link 52-100	ReplayTLPOrder	Link 61-20	FLR 2-2_5	Link 65-10	L1forD3State-C4-32_0
Link 52-10	RetransmitOnNak	Link 61-20	FLR 2-5_0	Link 66-10	ASPML1-01-2_5
Link 52-11	REPLAY_TIMER	Link 61-20	FLR 2-8_0	Link 66-10	ASPML1-01-5_0
Link 52-12	REPLAY_NUM	Link 61-20	FLR 2-16_0	Link 66-10	ASPML1-01-8_0
Link 52-150	CorruptedCRC_DLLP	Link 61-20	FLR 2-32_0	Link 66-10	ASPML1-01-16_0
Link 52-160	UndefinedDLLPEncoding	Link 62-10	LTR 1	Link 66-10	ASPML1-01-32_0
Link 52-170	WrongSeqNumInAckDLLP	Link 62-20	LTR 2-2_5	Link 66-10	ASPML1-03-2_5
Link 52-20	LinkRetrainOnRetryFail	Link 62-20	LTR 2-5_0	Link 66-10	ASPML1-03-5_0
Link 53-20	BadLCRC	Link 62-20	LTR 2-8_0	Link 66-10	ASPML1-03-8_0
Link 53-31	DuplicateTLP	Link 62-20	LTR 2-16_0	Link 66-10	ASPML1-03-16_0
Link 53-32	WrongTLPSeqNum	Link 62-20	LTR 2-32_0	Link 66-10	ASPML1-03-32_0
Link 53-40	NullifiedTLP	Link 65-10	L1forD3State-C1-2_5	Link 67-10	BusDevNumCapture
Link 54-20	BadECRC-01 -> 10	Link 65-10	L1forD3State-C1-5_0	Link 68-10	DLFeaturePacket A
Link 54-30	PoisonedTLP	Link 65-10	L1forD3State-C1-8_0	Link 68-10	DLFeaturePacket B
Link 55-10	ReservedBitsinTS	Link 65-10	L1forD3State-C1-16_0	Link 68-10	DLFeaturePacket C
Link 57-10	AdjustInitialPreset for 8.0 GTs	Link 65-10	L1forD3State-C1-16_0	Link 69-12	Precoding
Link 57-11	AdjustInitialPreset for 16.0 GTs	Link 65-10	L1forD3State-C2-2_5	Link 69-12	Precoding Disabled
Link 57-12	AdjustInitialPreset for 32.0 GTs	Link 65-10	L1forD3State-C2-5_0	Link 69-12	Precoding Enabled
Link 58-10	AdjustPresets for 8.0 GTs	Link 65-10	L1forD3State-C2-8_0	Link 70-10	EqualizationRedo8G_2_5
Link 58-11	AdjustPresets for 16.0 GTs	Link 65-10	L1forD3State-C2-16_0	Link 71-10	EqualizationRedo8G_5
Link 58-12	AdjustPresets 32.0 GTs	Link 65-10	L1forD3State-C2-32_0	Link 71-11	EqualizationRedo16G
Link 59-10	AdjustCoefficients for 8.0 GTs 01 -> 55	Link 65-10	L1forD3State-C2-4_5	Link 71-12	EqualizationRedo32G
Link 59-11	AdjustCoefficients for 16.0 GTs 01 -> 55	Link 65-10	L1forD3State-C4-5_0	Phy 2-6	Lane Margining
Link 59-12	AdjustCoefficients for 32.0 GTs 01 -> 55	Link 65-10	L1forD3State-C4-8_0	Trans 1-2	TXN_BFT_RequestCompletion_UR

The Austin Labs Advantage

- Qualified testing staff with extensive industry experience
- Intense focus on working with our customers to provide the best services
- Unmatched combination of testing, training, and test tools
- Completely confidential testing results
- Word class testing facility equipped with test equipment
- Complete analysis and debug of all issues discovered including protocol traces
- Certification testing and validation across both hardware and software
- Ability to provide reports for marketing and engineering purposes

Austin Labs

Tools and Methodology

This project includes running the tests and providing the results of the tests noted above along with PCIe® required testing equipment. Once a purchase order is received, Austin Labs will establish a date when test equipment can be made available to start the project.

The following outlines the timeline and key events from beginning to end of the testing cycle and who participates in each event.

The following outlines the timeline and key events from beginning to end of the testing cycle and who participates in each event.

- 1. Austin Labs provides dedicated contact/engineer for testing project
- 2. Austin Labs provides testing HW required for Gen4 electrical and protocol testing
- 3. Customer provides device under test
- 4. Customer provides any product training needed
- 5. Austin Labs runs tests and provides results to Customer
- 6. Austin Labs provides support for debug and analysis including trace collection and delivery

Test	Result
Link 41-20 ReservedFieldsDLLPReceive	PASSED
Link 52-100 ReplayTLPOrder	PASSED
Link 52-10 RetransmitOnNak	PASSED
Link 52-11 REPLAY_TIMER	PASSED
Link 52-12 REPLAY_NUM	PASSED
Link 52-150 CorruptedCRC_DLLP	PASSED
Link 52-170 WrongSeqNumInAckDLLP	PASSED
Link 52-20 LinkRetrainOnRetryFail	PASSED
Link 53-20 BadLCRC	PASSED
Link 53-31 DuplicateTLP	PASSED

Example Test Matrix

2.40 Link 58-10 AdjustingPresets 05 Result: PASS (1 out of 5 attempts)
2.41 Link 58-10 AdjustingPresets 06 Result: FAIL (5 out of 5 attempts) Details: The tests indicated "FAILURE: More than 32 ms before FS and LF reported by DUT." The analyzer buffer size was increased to 256MB as this is a common reason for failure in these tests, yet the test still failed. This test and the failing result should be further investigated before attempting certification.
2.42 Link 58-10 AdjustingPresets 07 Result: PASS (1 out of 5 attempts)

Example Test Results Description

Our engineers helped develop some of the industry’s key technologies and continue to have a vigorous passion for improving products and sharing their knowledge. This experience and enthusiasm translates into the highest quality testing and training services possible. We specialize in:

- ✓ Data Integrity
 - ✓ Signal Integrity
 - ✓ Stress and Performance Benchmarking
 - ✓ Compliance and Interoperability
- ✓ Protocol Analysis and Compliance
 - ✓ Error Injection and Recovery
 - ✓ Hardware and Software Feature Validation
 - ✓ Market and Product Analysis
- ✓ Interoperability
 - ✓ Virtualization
 - ✓ Automation

Why third-party validation?



COST SAVINGS

Third-party validation provides a defined solution with known expenses



RESOURCE CONSTRAINTS

Doing more with less means having to find new ways to test



HARDWARE NEEDS

Independent labs provide access to a wide range of equipment



TIME

Delivery schedules are always shortened – beat the market with a partner



PERSPECTIVE

It is beneficial to have someone external to the project test with a new view

Why Austin Labs?

ATTITUDE

- We will find serious flaws and bugs
- We will help you understand how to isolate and fix these problems
- We are your partner

APPROACH

- Our focus is on the entire product from documentation to critical issues
- We specialize in data corruption, data loss, disruptions
- We are protocol experts and have the tools to test protocol compliance
- We are attentive to issues that get overlooked

QUALITY

- We use Teledyne LeCroy test and analysis tools along with industry tools
- We supplement internal testing and provide an external validation
- Our customers always come back for more



TELEDYNE LECROY
Everywhere you look™

Want to become a Protocol Expert?

Austin Labs also offers a full line of advanced protocol training classes. Each of the classes is instructor-led and guides the students through the protocol specifications while using hands on labs with trace analysis to help students discover how the protocol is implemented. Classes are available on-site with a live instruction or through a virtual classroom environment. Additional topics are available upon request.

Current class offerings include:

- PCIe
- NVMe
- NVMe over RoCE
- NVMe over Fibre Channel
- NVMe over TCP
- Fibre Channel
- iSCSI
- SAS
- CXL



Austin Labs PCI Express® Protocol Compliance Testing Services

Please visit teledynelecroy.com/events/ for a listing of scheduled learning events.

teledynelecroy.com/services/austinlabs-testing.aspx
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