QPHY-DDR3

DDR3 Serial Data Compliance Software

Instruction Manual

Revision C – November, 2017

Relating to:

XStreamDSO™ Version 8.5.x.x and later

QualiPHY Software Version 8.5.x.x and later

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About This Manual

This manual assumes that you are familiar with using an oscilloscope–in particular the Teledyne LeCroy oscilloscope that will be used with QualiPHY–and that you have purchased the QPHY-DDR3 software option. Some of the images in this manual may have been captured using different model oscilloscopes, as they are meant to illustrate general concepts only. Rest assured that while the user interface may look different from yours, the functionality is identical.

Introduction

QualiPHY is highly automated compliance test software meant to help you develop and validate the PHY (physical-electrical) layer of a device, in accordance with the official documents published by the applicable standards organizations and special interest groups (SIGs). You can additionally set custom variables and limits to test compliance to internal standards.

QualiPHY is composed of a “framework” application that enables the configuration and control of separate tests for each standard through a common user interface. Features include:

- **Multiple Data Source Capability**
- **User-Defined Test Limits**: Tighten limits to ensure devices are well within the passing region, even if subsequently measured with different equipment.
- **Flexible Test Results Reporting** that includes XML Test Record Generation. Understand device performance distribution, or obtain process related information from the devices under test.

QPHY-DDR3 is an automated test package performing all the real time oscilloscope tests for Double Data Rate in accordance with JEDEC Standard No. JESD79-3F (DDR3), the JESD79-3-1A.01 addendum (DDR3L), and JESD209-3B (LPDDR3).

The software can be run on any Teledyne LeCroy oscilloscope with at least 2.5 GHz bandwidth and 20 GS/s sampling rate, although it is recommended to use an oscilloscope with greater bandwidth. Refer to the table below for the minimum recommended bandwidth for each variant and speed of DDR3.

QPHY-DDR3	Recommended Bandwidth
DDR3 (1600 MT/s or less)	6 GHz
DDR3 (1866 MT/s or greater)	8 GHz
DDR3L (All speeds)	8 GHz
LPDDR3 (All speeds)	6 GHz

Required Equipment

- Teledyne LeCroy real-time oscilloscope, ≥2.5 GHz BW, installed with:
  - XStreamDSO v.7.6.x.x minimum* with an activated QPHY-DDR3 option key
  - QualiPHY software v.7.6.x.x minimum with an activated QPHY-DDR3 component
  - VirtualProbe software option*

  ***Note**: The versions of XStreamDSO and QualiPHY software must match, so upgrade QualilPHY if you have upgraded your oscilloscope firmware. The versions listed above are the minimum versions required for this product. VirtualProbe is only required to use de-embedding tools. The QualiPHY software may be installed on a remote PC, but all other software must be run on the oscilloscope.

- A minimum of three differential probes ≥ 4 GHz (a fourth probe is required for some probe setups)

  Note: 6 or 8 GHz probes recommended depending on your test speed, per table above.

- PCF200 Probe Deskew and Calibration Fixture (included with WaveLink probe systems)

Remote Host Computer System Requirements

Usually, the oscilloscope is the host computer for the QualiPHY software, and all models that meet the acquisition requirements will also meet the host system requirements. However, if you wish to run the QualiPHY software from a remote computer, these minimum requirements apply:

- Operating System:
  - Windows 7 Professional
  - Windows 10 Professional
- 1 GHz or faster processor
- 1 GB (32-bit) or 2 GB (64-bit) of RAM
- Ethernet (LAN) network capability
- Hard Drive:
  - At least 100 MB free to install the framework application
  - Up to 2 GB per standard installed to store the log database (each database grows from a few MB to a maximum of 2 GB)

See Set Up Remote Control for configuration instructions.

Installation and Setup

QualiPHY is a Windows-based application that can be configured with one or more serial data compliance components. Each compliance component is purchased as a software option.

Install Base Application

Download the latest version of the QualiPHY software from:

teledynelecroy.com/support/softwaredownload under Oscilloscope Downloads > Software Utilities.

If the oscilloscope is not connected to the Internet, copy the installer onto a USB memory stick then transfer it to the oscilloscope desktop or a folder on a D:\ drive to execute it.

Run **QualiPHYInstaller.exe** and follow the installer prompts. Choose all the components you plan to activate. If you omit any components now, you will need to update the installation to activate them later.

By default, the oscilloscope appears as local host when QualiPHY is executed on the oscilloscope. Follow the steps under Add Connection to QualiPHY to check that the IP address is **127.0.0.1**.

Activate Components

The serial data compliance components are factory installed as part of the main application in your oscilloscope and are individually activated through the use of an alphanumeric code uniquely matched to the oscilloscope's serial number. This option key code is what is delivered when purchasing a software option.

To activate a component on the oscilloscope:

1. From the menu bar, choose **Utilities > Utilities Setup**.
2. On the Options tab, click **Add Key**.
3. Use the Virtual Keyboard to **Enter Option Key**, then click **OK**.

   If activation is successful, the key code now appears in the list of Installed Option Keys.
4. Restart the oscilloscope application by choosing **File > Exit**, then double-clicking the **Start DSO** icon on the desktop.

Set Up Dual Monitor Display

Teledyne LeCroy recommends running QualiPHY on an oscilloscope equipped with Dual Monitor Display capability. This allows the waveform and measurements to be shown on the oscilloscope LCD display while the QualiPHY application and test results are displayed on a second monitor.

See the oscilloscope *Operator's Manual* for instructions on setting up dual monitor display.

Set Up Remote Control

QualiPHY software can be executed from a remote host computer, controlling the oscilloscope through a LAN Connection. To set up remote control:

- The oscilloscope must be connected to a LAN and assigned an IP address (fixed or dynamic).
- The host computer must be on the same LAN as the oscilloscope.

Configure Oscilloscope for Remote Control

1. From the menu bar, choose Utilities → Utilities Setup...
2. Open the **Remote** tab and set Remote Control to **TCP/IP**.
3. Verify that the oscilloscope shows an IP address.

Add Connection to QualiPHY

1. On the host PC, download and run **QualiPHYInstaller.exe**.
2. Start QualiPHY and click the **General Setup** button.
3. On the Connection tab, click Scope Selector.
4. Click **Add** and choose the connection type. Enter the oscilloscope IP address from Step 3 above. Click **OK**.
5. When the oscilloscope is properly detected, it appears on the Scope Selector dialog. Select the connection, and click **OK**.

   QualiPHY is now ready to control the oscilloscope.

Select Connection

Multiple oscilloscopes may be accessible to a single remote host. In that case, go to General Setup and use the Scope Selector at the start of the QPHY session to choose the correct connection.

QualiPHY tests the oscilloscope connection when starting a test. The system warns you if there is a connection problem.

Using QualiPHY

This section provides an overview of the QualiPHY user interface and general procedures. For detailed information about the QPHY-DDR3 software option, see QPHY-DDR3 Testing.

Accessing the Software

Once QualiPHY is installed and activated, it can be accessed from the oscilloscope menu bar by choosing **Analysis > QualiPHY**, or by double-clicking the **QualiPHY desktop icon** on a remote computer.

The QualiPHY framework dialog illustrates the overall software flow, from general set up through running individual compliance tests. Work from left to right, making all desired settings on each sub-dialog.

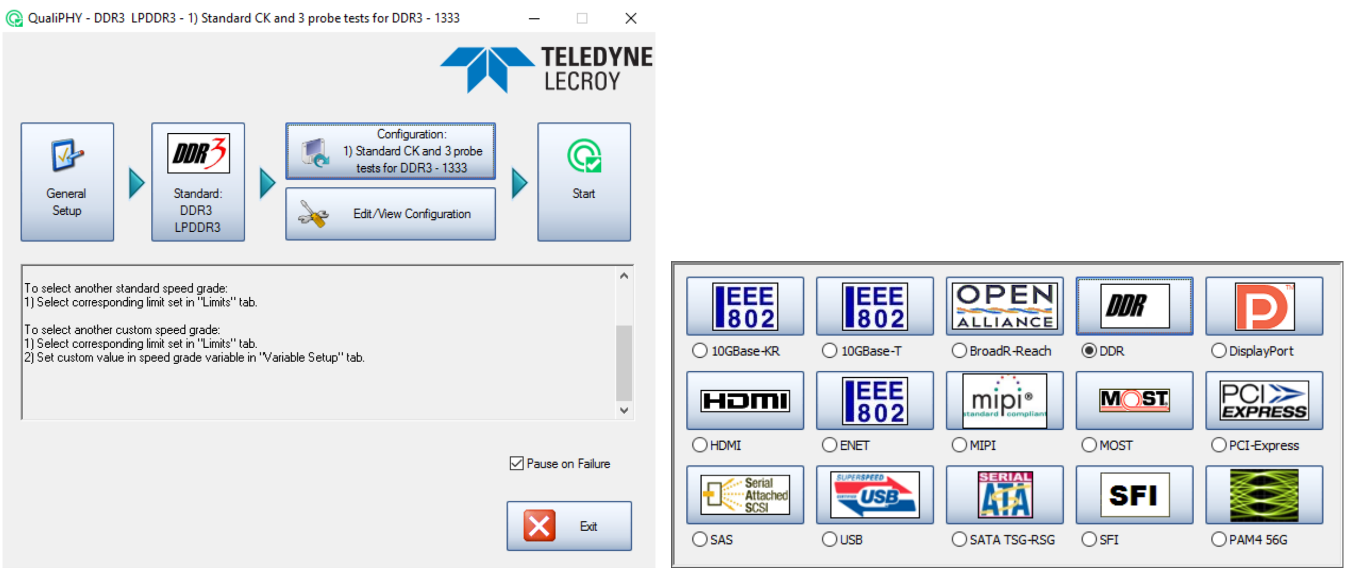


Figure 1. QualiPHY framework dialog and Standard selection menu

The sub-dialogs are organized into tabs each containing configuration controls related to that part of the process. These are described in more detail in the following sections.

If **Pause on Failure** is checked, QauliPHY prompts to retry a measure whenever a test fails.

Report Generator launches the manual report generator dialog.

The **Exit** button at the bottom of the framework dialog closes the QualiPHY application.

General Setup

The first sub-dialog contains general system settings. These remain in effect for each session, regardless of Standard, until changed.

Setup tab

Settings made on this tab will preselect configurations and tests based on which Generation of the protocol you are testing.

Connection tab

Shows **IP Address** of the test oscilloscope (local host 127.0.0.1 if QualiPHY is run from the oscilloscope). The **Scope Selector** allows you to choose the oscilloscope used for testing when several are connected to the QualiPHY installation. See Set Up Remote Control for details.

Session Info tab

Optional information about the test session that may be added to reports, such as: **Operator Name**, **Device Under Test** (DUT), **Temperature** (in °C) of the test location, and any additional **Comments**. There is also an option to **Append Results** or **Replace Results** when continuing a previous session.

To optimize report generation, enter at least a DUT name at the beginning of each session.

Report tab

Settings related to automatic report generation. Choose:

- Reporting behavior of:
    - "Ask to generate a report after tests," where you'll be prompted to create a new file for each set of test results.
    - "Never generate a report after tests," where you'll need to manually execute the Report Generator to create a report.
    - "Always generate a report after tests," to autogenerate a report of the latest test results.
- **Default** report output type of XML, HTML, or PDF.
- A generic **Output file name**, including the full path to the report output folder.

Optionally, check **Allow style sheet selection in Report Generator** to enable the use of a custom .xslt when generating reports (XML and HTML output only). The path to the .xslt is entered on the Report Generator dialog.

Report Generator launches the Report Generator dialog, which contains the same settings as the Report tab, only applied to individual reports.

Advanced tab

This tab launches the **X-Replay Mode** dialog. See X-Replay Mode.

About tab

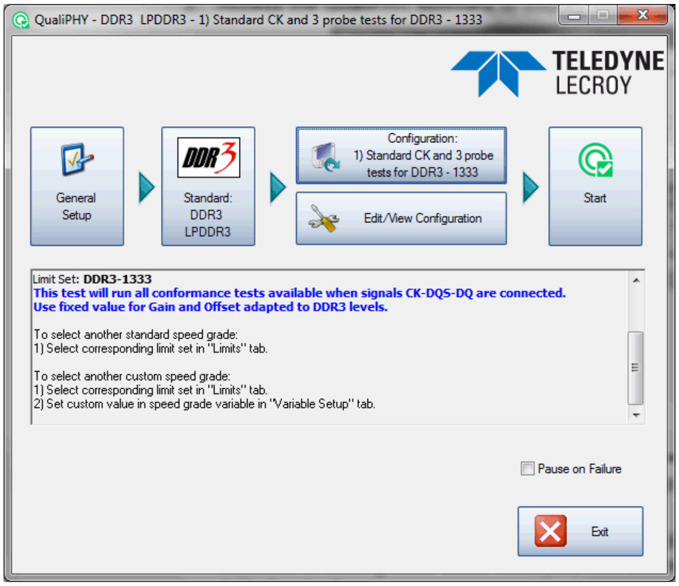
Information about your QualiPHY installation.

QualiPHY Test Process

Once general system settings are in place, these are the steps for running test sessions.

Set Up Test Session

1. Connect the oscilloscope to the DUT. See QPHY-DDR3 Testing Physical Setup.
2. Access the QualiPHY software to display the framework dialog.



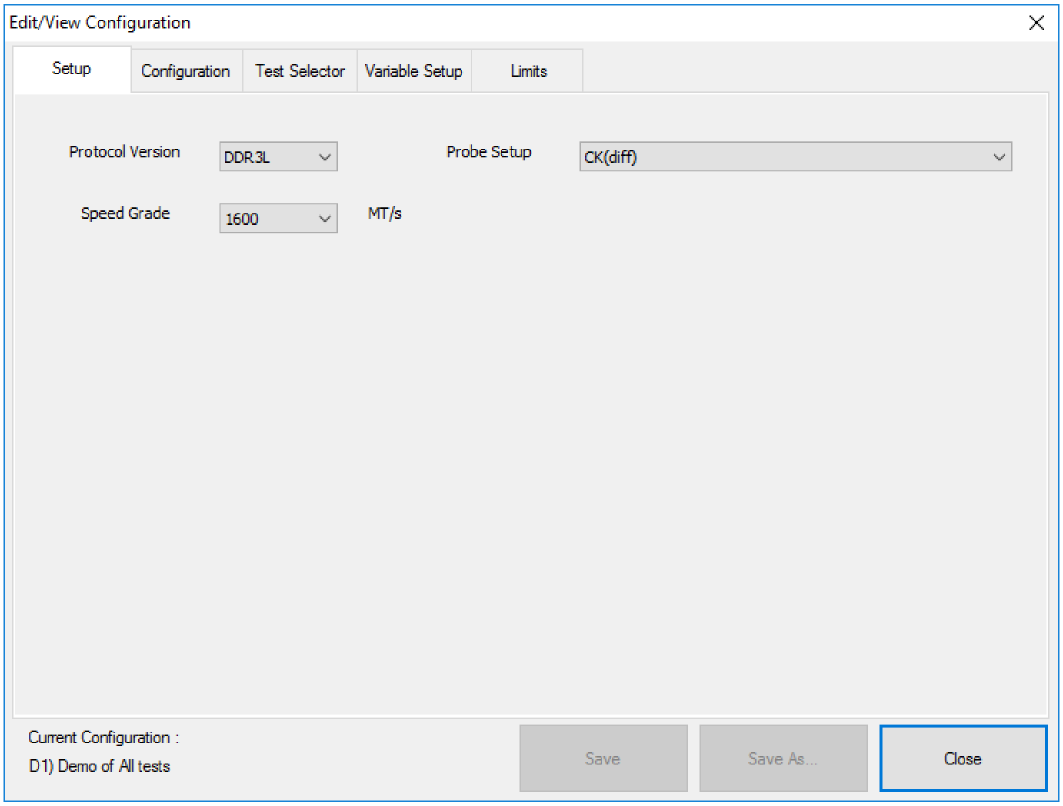
3. If running QualiPHY remotely, click **General Setup** and open the **Scope Selector** to select the correct oscilloscope connection.
4. If you have more than one component activated, click **Standard** and select the desired standard to test against. Otherwise, your one activated component will appear as the default selection.

   Note: Although all the QualiPHY components appear on this dialog, only those selected when installing QualiPHY are enabled for selection now.

5. Click the **Configuration** button and select the test configuration to run. These pre-loaded configurations are set up to run a number of common tests to provide a quick, easy way to begin testing. See QPHY-DDR3 Test Configurations for a description of your configurations.

   You can also create custom configurations by copying and modifying the pre-loaded configurations. See Customizing QualiPHY for details.

6. Return to the framework dialog, then click the **Edit/View Configuration** button to open the **Setup** tab. Make selections as required to tailor the configuration to your test setup (e.g., changing Speed Grade or Probe Setup).



   If you make changes, **Save As** a new configuration.

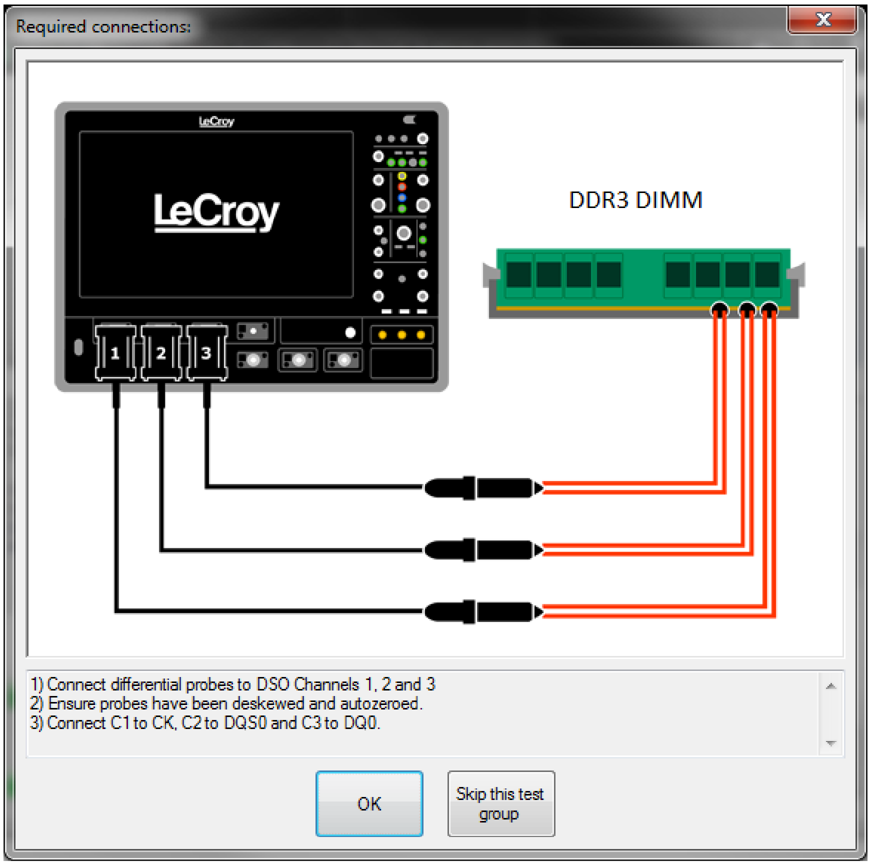
7. **Close** the Edit/View Configuration dialog to return to the framework dialog. The modified configuration will be pre-selected on the framework dialog.

Run Tests

1. On the framework dialog, click **Start** to begin testing.

   When tests are in progress, this button changes to **Stop**. Click it at any time to stop the test in process. You'll be able to resume from the point of termination or from the beginning of the test.

2. Follow the pop-up window prompts. QualiPHY guides you step-by-step through each of the tests described in the standard specification, including diagrams of the connection to the DUT for each required test mode.



3. When all tests are successfully completed, both progress bars on the framework dialog are completely green and the message "All tests completed successfully" appears. If problems are encountered, you'll be offered options to:

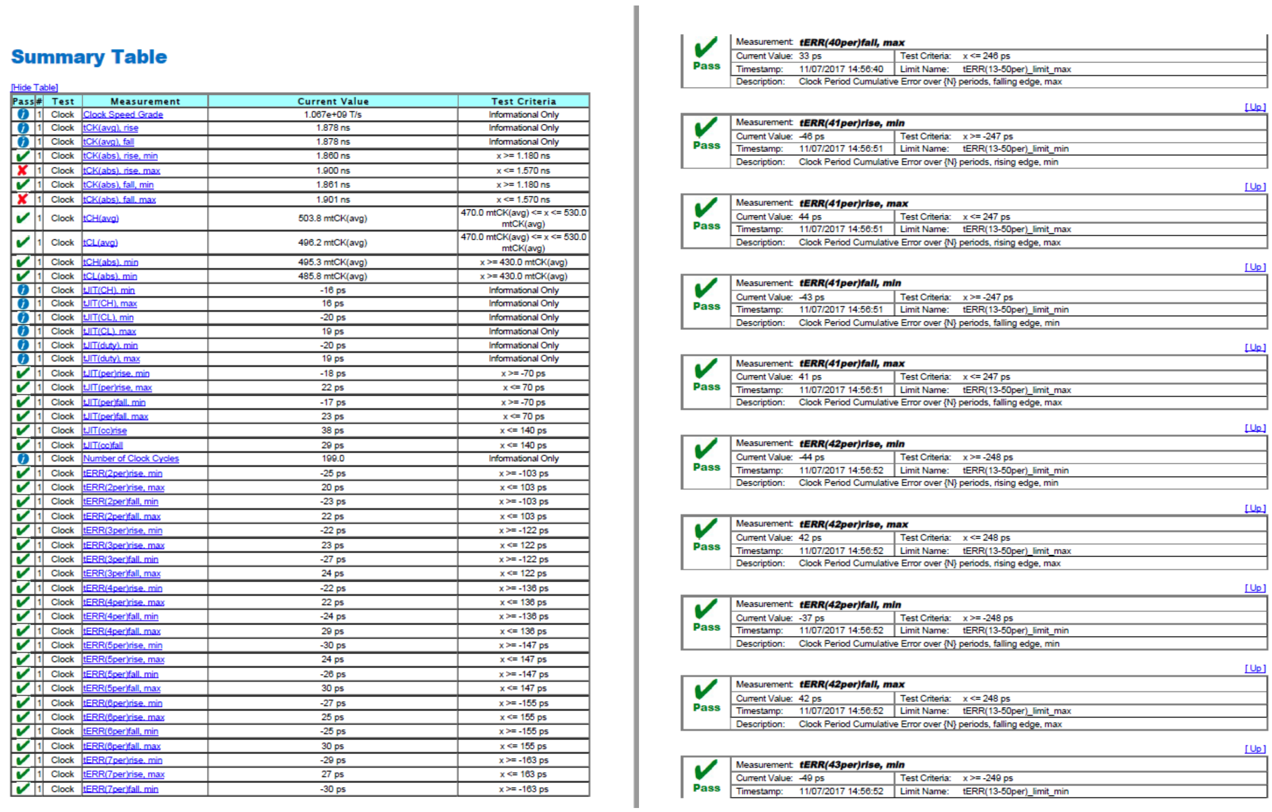
   - **Retry** the test from the latest established point defined in the script
   - **Ignore and Continue** with the next test
   - **Abort Session**

Generate Reports

The QualiPHY software automates report generation. On the framework dialog, go to **General Setup > Report** to pre-configure reporting behavior. You can also manually launch the **Report Generator** from the framework dialog once a test is run.

The Report Generator offers the same selections as the Report tab, only applied to each report individually, rather than as a system setting. This enables you to save reports for each test session, rather than overwrite the generic report file. There are also options to link a custom style sheet (.xslt) to the report, or to Exclude Informative Results.

The Test Report includes a summary table with links to the detailed test result pages.



Summary Table

[Hide Table]

Pass	#	Test	Measurement	Current Value	Test Criteria
i	1	Clock	Clock Speed Grade	1.067e+09 T/s	Informational Only
i	1	Clock	tCK(avg), rise	1.878 ns	Informational Only
i	1	Clock	tCK(avg), fall	1.878 ns	Informational Only
✔	1	Clock	tCK(abs), rise, min	1.860 ns	x >= 1.180 ns
✘	1	Clock	tCK(abs), rise, max	1.900 ns	x <= 1.570 ns
✔	1	Clock	tCK(abs), fall, min	1.861 ns	x >= 1.180 ns
✘	1	Clock	tCK(abs), fall, max	1.901 ns	x <= 1.570 ns
✔	1	Clock	tCH(avg)	503.8 mtCK(avg)	470.0 mtCK(avg) <= x <= 530.0 mtCK(avg)
✔	1	Clock	tCL(avg)	496.2 mtCK(avg)	470.0 mtCK(avg) <= x <= 530.0 mtCK(avg)
✔	1	Clock	tCH(abs), min	495.3 mtCK(avg)	x >= 430.0 mtCK(avg)
✔	1	Clock	tCL(abs), min	485.8 mtCK(avg)	x >= 430.0 mtCK(avg)
i	1	Clock	tJIT(CH), min	-16 ps	Informational Only
i	1	Clock	tJIT(CH), max	16 ps	Informational Only
i	1	Clock	tJIT(CL), min	-20 ps	Informational Only
i	1	Clock	tJIT(CL), max	19 ps	Informational Only
i	1	Clock	tJIT(duty), min	-20 ps	Informational Only
i	1	Clock	tJIT(duty), max	19 ps	Informational Only
✔	1	Clock	tJIT(per)rise, min	-18 ps	x >= -70 ps
✔	1	Clock	tJIT(per)rise, max	22 ps	x <= 70 ps
✔	1	Clock	tJIT(per)fall, min	-17 ps	x >= -70 ps
✔	1	Clock	tJIT(per)fall, max	23 ps	x <= 70 ps
✔	1	Clock	tJIT(cc)rise	38 ps	x <= 140 ps
✔	1	Clock	tJIT(cc)fall	29 ps	x <= 140 ps
i	1	Clock	Number of Clock Cycles	199.0	Informational Only
✔	1	Clock	tERR(2per)rise, min	-25 ps	x >= -103 ps
✔	1	Clock	tERR(2per)rise, max	20 ps	x <= 103 ps
✔	1	Clock	tERR(2per)fall, min	-23 ps	x >= -103 ps
✔	1	Clock	tERR(2per)fall, max	22 ps	x <= 103 ps
✔	1	Clock	tERR(3per)rise, min	-22 ps	x >= -122 ps
✔	1	Clock	tERR(3per)rise, max	23 ps	x <= 122 ps
✔	1	Clock	tERR(3per)fall, min	-27 ps	x >= -122 ps
✔	1	Clock	tERR(3per)fall, max	24 ps	x <= 122 ps
✔	1	Clock	tERR(4per)rise, min	-22 ps	x >= -136 ps
✔	1	Clock	tERR(4per)rise, max	22 ps	x <= 136 ps
✔	1	Clock	tERR(4per)fall, min	-24 ps	x >= -136 ps
✔	1	Clock	tERR(4per)fall, max	29 ps	x <= 136 ps
✔	1	Clock	tERR(5per)rise, min	-30 ps	x >= -147 ps
✔	1	Clock	tERR(5per)rise, max	24 ps	x <= 147 ps
✔	1	Clock	tERR(5per)fall, min	-26 ps	x >= -147 ps
✔	1	Clock	tERR(5per)fall, max	30 ps	x <= 147 ps
✔	1	Clock	tERR(6per)rise, min	-27 ps	x >= -155 ps
✔	1	Clock	tERR(6per)rise, max	25 ps	x <= 155 ps
✔	1	Clock	tERR(6per)fall, min	-25 ps	x >= -155 ps
✔	1	Clock	tERR(6per)fall, max	30 ps	x <= 155 ps
✔	1	Clock	tERR(7per)rise, min	-29 ps	x >= -163 ps
✔	1	Clock	tERR(7per)rise, max	27 ps	x <= 163 ps
✔	1	Clock	tERR(7per)fall, min	-30 ps	x >= -163 ps

Pass	Measurement	Current Value	Test Criteria	Timestamp	Limit Name	Description
✔ Pass	tERR(40per)fall, max	33 ps	x <= 246 ps	11/07/2017 14:56:40	tERR(13-50per)_limit_max	Clock Period Cumulative Error over {N} periods, falling edge, max
✔ Pass	tERR(41per)rise, min	-46 ps	x >= -247 ps	11/07/2017 14:56:51	tERR(13-50per)_limit_min	Clock Period Cumulative Error over {N} periods, rising edge, min
✔ Pass	tERR(41per)rise, max	44 ps	x <= 247 ps	11/07/2017 14:56:51	tERR(13-50per)_limit_max	Clock Period Cumulative Error over {N} periods, rising edge, max
✔ Pass	tERR(41per)fall, min	-43 ps	x >= -247 ps	11/07/2017 14:56:51	tERR(13-50per)_limit_min	Clock Period Cumulative Error over {N} periods, falling edge, min
✔ Pass	tERR(41per)fall, max	41 ps	x <= 247 ps	11/07/2017 14:56:51	tERR(13-50per)_limit_max	Clock Period Cumulative Error over {N} periods, falling edge, max
✔ Pass	tERR(42per)rise, min	-44 ps	x >= -248 ps	11/07/2017 14:56:52	tERR(13-50per)_limit_min	Clock Period Cumulative Error over {N} periods, rising edge, min
✔ Pass	tERR(42per)rise, max	42 ps	x <= 248 ps	11/07/2017 14:56:52	tERR(13-50per)_limit_max	Clock Period Cumulative Error over {N} periods, rising edge, max
✔ Pass	tERR(42per)fall, min	-37 ps	x >= -248 ps	11/07/2017 14:56:52	tERR(13-50per)_limit_min	Clock Period Cumulative Error over {N} periods, falling edge, min
✔ Pass	tERR(42per)fall, max	42 ps	x <= 248 ps	11/07/2017 14:56:52	tERR(13-50per)_limit_max	Clock Period Cumulative Error over {N} periods, falling edge, max
✔ Pass	tERR(43per)rise, min	-49 ps	x >= -249 ps	11/07/2017 14:56:52	tERR(13-50per)_limit_min	

[Up] [Up] [Up] [Up] [Up] [Up] [Up] [Up] [Up]

Figure 2. Test Report Summary Table and Details pages

Reports are output to the folder D:\QPHY\Reports, or C:\LeCroy\QPHY\Reports if QualiPHY is installed on a remote PC.

You can add your own logo to the report by replacing the file *\QPHY\StyleSheets\CustomerLogo.jpg.

The recommended maximum size is 250x100 pixels at 72 ppi, 16.7 million colors, 24 bits. Use the same file name and format.

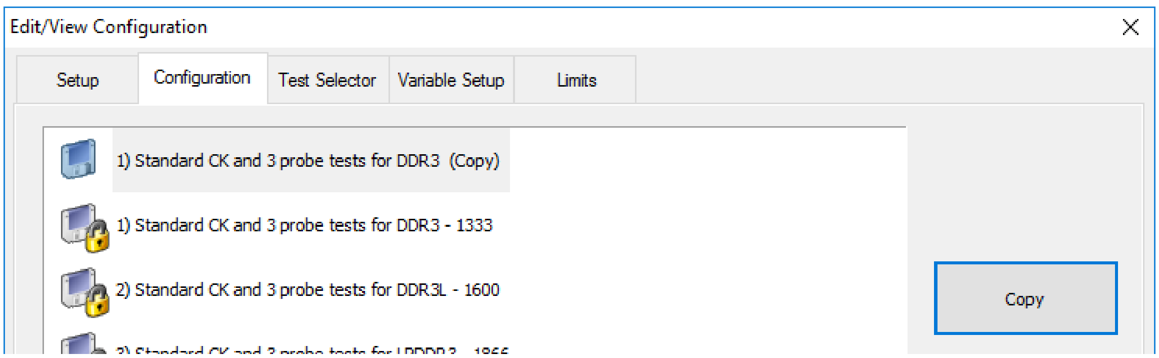
Customizing QualiPHY

The pre-loaded configurations cannot be modified. However, you can create your own test configurations by copying one of the pre-loaded configurations and modifying it.

Copy Configuration

1. Access the QualiPHY framework dialog and select a **Standard**.
2. Click **Edit/View Configuration** and select the configuration upon which to base the new configuration. This can be a pre-loaded configuration or another copy.
3. Click **Copy** and enter a name and description. Once a custom configuration is defined, it appears on the Configuration tab.

   Note: Until you enter a new name, the new configuration is shown followed by "(Copy)".

4. Select the new, custom configuration and follow the procedures below to continue making changes.

   Note: When any configuration is changed, the Save As button at the bottom of the Configuration tab becomes active. When a custom configuration is changed, the Save button also becomes active to apply the changes to the existing configuration, rather than create a new one.

Edit Setup

On the Setup tab, make any changes required to tailor the configuration to your DUT. Your selections here will modify the corresponding test variables:

- Protocol Version – DDR3, DDR3L, or LPDDR3
- Speed Grade – the speed grades associated with the selected protocol version, or a Custom Speed Grade
- Probe Setup – the physical setup in use

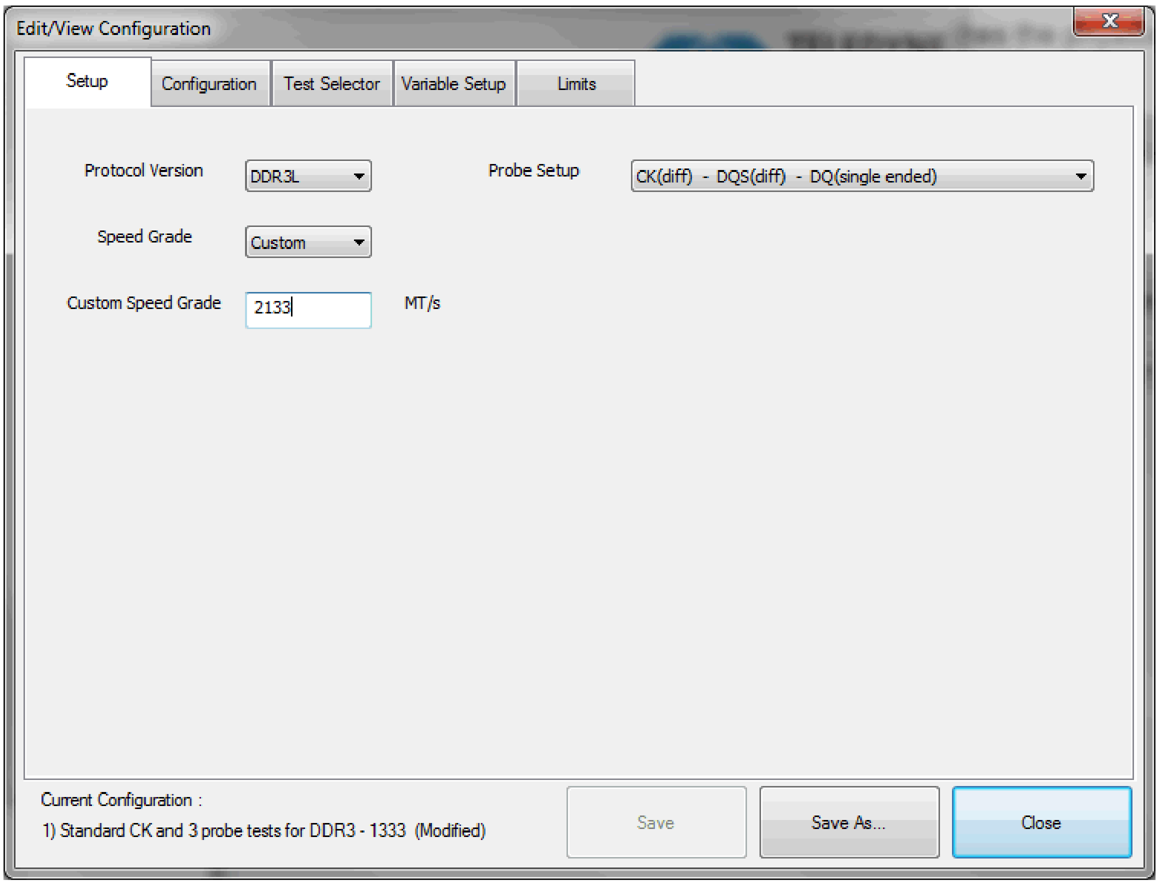


Figure 3. Configuration Setup Tab

Select Tests

On the **Test Selector** tab, check the tests that make up the configuration. Each test is defined by the DDR3, DDR3L, or LPDDR3 standards. A description of each test is displayed when it is selected.

To loop an individual test or group of tests, select it from the list, then choose to **Loop selected test** until stopped or enter the number of repetitions. When defining a number of repetitions, enter the number of repetitions before selecting the checkbox.

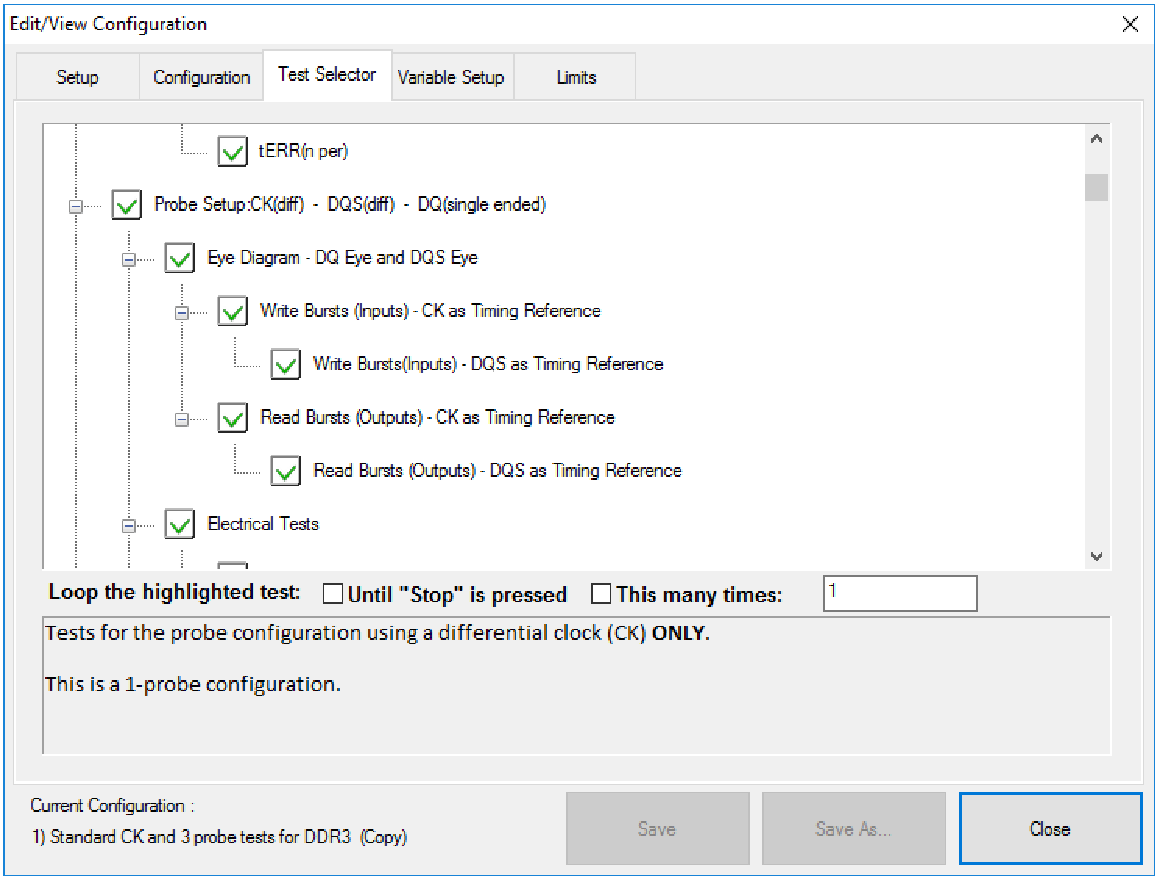


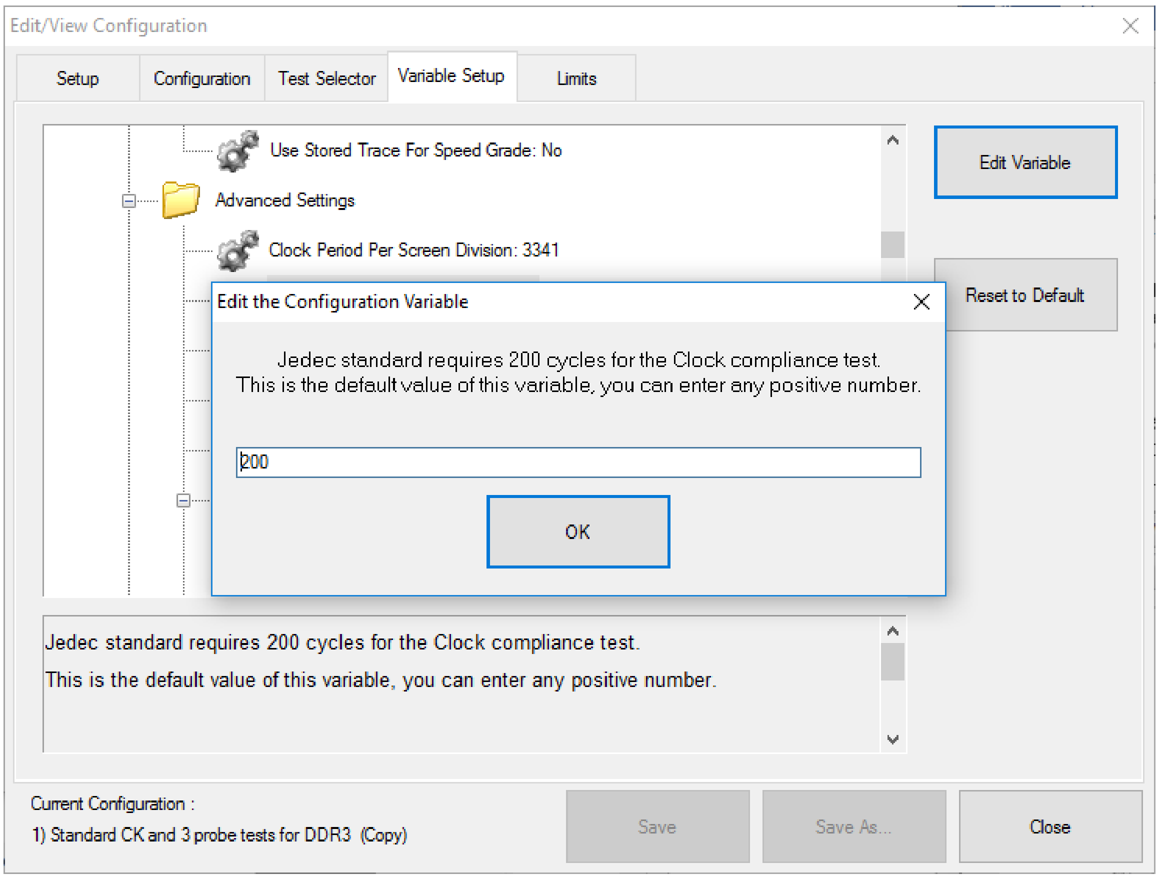
Figure 4. Configuration Test Selector Tab

Edit Variables

The Variable Setup tab contains a list of test variables. See QPHY-DDR3 Variables for a description of each.

To modify a variable:

1. Select the variable on the Variable Setup tab, then click **Edit Variable**. (You can also choose to Reset to Default at any time.)
2. The conditions of this variable appear on a pop-up. Choose the new condition to apply.



Edit Test Limits

The Limits tab shows the Limit Set currently associated with the configuration. Any limit set can be associated with a custom configuration by selecting it in this field.

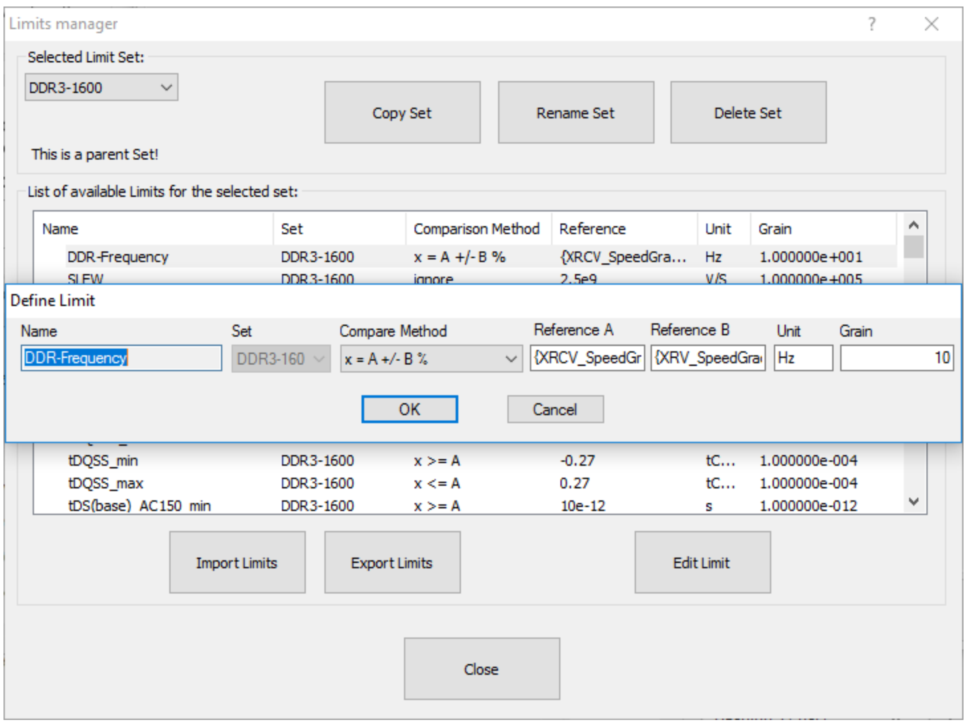
The Limits Manager shows the settings for every test limit in a limit set. Those in the default set are the limits defined by the standard.

To create a custom limit set:

1. On the Limits tab, click **Limits Manager**.
2. With the default set selected, click **Copy Set** and enter a name.

   Note: You can also choose to copy and/or modify another custom set that has been associated with this configuration.

3. Double click the limit to be modified, and in the pop-up enter the new values.



You can also **Import Limits** from a .csv file. Navigate to the file location after clicking the button.

Tip: Likewise, Export Limits creates a .csv file from the current limit set. You may wish to do this and copy it to format the input .csv file.

X-Replay Mode

The X-Replay mode window is an advanced ("developer") view of QualiPHY. The tree in the upper-left frame enables you to navigate to processes in the DDR3 test script, in case you need to review the code, which appears in the upper-right frame.

Two other particularly useful features are:

- A **list of recent test sessions** in the lower-left frame. While you can only generate a report of the current test session in the QualiPHY wizard, in X-Replay Mode you can generate a report for any of these recent sessions. Select the session and choose **Report > Create Report** from the menu bar.
- The **QualiPHY log** in the bottom-right frame. The frame can be split by dragging up the lower edge. The bottom half of this split frame now shows the **raw Python output**, which can be useful if ever the script needs debugging.

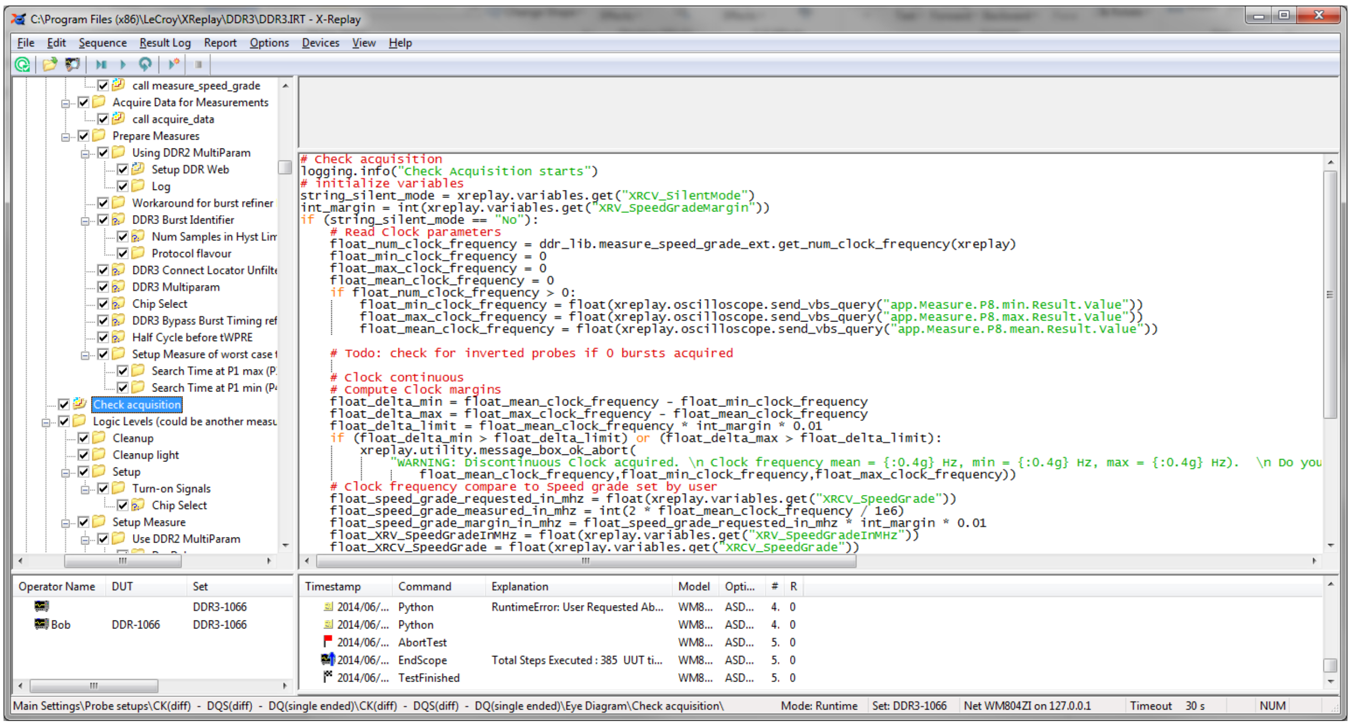


Figure 5. X-Replay Mode window

QPHY-DDR3 Testing

Test Preparation

Before beginning any test or data acquisition, the oscilloscope should be warmed for at least 20 minutes.

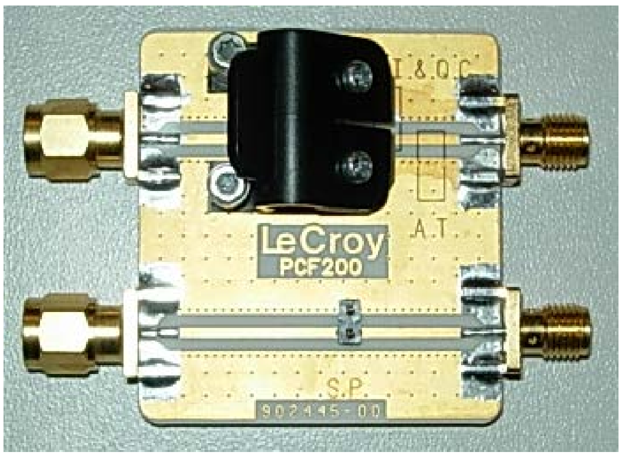
Calibration is automatically performed by the oscilloscope software; no manual calibration is required. The calibration procedure will be run again if the temperature of the oscilloscope changes by more than a few degrees.

Deskewing the Probes

For DDR measurements, it is crucial to make sure that probes are properly deskewed before running QPHY-DDR3 to ensure proper signal timing. Ideally, the same settings should be used when deskewing as when acquiring signals for analysis. This will ensure that the channels are deskewed using the same setup as when running conformance tests. Deskew values are saved and stored by QualiPHY at the beginning of each run.

Required Equipment

- PCF200 (included with "-PS" probe systems)



- Square-Pin (SP) tip (included with D4x0-PS, D6x0-PS, and Dxx30-PS)
- 50 Ω terminator

Note: Alternatively an LPA-K-A adapter and a SMA cable could be used

Methodology

Before beginning the procedure, be sure to warm the oscilloscope for at least 20 minutes.

1. Connect the PCF200 to the oscilloscope's fast edge output. The PCF200 fixture has two different signal paths that can be used, depending on the type of probe tip being used for the measurement:

    - The upper signal path is for deskewing Solder-In (SI), Quick-Connect (QC) and Adjustable Tip (AT) probe tips.
    - The lower circuit is for Square-Pin (SP) probe tips.

    Depending upon which probe tip is being used, connect the appropriate signal path to the fast edge output. For ease of connectivity it is recommended that SP tip is used. As long as the same tip is used to deskew each probe it does not matter which style of probe tip is used.

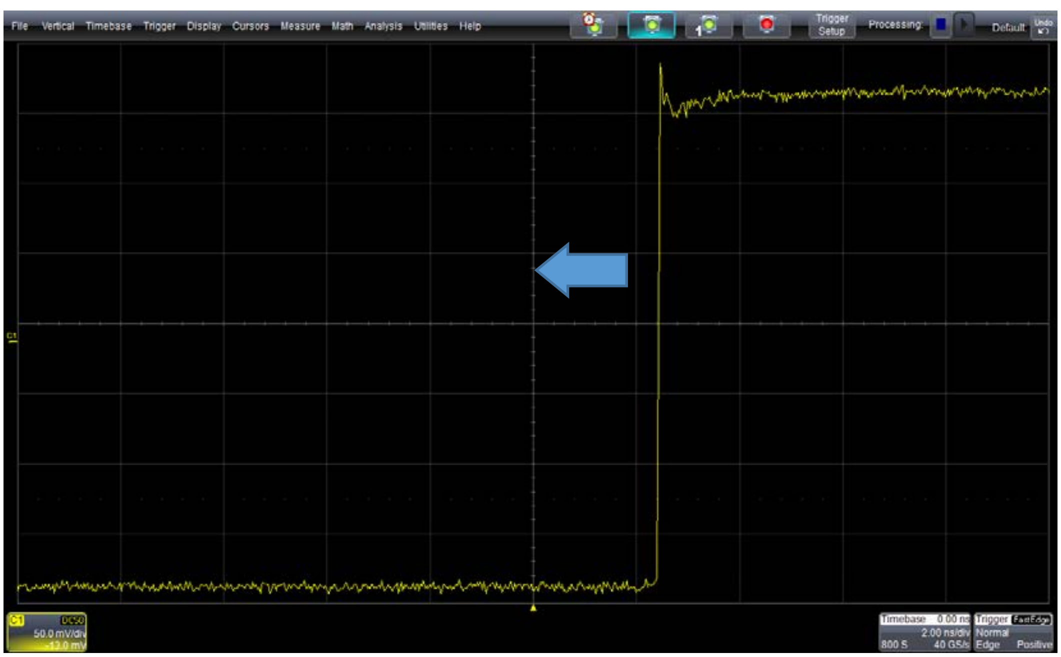
2. Connect probes electrically in a single-ended arrangement using their designated area on the fixture:

    - Connect the positive side of the probe to the signal trace (in between the two white strips). The positive polarity is indicated on the tip of the probe by a plus sign.
    - Connect the negative side to the ground plane (outside of the white strips).
    - In order to minimize reflections, apply a 50 Ω terminator to the end of the signal path in use. If a 50 Ω terminator is not available, an SMA cable can be used to terminate the PCF200 to one of the oscilloscope's outputs.

3. Set the oscilloscope **Trigger Source** to **Fast Edge**, **Trigger Type** to **Edge**.

4. Set a **Timebase** of approximately **10 ns/div** and **Timebase Delay** of **0.**

    Once everything is properly set up the oscilloscope display should look similar to the figure below. If there is no propagation delay due to the probe, and no internal oscilloscope channel propagation delay, the 50% trigger level will be at the center line of the oscilloscope grid.



5. From the channel setup dialog (C*n*):

    - Enable **Sinx/x** interpolation and set the **Averaging** to **50** sweeps.

- Touch the **Deskew** field once to highlight it, then adjust the deskew value to move the rising edge of the trace to the center of the display.

6. Now, decrease the **Timebase** to around **20 ps/div** and once again adjust the **Deskew** value so that the 50% rising edge point is centered in time.

Repeat this procedure for each probe using the same probe tip.

Note: Before moving on to the next probe, reset Averaging to 1 sweep and turn off Sinx/x interpolation.

When QualiPHY is started the deskew values from each channel dialog are saved and stored by QPHY at the beginning of each run. However, at the end of the testing these values will be erased. By saving a panel setup it is possible to refer to the deskew values after testing has completed.

Connecting the Probes

Determining Signals to Access

The required signals to probe depend up on which tests are being run in QPHY-DDR3. The tests are broken up into different “Probe Setups” to allow the user to easily see which signals are required for a particular test. You can view each of the probe setups in the Test Selector tab.

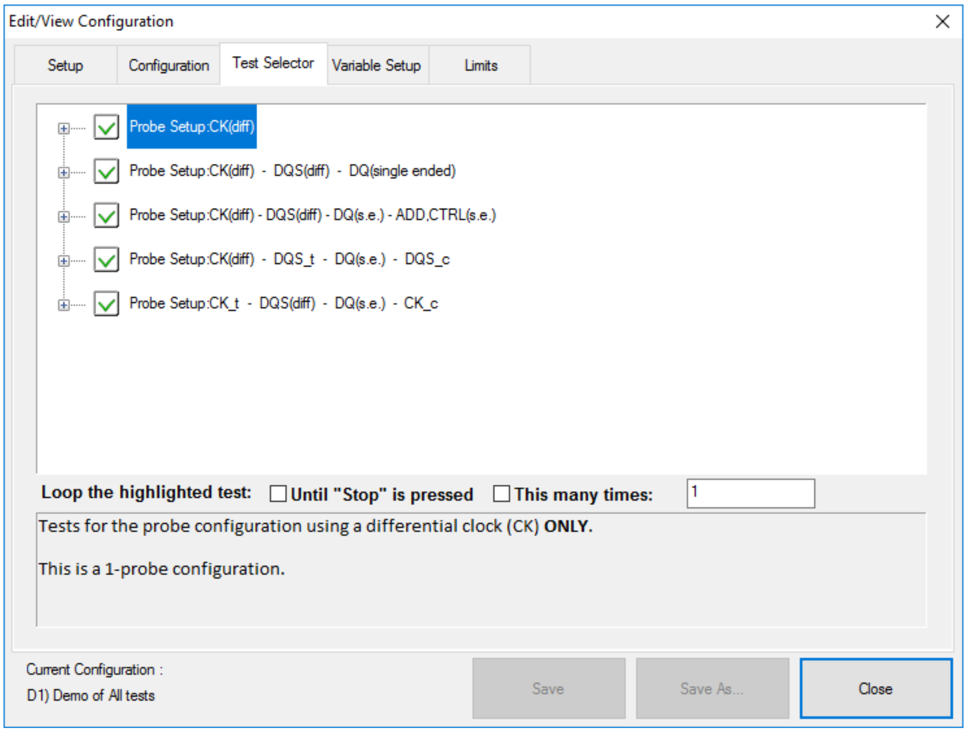


Figure 6. QPHY-DDR3 Probe Setups

Best Places to Probe

The DDR specification is defined at the balls of the DRAM so the probes should be placed as close to the DRAM as possible in order to closely follow the specification. This is important to minimize reflections on the signals. However, in some situations it can make sense to place the probes as close to the controller as possible. For example, if the user is a controller designer and is only interested in verifying the performance of the controller. It should be noted that some of the limits may not be applicable in this scenario.

One of the most desirable locations for probing is at the back side of the vias. This will generally result in good signal integrity; however, these may not always be accessible. Another alternative is to use an interposer such as the ones available from Nexus Technologies. No matter where the probes are placed it is essential to ensure that the probing points are equidistant from the DRAM. This will ensure that there is no additional skew introduced for timing measurements.

Read (R) and Write (W) Burst Requirements

R/W Burst Detection

QPHY-DDR3 separates R and W burst depending upon the skew between the data (DQ) and strobe (DQS) signals. For a W burst, QPHY expects to see that the DQ and DQS signals are approximately a quarter cycle out of phase. For an R burst, QPHY expects that the DQ and DQS signals are in phase.

R/W Burst Generation

It is recommended to capture a minimum of 10 R and 10 W bursts during each acquisition, but for greater statistical significance, it is encouraged to capture more. Programs which can communicate with the DRAM and controller are widely available online. One example is Memtest86+, which is available for download from memtest.org. When using Memtest, it is recommended to use test mode 7, which will randomly generate both R and W bursts. Additionally, a custom program can be used to stimulate the DUT.

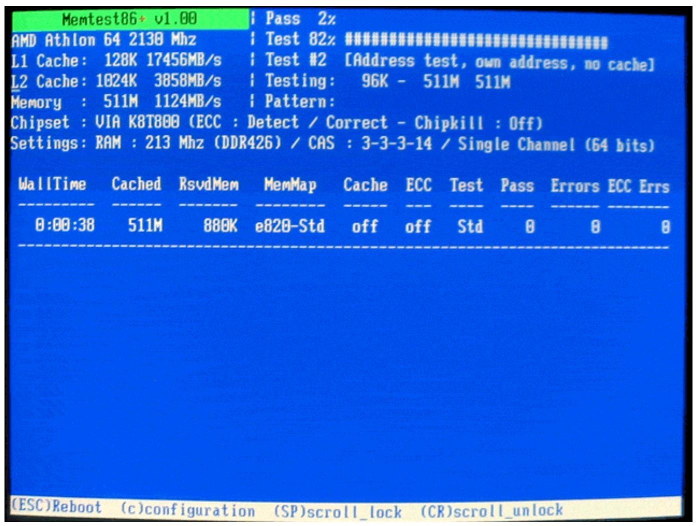


Figure 7. Memtest86+

Initial Signal Checking

Before running QPHY-DDR3, check the signals to verify that they make sense. This section covers some of the basic things which should be verified by the operator before running QPHY-DDR3.

Expected Channels

By default, QPHY-DDR3 expects to see the Clock (CK) on CH1, Strobe (DQS) on CH2 and Data (DQ) on CH3. This is what is shown in the connection diagram. The Input Channel variable can always be used to modify any of these channel assignments

Signal Amplitude

For best results, it is recommended that the signals take up 80% of the vertical grid.

Clock Frequency

By applying the Frequency measurement parameter to the CK signal, the user can verify that the DDR system is running at the expected transfer rate (Transfer Rate =Frequency * 2). This will also help in the limit selection. Do a quick visual inspection to ensure that the signal does not have any non-monotonic edges due to reflections.

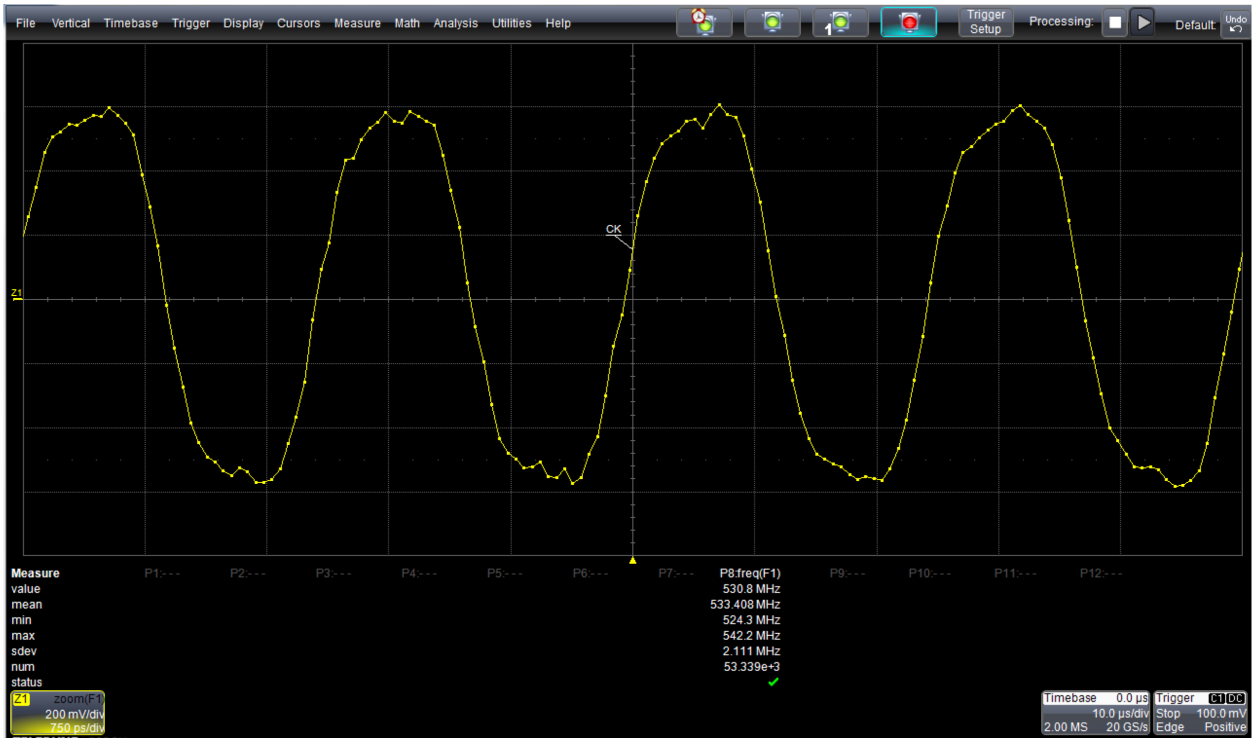


Figure 8. Verification of CK signal

Presence of R/W Burst

The operator should do a quick check to make sure their device is outputting the expected bursts. As a general rule of thumb, during a R burst DQ and DQS should be in phase and during a W burst DQ and DQS should be a quarter cycle out of phase. Additionally, the signal amplitude can be used to determine the presence of R and W bursts. If probing at the memory, R bursts will have a larger amplitude than W bursts.

Check Idle Levels

Before running QPHY-DDR3, validate the signal idle levels. Signal idle levels that are off will have an impact on the R/W burst detection, electrical, and timing measurements. DQS should have an idle level of ~ 0 mV. DQ should have an idle level of ~ VDD/2 (750 mV for DDR3).

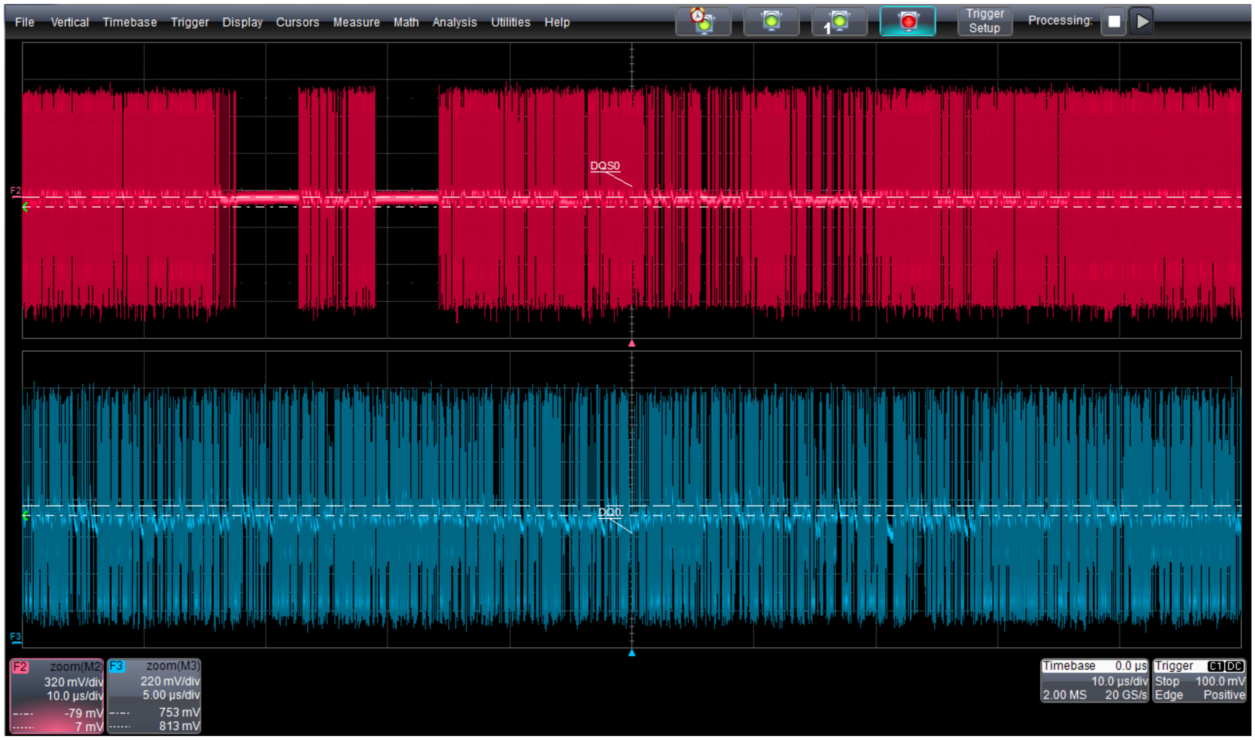


Figure 9. Verification of Idle Levels

QPHY-DDR3 Test Configurations

Test configurations include variable settings, limit sets, and test selections. See QPHY-DDR3 Variables for a description of each variable and its default value.

Standard CK and 3 probe tests for DDR3-1333

This configuration will run all of the clock tests and all tests on read and write bursts in which three probes are required. A probe must be connected to the differential clock, the differential strobe, and the single-ended data. All variables are set to their defaults. The limit set in use is DDR3-1333.

Standard CK and 3 probe tests for DDR3L-1600

This configuration will run all of the clock tests and all tests on read and write bursts in which three probes are required. A probe must be connected to the differential clock, the differential strobe, and the single-ended data. All variables are set to their defaults. The limit set in use is DDR3L-1333.

Standard CK and 3 probe tests for LPDDR3-1866

This configuration will run all of the clock tests and all tests on read and write bursts in which three probes are required. A probe must be connected to the differential clock, the differential strobe, and the single-ended data. All variables are set to their defaults. The limit set in use is LPDDR3-1866.

Demo of All Tests

This configuration uses the saved waveforms found in the D:\Waveforms\DDR3 folder to run all the tests. All variables are set to their defaults except “Use Stored Waveforms” is set to Yes and “Use Stored Trace for Speed Grade” is set to Yes. The limit set in use is DDR3-1066.

QPHY-DDR3 Test Descriptions

These are the standard DDR3 validation tests. Each QPHY-DDR3 test configuration repeats certain groups of tests using different input signals and probe setups. The probe setups are:

1. CK(diff) — differential clock
2. CK(diff) - DQS(diff) - DQ(single ended) — differential clock, differential strobe, and single-ended data
3. CK(diff) - DQS(diff) - DQ(s.e.) - ADD,CTRL(s.e.) — differential clock, differential strobe, single-ended data, and single-ended address/control
4. CK(diff) - DQS_t - DQ(s.e.) - DQS_c — differential clock, single-ended strobe (true), single-ended data, single-ended strobe (compliment)
5. CK_t - DQS(diff) - DQ(s.e.) - CK_c — single-ended clock (true), differential strobe, single-ended data, single-ended clock(compliment)
6. VREF(single ended) — single-ended VREF

The descriptions below indicate by number for which probe setups a test may be performed.

Clock Tests

The tests in this configuration are performed using probe setup 1.

tCK(avg), Average Clock Period
tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

tCK(abs), Absolute Clock Period
tCK(abs) is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge.

tCH(avg), Average High Pulse Width
tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

tCL(avg), Average Low Pulse Width
tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

tCH(abs), Absolute High Pulse Width
tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.

tCL(abs), Absolute Low Pulse Width
tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.

tJIT(duty), Half Period Jitter
tJIT(duty) is defined as the cumulative set of tCH jitter and tCL jitter over 200 consecutive cycles. tCH jitter is the largest deviation of any single tCH from tCH(avg) and tCL jitter is the largest deviation of any single tCL from tCL(avg).

tJIT(duty) = Min/max of {tJIT(CH), tJIT(CL)} where, tJIT(CH) = {tCHi - tCH(avg) where i=1 to 200} and tJIT(CL) = {tCLi - tCL(avg) where i=1 to 200}

tJIT(per), Clock Period Jitter

tJIT(per) is defined as the largest deviation of any signal tCK from tCK(avg).

tJIT(per) = Min/max of {tCKi - tCK(avg) where i = 1 to 200}.

tJIT(cc), Cycle to Cycle Period Jitter

tJIT(cc) is defined as the absolute difference in clock period between two consecutive clock cycles.

tJIT(cc) = Max of |{tCKi +1 - tCKi}|.

At the completion of the tCK, tCH, tCL, tJIT(duty), tJIT(per), and tJIT(cc) testsm the oscilloscope is in the following state:

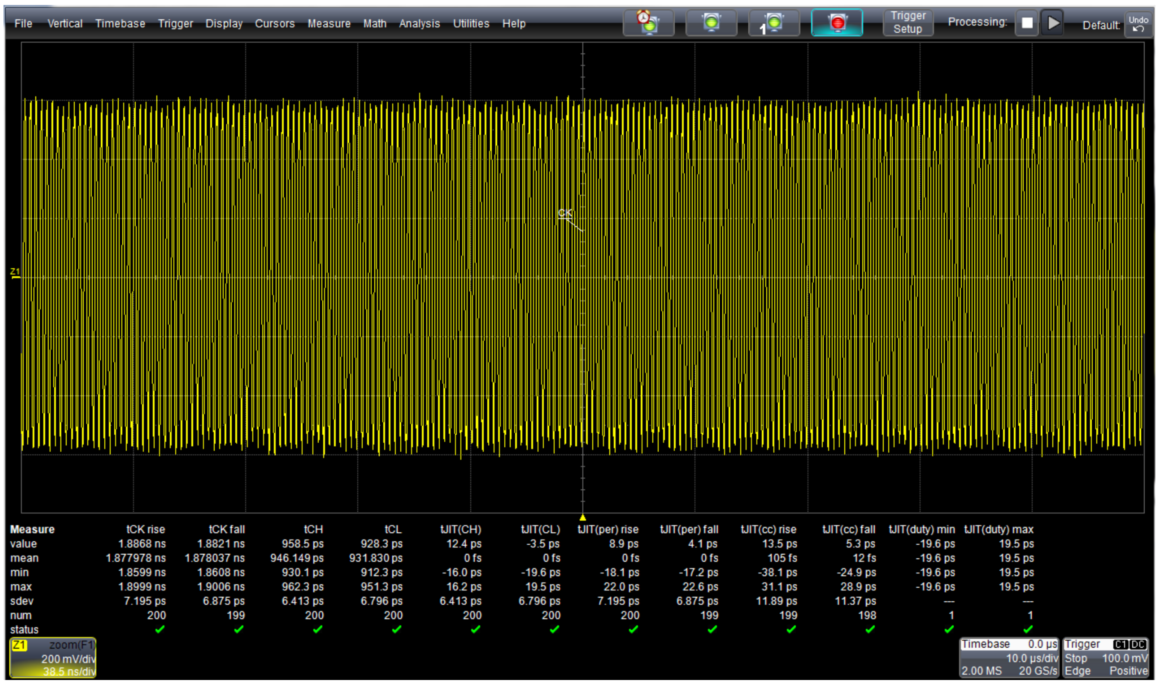


Figure 10. Clock Jitter test

Shown on this screen: Z1 is a zoom of the differential clock signal.

In the Measure table:

- **tCK rise** (P1) is the period measurement at Vref (0 mV) of Z1 (differential clock signal) on only the rising edges. The mean value is the measured value for **tCK(avg), rise**. The minimum value is the measured value for **tCK(abs), rise, min** reported in mtCK(avg). The maximum value is the measured value for **tCK(abs), rise, max** reported in mtCK(avg).
- **tCK fall** (P2) is the period measurement at Vref (0 mV) of Z1 (differential clock signal) on only the falling edges. The mean value is the measured value for **tCK(avg), fall**. The minimum value is the measured value for **tCK(abs), fall, min** reported in mtCK(avg). The maximum value is the measured value for **tCK(abs), fall, max** reported in mtCK(avg).
- **tCH** (P3) is the width measure at Vref (0 mV) of Z1 (differential clock signal) on only the high pulses. The mean value is the measured value for **tCH(avg)** reported in mtCK(avg). The minimum value is the measured value for **tCH(abs), min** reported in mtCK(avg).
- **tCL** (P4) is the width measure at Vref (0 mV) of Z1 (differential clock signal) on only the low pulses. The mean value is the measured value for **tCL(avg)** reported in mtCK(avg). The minimum value is the measured value for **tCL(abs), min** reported in mtCK(avg).
- **tJIT(CH)** (P5) subtracts the mean of P3 (tCH(avg)) from all of the tCH values. The minimum value is the measured value for **tJIT(CH), min** and the maximum value is the measured value for **tJIT(CH), max**.
- **tJIT(CL)** (P6) subtracts the mean of P4 (tCL(avg)) from all of the tCL values. The minimum value is the measured value for **tJIT(CL), min** and the maximum value is the measured value for **tJIT(CL), max**.
- **tJIT(per) rise** (P7) subtracts the mean of P1 (tCK(avg), rise) from all of the tCK rise values. The minimum value is the measured value for **tJIT(per)rise, min** and the maximum value is the measured value for **tJIT(per)rise, max**.
- **tJIT(per) fall** (P8) subtracts the mean of P2 (tCK(avg), fall) from all of the tCK fall values. The minimum value is the measured value for **tJIT(per)fall, min** and the maximum value is the measured value for **tJIT(per)fall, max**.
- **tJIT(cc) rise** (P9) takes the difference between the clock period of two consecutive cycles for only the rising edge. The absolute value of the maximum deviation between any two consecutive clock cycles is the measured value for **tJIT(cc)rise**.
- **tJIT(cc) fall** (P10) takes the difference between the clock period of two consecutive cycles for only the falling edge. The absolute value of the maximum deviation between any two consecutive clock cycles is the measured value for **tJIT(cc)fall**.
- **tJIT(duty) min** (P11) is the minimum value of the difference between minimum tCH/tCL clock period and the average tCH/tCL. This is the measured value for **tJIT(duty), min** in mUI.
- **tJIT(duty) max** (P12) is the maximum value of the difference between minimum tCH/tCL clock period and the average tCH/tCL. This is the measured value for **tJIT(duty), min** in mUI.

tERR(n Per), Cumulative Error

tERR(n Per) is defined as the cumulative error across n multiple clock cycles from tCK(avg).

There are 12 different tests: tERR(2per), tERR (3per), tERR (4per), tERR (5per), tERR(6per), tERR (7per), tERR (8per), tERR (9per), tERR (10per), tERR (11per), tERR (12per), tERR (13-50per)

Note: Only tERR(2per), tERR (3per), tERR (4per), and tERR (5per) will be discussed below. The setup for all tERR(n per) tests is exactly the same.

After the completion of the tERR(2per), tERR (3per), tERR (4per), and tERR (5per) tests the oscilloscope is in the following state:

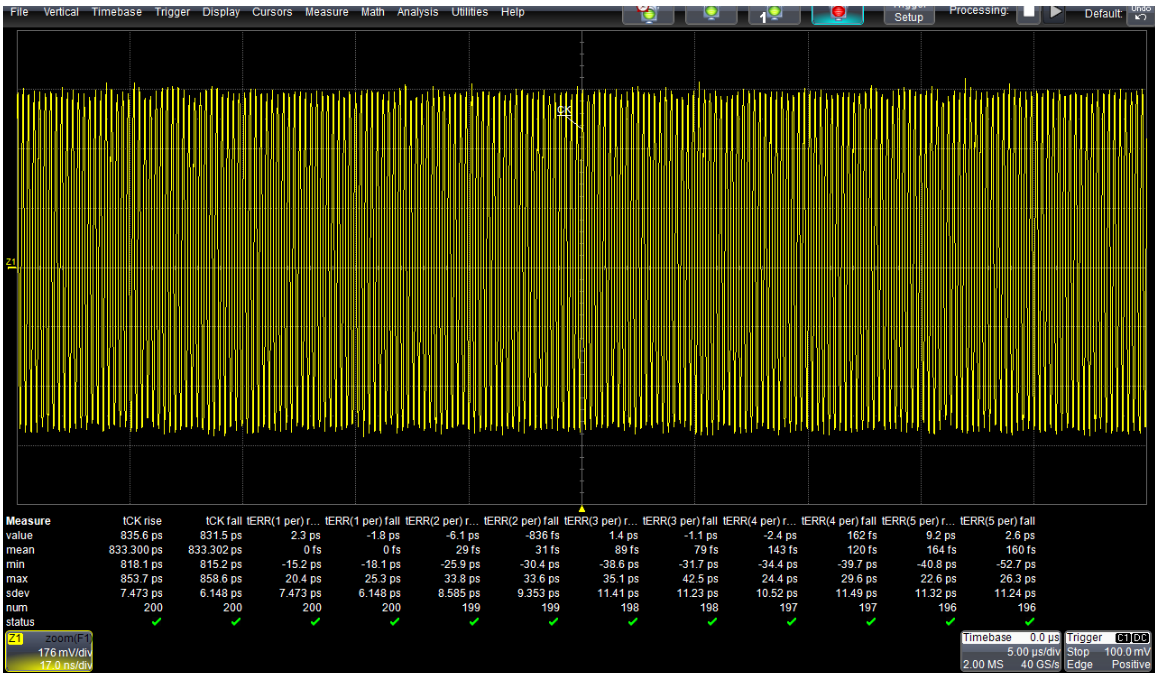


Figure 11. Clock Cumulative Error test

Shown on this screen: Z1 is a zoom of the differential clock signal.

In the Measure table:

- **tCK rise** (P1) is the period measurement at Vref (0 mV) of Z1 (differential clock signal) on only the rising edges. This value is used for the tERR calculation on the rising edge.
- **tCK fall** (P2) is the period measurement at Vref (0 mV) of Z1 (differential clock signal) on only the falling edges. This value is used for the tERR calculation on the rising edge.
- **tERR(1 per) r** (P3) is the TIE measure at Vref (0 mV) of Z1 (differential clock signal) on only the rising edges (positive pulses). It is set up to measure edges at intervals of 1. This is reported as informational only.
- **tERR(1 per) fall** (P4) is the TIE measure at Vref (0 mV) of Z1 (differential clock signal) on only the falling edges (negative pulses). It is set up to measure edges at intervals of 1. This is reported as informational only.
- **tERR(2 per) r** (P5) is the TIE measure at Vref (0 mV) of Z1 (differential clock signal) on only the rising edges (positive pulses). It is set up to measure edges at intervals of 2. The minimum value is measured as **tERR(2per)rise, min** reported in mUI and the maximum value is measured as **tERR(2per)rise, max** reported in mUI.

- **tERR(2 per) fall** (P6) is the TIE measure at Vref (0 mV) of Z1 (differential clock signal) on only the falling edges (negative pulses). It is set up to measure edges at intervals of 2. The minimum value is measured as **tERR(2per)fall, min** reported in mUI and the maximum value is measured as **tERR(2per)fall, max** reported in mUI.
- **tERR(3 per) r** (P7) is the TIE measure at Vref (0 mV) of Z1 (differential clock signal) on only the rising edges (positive pulses). It is set up to measure edges at intervals of 3. The minimum value is measured as **tERR(3per)rise, min** reported in mUI and the maximum value is measured as **tERR(3per)rise, max** reported in mUI.
- **tERR(3 per) fall** (P8) is the TIE measure at Vref (0 mV) of Z1 (differential clock signal) on only the falling edges (negative pulses). It is set up to measure edges at intervals of 3. The minimum value is measured as **tERR(3per)fall, min** reported in mUI and the maximum value is measured as **tERR(3per)fall, max** reported in mUI.
- **tERR(4 per) r** (P9) is the TIE measure at Vref (0 mV) of Z1 (differential clock signal) on only the rising edges (positive pulses). It is set up to measure edges at intervals of 4. The minimum value is measured as **tERR(4per)rise, min** reported in mUI and the maximum value is measured as **tERR(4per)rise, max** reported in mUI.
- **tERR(4 per) fall** (P10) is the TIE measure at Vref (0 mV) of Z1 (differential clock signal) on only the falling edges (negative pulses). It is set up to measure edges at intervals of 4. The minimum value is measured as **tERR(4per)fall, min** reported in mUI and the maximum value is measured as **tERR(4per)fall, max** reported in mUI.
- **tERR(5 per) r** (P11) is the TIE measure at Vref (0 mV) of Z1 (differential clock signal) on only the rising edges (positive pulses). It is set up to measure edges at intervals of 5. The minimum value is measured as **tERR(5per)rise, min** reported in mUI and the maximum value is measured as **tERR(5per)rise, max** reported in mUI.
- **tERR(5 per) fall** (P12) is the TIE measure at Vref (0 mV) of Z1 (differential clock signal) on only the falling edges (negative pulses). It is set up to measure edges at intervals of 5. The minimum value is measured as **tERR(5per)fall, min** reported in mUI and the maximum value is measured as **tERR(5per)fall, max** reported in mUI.

Eye Diagram – DQ and DQS Eyes

These tests are performed on both write bursts (inputs) and read bursts (outputs) using probe setup 2. They are informational tests that create an eye diagram of all of the bursts in the acquisition. The eyes are created either using CK or DQS as the timing reference to allow for additional debugging.

Write Bursts (Inputs) – CK as Timing Reference

This test will display both the DQ and DQS eyes relative to the CK signal. This will provide insight to any skew between DQS and CK.

After the completion of Write Bursts (Inputs) – CK as Timing Reference the oscilloscope is in the following state:

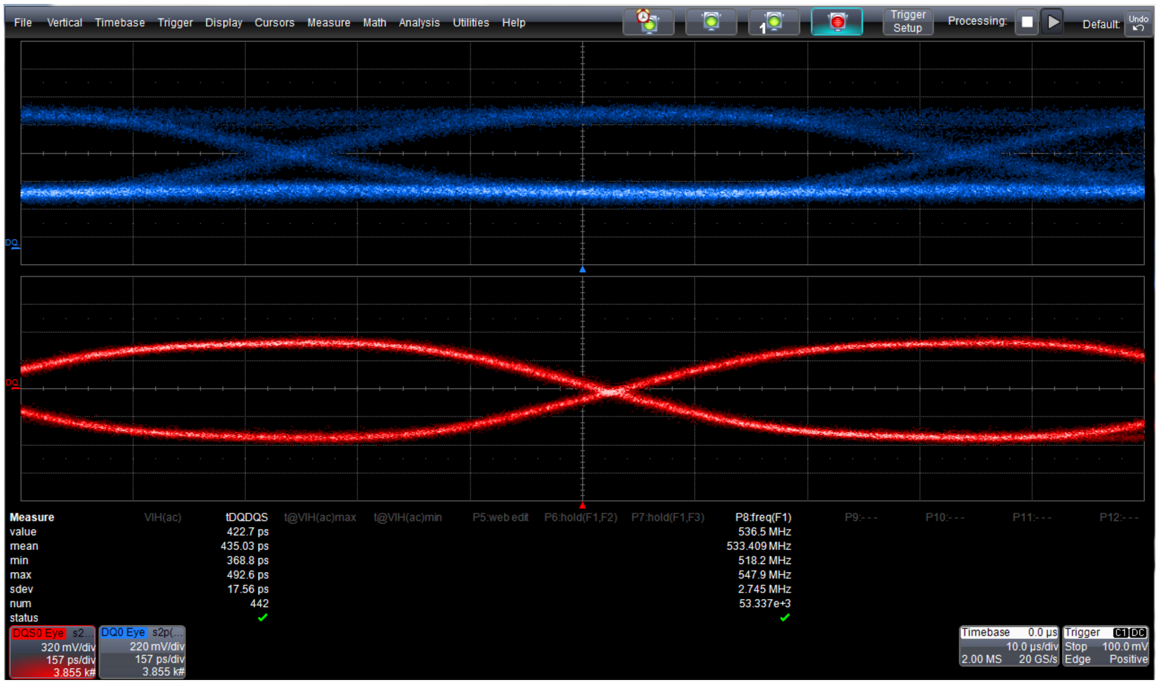


Figure 12. DQ and DQS Eye Diagrams relative to CK on Write Bursts

Shown on screen:

- F6 is the DQS eye diagram of the W bursts from the acquired signal. CK is used as the timing reference for this test and any skew between DQS and CK can be seen by comparing the crossing location to the center of the grid. This math function is assigned an alias based on the assigned DQS signal name. The number of bits contained in the eye diagram is displayed in the bottom row of the F6 descriptor box. In this case there are 3,894 DQS bits in the eye.
- F7 is the DQ eye diagram of the W bursts from the acquired signal. This math function is assigned an alias based on the assigned DQ signal name. The number of bits contained in the eye diagram is displayed in the bottom row of the F7 descriptor box. In this case there are 3,894 DQ bits in the eye.

In the Measure table:

- **tDQDQS** (P2) is measuring the skew between DQ and DQS. Since this measurement is performed once per burst, this shows how many W bursts were in the acquired waveform.
- **freq(F1)** is measuring the frequency of the differential clock signal.

Write Bursts (Inputs) – DQS as Timing Reference

This test will display both the DQ and DQS eyes relative to the DQS signal. This will provide insight to any skew between DQ and DQS.

After the completion of Write Bursts (Inputs) – DQS as Timing Reference the oscilloscope is in the following state:

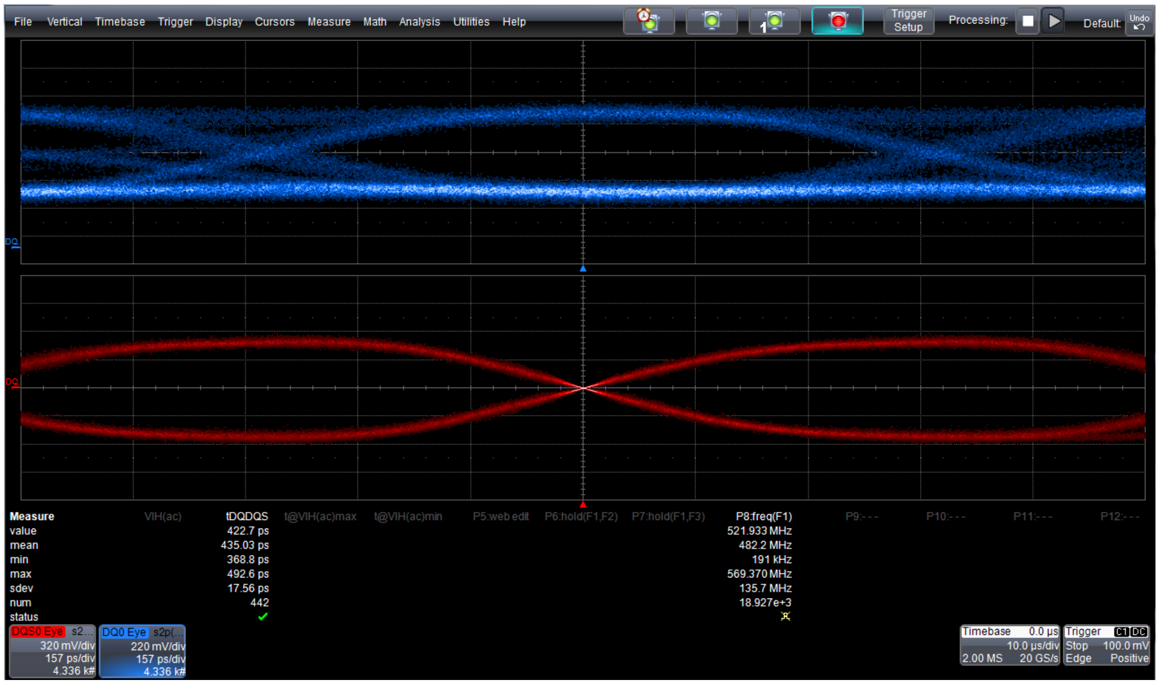


Figure 13. DQ and DQS Eye Diagrams relative to DQS on Write Bursts

Shown on this screen:

- F6 is the **DQS Eye** diagram of the W bursts from the acquired signal. DQS is used as the timing reference for this test which causes the eye to come to a "pin point" on the center grid. This math function is assigned an alias based on the assigned DQS signal name. The number of bits contained in the eye diagram is displayed in the bottom row of the F6 descriptor box. In this case there are 3,894 DQS bits in the eye.
- F7 is the **DQ Eye** diagram of the W bursts from the acquired signal. This math function is assigned an alias based on the assigned DQ signal name. The number of bits contained in the eye diagram is displayed in the bottom row of the F7 descriptor box. In this case there are 3,894 DQ bits in the eye.

In the Measure table:

- **tDQDQS** (P2) is measuring the skew between DQ and DQS. Since this measurement is performed once per burst, this shows how many W bursts were in the acquired waveform.
- **freq(F1)** is measuring the frequency of the differential clock signal.

Read Bursts (Outputs) – CK as Timing Reference

This test will display both the DQ and DQS eyes relative to the CK signal. This will provide insight to any skew between DQS and CK.

After the completion of Read Bursts (Outputs) – CK as Timing Reference the oscilloscope is in the following state:

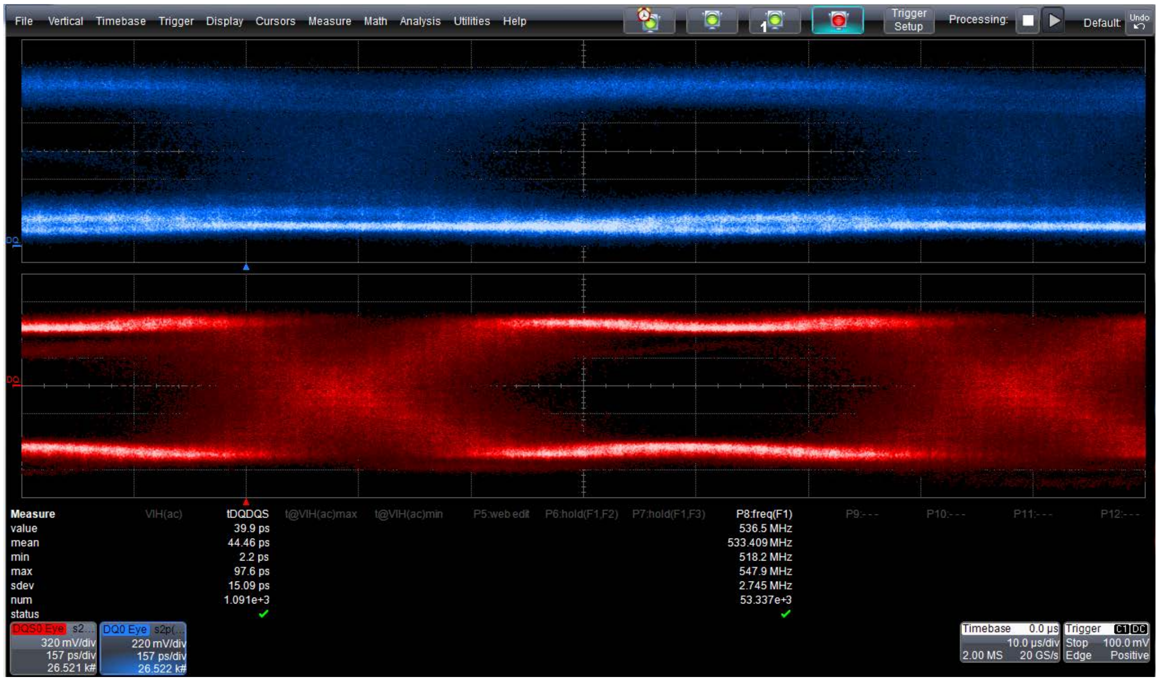


Figure 14. DQ and DQS Eye Diagrams relative to CK on Read Bursts

Shown on this screen:

- F6 is the **DQS Eye** diagram of the R bursts from the acquired signal. CK is used as the timing reference for this test. This math function is assigned an alias based on the assigned DQS signal name. The number of bits contained in the eye diagram is displayed in the bottom row of the F6 descriptor box. In this case there are 26,513 DQS bits in the eye.
- F7 is the **DQ Eye** diagram of the R bursts from the acquired signal. This math function is assigned an alias based on the assigned DQ signal name. The number of bits contained in the eye diagram is displayed in the bottom row of the F7 descriptor box. In this case there are 26,513 DQ bits in the eye.

In the Measure table:

- **tDQDQS** (P2) is measuring the skew between DQ and DQS. Since this measurement is performed once per burst, this shows how many W bursts were in the acquired waveform.
- **freq(F1)** is measuring the frequency of the differential clock signal.

Read Bursts (Outputs) – DQS as Timing Reference

This test will display both the DQ and DQS eyes relative to the DQS signal. This will provide insight to any skew between DQ and DQS.

After the completion of Read Bursts (Outputs) – DQS as Timing Reference the oscilloscope is in the following state:

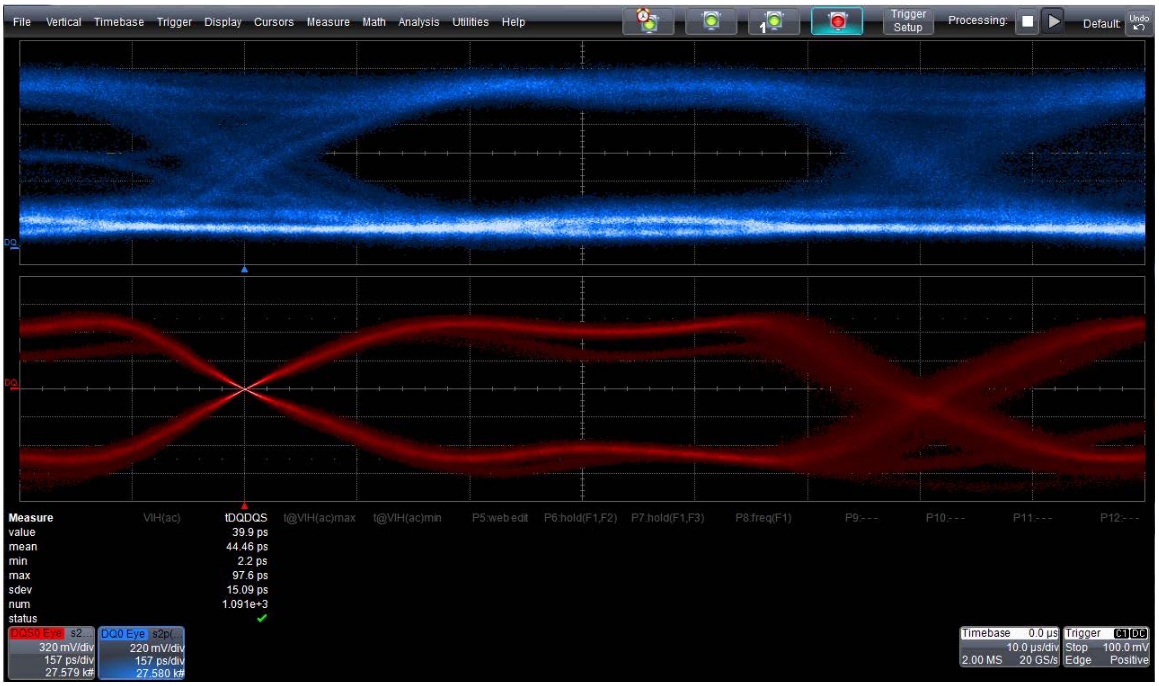


Figure 15. DQ and DQS Eye Diagrams relative to DQS on Read Bursts

Shown on this screen:

- F6 is the **DQS Eye** diagram of the R bursts from the acquired signal. DQS is used as the timing reference for this test which causes the eye to come to a "pin point" on the second division. This math function is assigned an alias based on the assigned DQS signal name. The number of bits contained in the eye diagram is displayed in the bottom row of the F6 descriptor box. In this case there are 26,489 DQS bits in the eye.
- F7 is the **DQ Eye** diagram of the R bursts from the acquired signal. This math function is assigned an alias based on the assigned DQ signal name. The number of bits contained in the eye diagram is displayed in the bottom row of the F7 descriptor box. In this case there are 26,489 DQ bits in the eye.

In the Measure table:

- **tDQDQS** (P2) is measuring the skew between DQ and DQS. Since this measurement is performed once per burst, this shows how many W bursts were in the acquired waveform.
- **freq(F1)** is measuring the frequency of the differential clock signal.

Electrical Tests on Write Bursts

These electrical tests are performed on write bursts (inputs) using the probe setups listed below.

SlewR/SlewF, Input Slew Rate

These tests are performed using probe setups 2, 3, and 5.

The purpose of these tests is to characterize the slew rate on all of the write bursts (input) signals. This test is performed on both rising (SlewR) and falling edges (SlewF).

- For single-ended signals SlewR is measured from Vref to VIH(ac) min and SlewF is measured from Vref to VIL(ac) max.
- For differential signals SlewR is measured from VILdiff(ac) max to VIHdiff(ac) min and SlewF is measured from VIHdiff(ac) min to VILdiff(ac) max.

Note: Only SlewR measured on DQ will be discussed below. The measurement methodology is exactly same for SlewF except VIL(ac) is used in place of VIH(ac).

After the completion of the SlewR test the oscilloscope is in the following state:

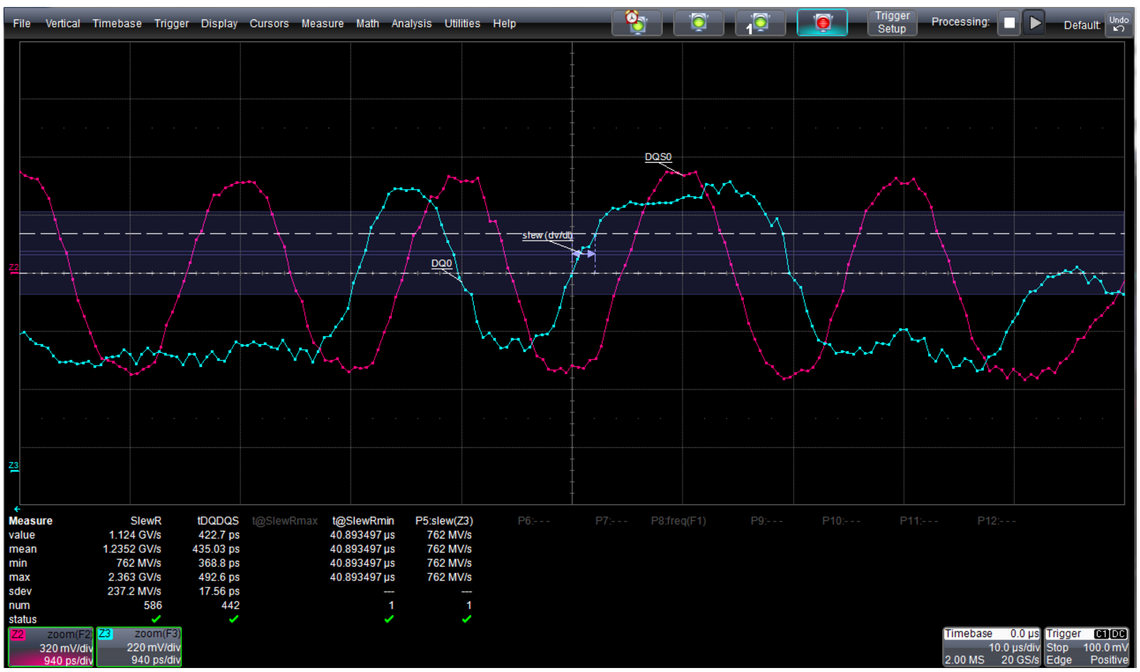


Figure 16. Electrical tests on Write Bursts

Shown on this screen:

- Z2 is a zoom of F2, the acquired DQS signal after any probe deskew has been applied. The zoom is positioned at the location of the “worst case” SlewR measurement indicated by t@SlewRmin. A trace label is applied on this trace according to the signal name assigned to DQS. This signal is not measured in this test and is only provided as a visual reference.
- Z3 is a zoom of F3, the acquired DQ signal after any probe deskew has been applied. The zoom is position at the location of the “worst case” SlewR measurement indicated by t@SlewRmin. A trace label is applied on this trace according to the signal name assigned to DQ. This is the signal which is measured in this test.

In the Measure table:

- **SlewR** (P1) is measuring the slew rate of DQ on the rising edges. The slew rate on the rising edge is measured from Vref to VIH(ac) min. The minimum value is the measured value for **SlewR of DQ min**. This test is informational only.
- **tDQDQS** (P2) is measuring the skew between DQ and DQS. Since this measurement is performed once per burst, this shows how many W bursts were in the acquired waveform.
- **t@SlewRmin** (P4) displays the location of where the minimum value of SlewR occurred. This is used to position the zoom traces at the location of the “worst case results”.
- **slew(Z3)** displays the minimum value of SlewR and is used to display the slew rate measurement markers.

VIH(ac)/VIL(ac), Differential AC input logic high/low

These tests are performed using the probe setups 2 and 3. VIH(ac) measures the local maximum value from Vref to Vref of the high pulse and VIL(ac) measures the local minimum value from Vref to Vref of the low pulse.

Note: Only VIH(ac) min will be discussed below. The measurement methodology is exactly same for VIL(ac) max except low pulses are used.

At the completion of the VIH(ac) test, the oscilloscope is in the following state:

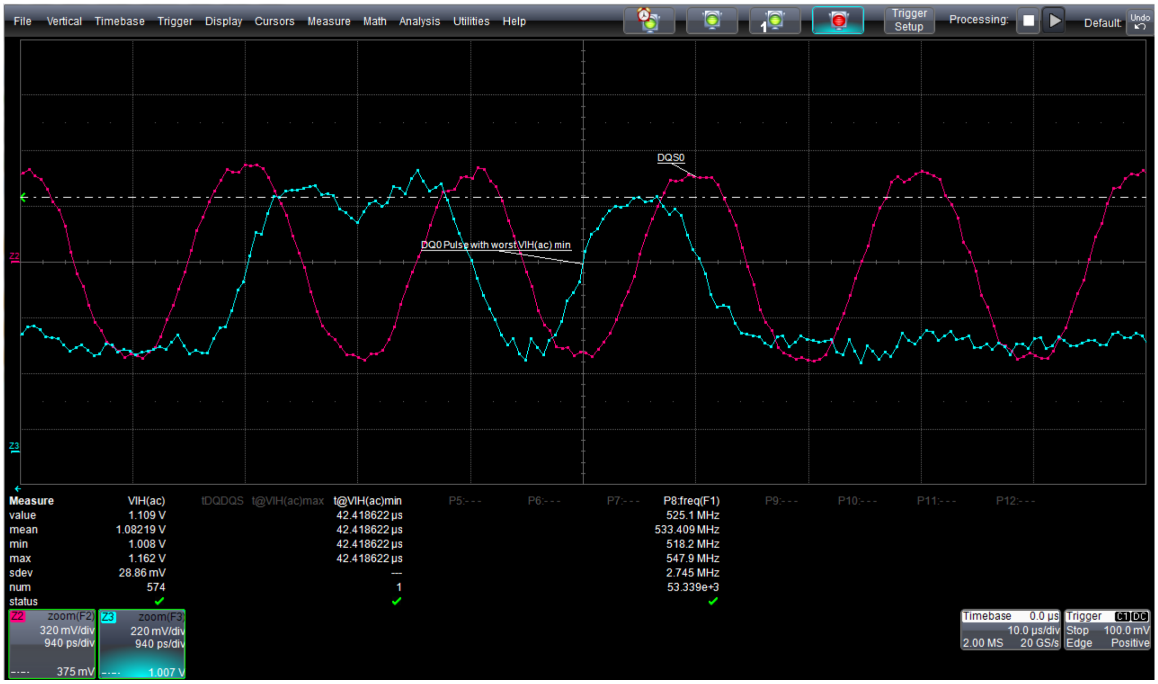


Figure 17. Differential AC Input Logic

Shown on this screen:

- Z2 is a zoom of F2, the acquired DQS signal after any probe deskew has been applied. The zoom is positioned at the location of the “worst case” VIH(ac) measurement indicated by t@VIH(ac)min. A trace label is applied on this trace according to the signal name assigned to DQS. This signal is not measured in this test and is only provided as a visual reference.
- Z3 is a zoom of F3, the acquired DQ signal after any probe deskew has been applied. The zoom is position at the location of the “worst case” VIH(ac) measurement indicated by t@VIH(ac)min. A trace label is applied on this trace according to the signal name assigned to DQ. This is the signal which is measured in this test.

In the Measure table:

- **VIH(ac)** (P1) is measuring the local minimum of DQ from Vref to Vref. The minimum value is the measured value for **VIH(ac) min**. This test is consider to be passing if the measured value is greater than Vref plus the AC level being used.
- **t@VIH(ac)min** (P4) displays the location of where the minimum value of VIH(ac) occurred. This is used to position the zoom traces at the location of the “worst case results”.
- **freq(F1)** is measuring the frequency of the differential clock signal.

Time Above AC-Level (tDVAC and tVAC)

This is a group of two tests performed using probe setup 2. The purpose is to verify the allowed time before ringback. tDVAC measures the time above VIHdiff(ac) and below VILdiff(ac) for differential inputs (DQS and CK). tVAC measures the time above VIH(ac) and below VIL(ac) for inputs. These signals are only measured when a write burst has been detected.

Note: Only tDVAC of DQS measured on above VIHdiff(ac) will be discussed below. The measurement methodology is exactly same for below VILdiff(ac). tVAC will be measured above VIHdiff(ac) rather than VIHdiff(ac) and VILdiff(ac).

After the completion of the tDVAC test the oscilloscope is in the following state:

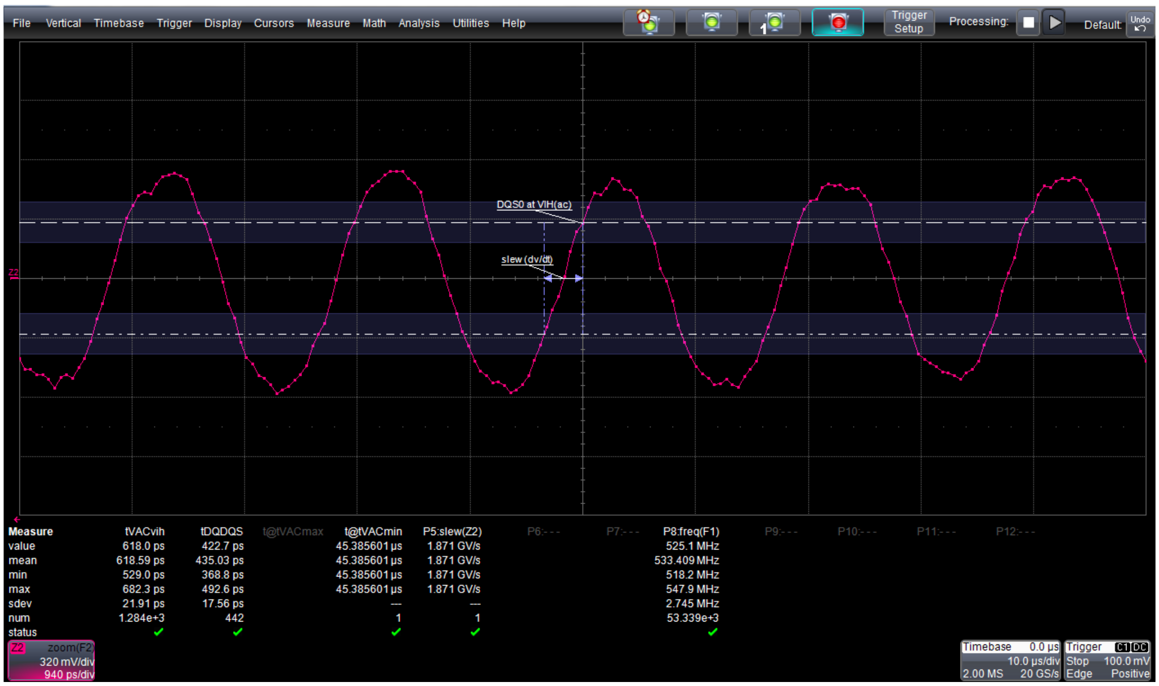


Figure 18. Time Above AC Level

Shown on this screen:

- **Z2** is a zoom of F2, the acquired DQS signal after any probe deskew has been applied. The zoom is positioned at the location of the "worst case" tDVAC measurement indicated by t@tVACmin.

In the Measure table:

- **tVACvih** (P1) is measuring the time above VIHdiff(ac) for DQS. VIHdiff(ac) is indicated by the trace label "DQS at VIH(ac)". The minimum value is the measured value for **tDVAC Pos min of DQS**. The AC level in use is captured in the report. This test is considered passing if the measured value is greater than the defined limit.
- **tDQDQS** (P2) is measuring the skew between DQ and DQS. Since this measurement is performed once per burst, this shows how many W bursts were in the acquired waveform.
- **t@tVACmin** (P4) displays the location of where the minimum value of tDVAC occurred. This is used to position the zoom traces at the location of the "worst case results".
- **Slew(Z2)** is measuring the slew rate on the rising edge of DQS at t@tVACmin from Vref to VIH(ac). This value is used to determine the appropriate limit for tDVAC.
- **freq(F1)** is measuring the frequency of the differential clock signal.

AC Over/Undershoot

This is a group of four tests performed on DQ, DQS, CK, and ADD using probe setups 2, 3, 4, and 5. The purpose is to characterize the overshoot above VDDQ and undershoot below VSSQ on DQ, DQS, and CK during W bursts. Both peak amplitude and area are tested.

Note: Only overshoot of DQ will be discussed below. The measurement methodology is exactly same for the DQS, CK, and ADD. The measurement methodology is also identical for undershoot except VSSQ is used instead of VDDQ.

Peak Amplitude

At the completion of the Overshoot Peak Amplitude test the oscilloscope is in the following state:

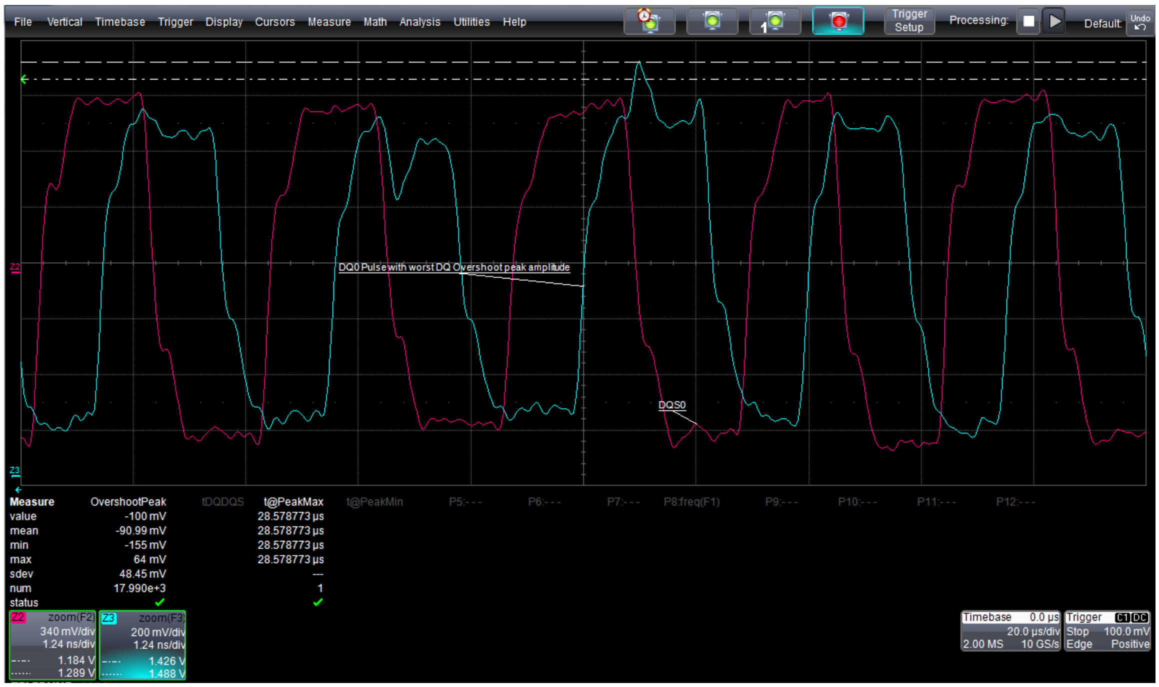


Figure 19. AC Over/Undershoot Peak Amplitude

Shown on this screen:

- Z2 is a zoom of F2, the acquired DQS signal after any probe deskew has been applied. The zoom is positioned at the location of the “worst case” Overshoot Peak Amplitude measurement indicated by t@PeakMax. This signal is not measured, it is only provided as a visual reference.
- Z3 is a zoom of F3, the acquired DQ signal after any probe deskew has been applied. The zoom is position at the location of the “worst case” Overshoot Peak Amplitude measurement indicated by t@PeakMax. A trace label is applied on this trace on the pulse with the worst overshoot peak amplitude. This is the signal that is measured in this test.

In the Measure table:

- **OvershootPeak** (P1) is measuring the overshoot peak amplitude above VDDQ for of each DQ pulse. The VDDQ level is indicated by alternating dashed cursor and the peak amplitude level is indicator by the other cursor. The peak amplitude is measured only 1 UI after a transition. If the peak value does not exceed VDDQ, the measured value will return a negative result. The maximum value is the measured value for **DQ Overshoot peak amplitude Max**. This test is considered passing if the measured value is less than 400 mV.
- **t@PeakMax** (P3) displays the location of where the maximum value of OvershootPeak occurred. This is used to position the zoom traces at the location of the “worst case results”.

Area

At the completion of the Overshoot Area test, the oscilloscope is in the following state:

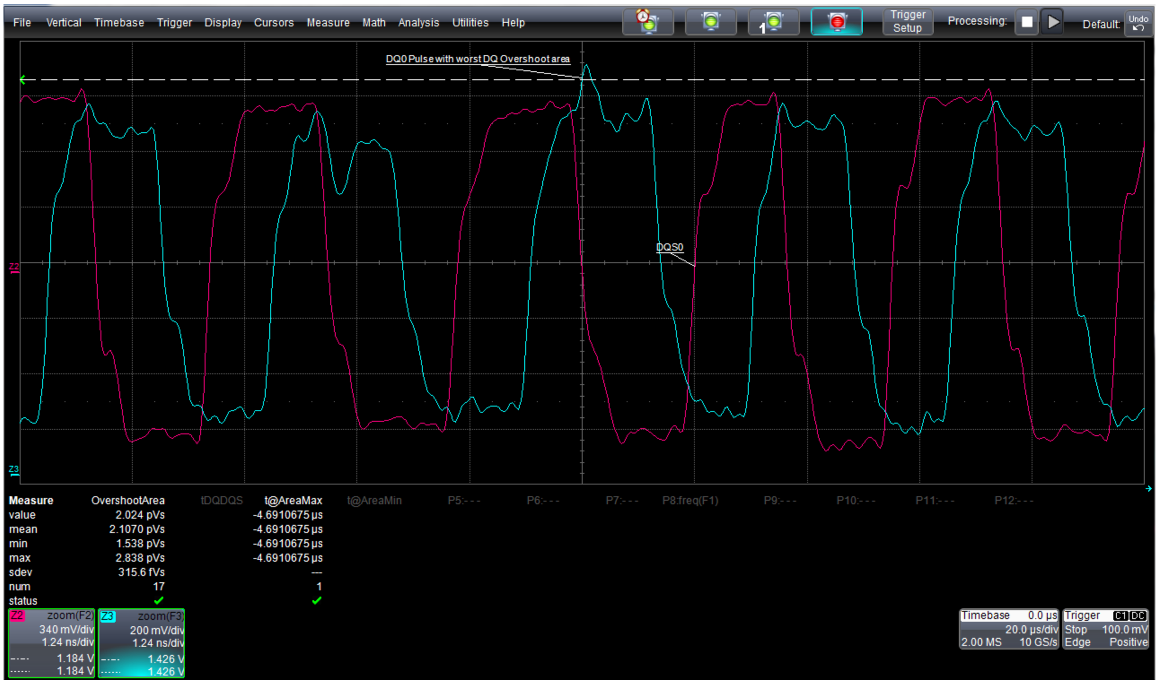


Figure 20. AC Over/Undershoot Area

Shown on this screen:

- Z2 is a zoom of F2, the acquired DQS signal after any probe deskew has been applied. The zoom is positioned at the location of the “worst case” Overshoot Area measurement indicated by t@AreaMax. A trace label is applied on this trace according to the signal name assigned to DQS. This signal is not measured in this test and is only provided as a visual reference.
- Z3 is a zoom of F3, the acquired DQ signal after any probe deskew has been applied. The zoom is position at the location of the “worst case” Overshoot Area measurement indicated by t@AreaMax. A trace label is applied on this trace according to the signal name assigned to DQ. This is the signal which is measured in this test.

In the Measure table:

- **OvershootArea** (P1) is measuring the overshoot peak amplitude above VDDQ for of each DQ pulse. The VDDQ level is indicated the cursor. The peak amplitude is measured only 1 UI after a transition. The maximum value is the measured value for **DQ Overshoot area Max**. This test is considered passing if the measured value is less than the specified limit.
- **t@AreaMax** (P3) displays the location of where the maximum value of OvershootArea occurred. This is used to position the zoom traces at the location of the “worst case results”.

VSWING(MAX), Input Signal Maximum Peak to Peak Swing

This test is performed using probe setup 3. The purpose of this test is to characterize the maximum peak to peak swing on the ADD/CTRL signal.

At the completion of the VSWING test, the oscilloscope is in the following state:

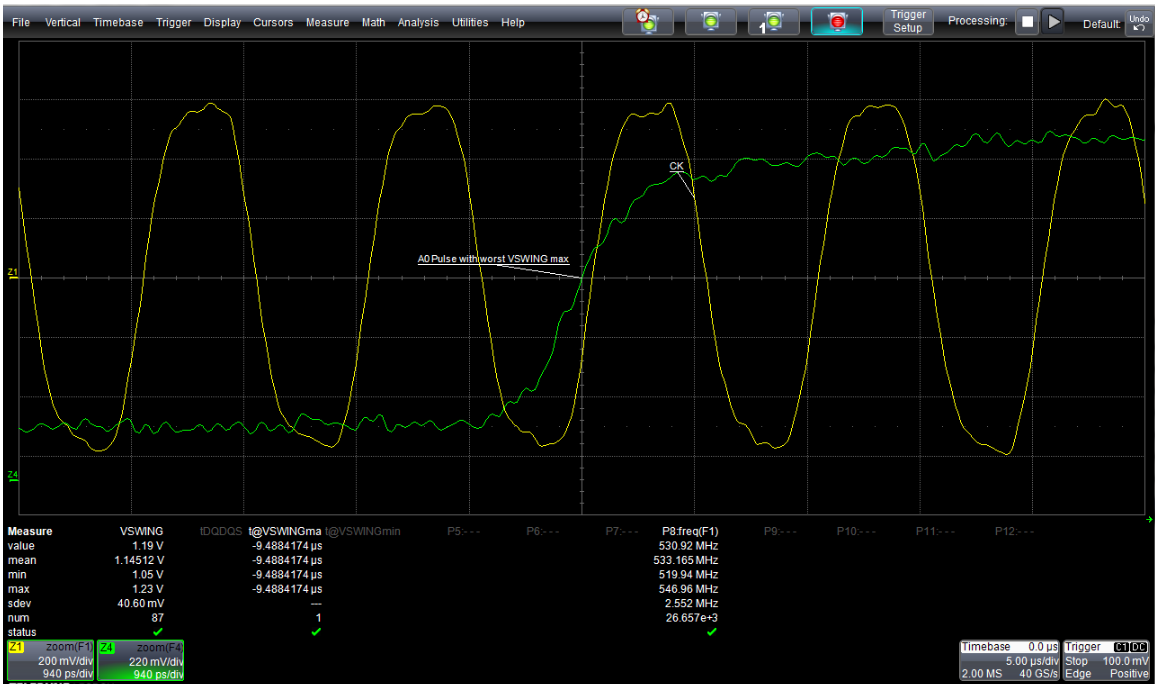


Figure 21. Maximum Peak to Peak Swing

Shown on this screen:

- Z1 is a zoom of F1, the acquired CK signal after any probe deskew has been applied. The zoom is positioned at the location of the "worst case" VSWING measurement indicated by t@VSWINGma. A trace label is applied on this trace according to the signal name assigned to CK. This signal is not measured in this test and is only provided as a visual reference.
- Z4 is a zoom of F4, the acquired ADD signal after any probe deskew has been applied. The zoom is position at the location of the "worst case" VSWING measurement indicated by t@ VSWINGma. A trace label is applied on this trace according to the signal name assigned to ADD. This is the signal which is measured in this test.

In the Measure table:

- **VSWING** (P1) is measuring the peak to peak swing of each ADD/CTRL pulse. This is taking the difference of VIH(ac) and VIL(ac). The maximum value is the measured value for **VSWING Max**. This test is informational only and is measured using the legacy method from DDR2
- **t@VSWINGma** (P3) displays the location of where the maximum value of VSWING occurred. This is used to position the zoom traces at the location of the "worst case results".
- **freq(F1)** is measuring the frequency of the differential clock signal.

VSEH(ac)min/VSEL(ac)max, Single-ended AC high/low level

This test is performed using probe setups 4 and 5. VSEH(ac) measures the local minimum value from Vref to Vref of the high pulse and VIL(ac) measures the local maximum value from Vref to Vref of the low pulse. This is equivalent to VIH(ac)/VIL(ac) for single-ended signals.

Note: Only VSEH(ac) min will be discussed below. The measurement methodology is exactly same for VSEL(ac) max except low pulses are used.

After the completion of the VSEH(ac) test, the oscilloscope is in the following state:

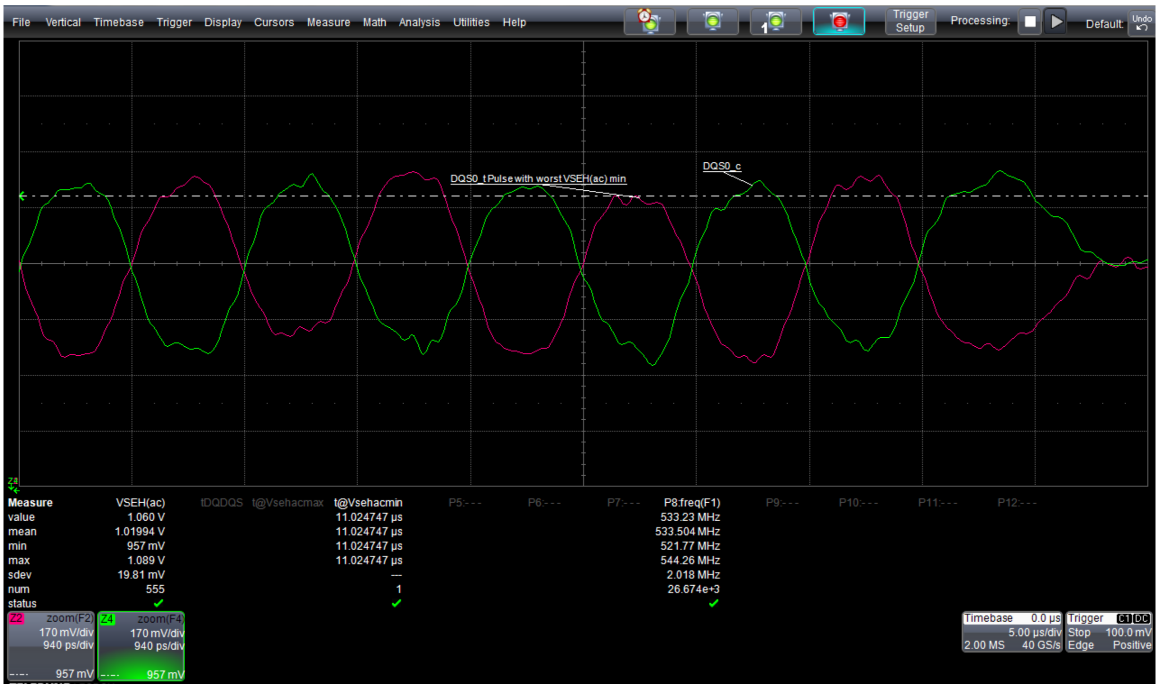


Figure 22. Single-ended AC High/Low Level

Shown on this screen:

- Z2 is a zoom of F2, the acquired DQS_t signal after any probe deskew has been applied. The zoom is positioned at the location of the “worst case” VSEH(ac) measurement indicated by t@Vsehacmin. A trace label is applied on this trace according to the signal name assigned to DQS_t. This is the signal which is measured in this test.
- Z4 is a zoom of F4, the acquired DQS_c signal after any probe deskew has been applied. The zoom is position at the location of the “worst case” VSEH(ac) measurement indicated by t@Vsehacmin. A trace label is applied on this trace according to the signal name assigned to DQS_c. This signal is not measured in this test and is only provided as a visual reference.

In the Measure table:

- **VSEH(ac) (P1)** is measuring the local minimum of DQS_t from Vref to Vref. The minimum value is the measured value for VSEH(ac) Min DQS_t. This test is consider to be passing if the measured value is greater than Vref plus the AC level being used.
- **t@VIH(ac)min (P4)** displays the location of where the minimum value of VIH(ac) occurred. This is used to position the zoom traces at the location of the “worst case results”.
- **freq(F1)** is measuring the frequency of the differential clock signal.

VIX(ac), AC Differential Input Cross Point Voltage

This test is performed using probe setups 4 and 5. The purpose of this test is to characterize the differential input cross point voltage. VIX(ac) measures the voltage at which differential input signals cross. The typical value of VIX(ac) is expected to be about 0.5 x VDDQ of the transmitting device. Both the minimum and maximum values are measured.

At the completion of the VIX(ac) test, the oscilloscope is in the following state:

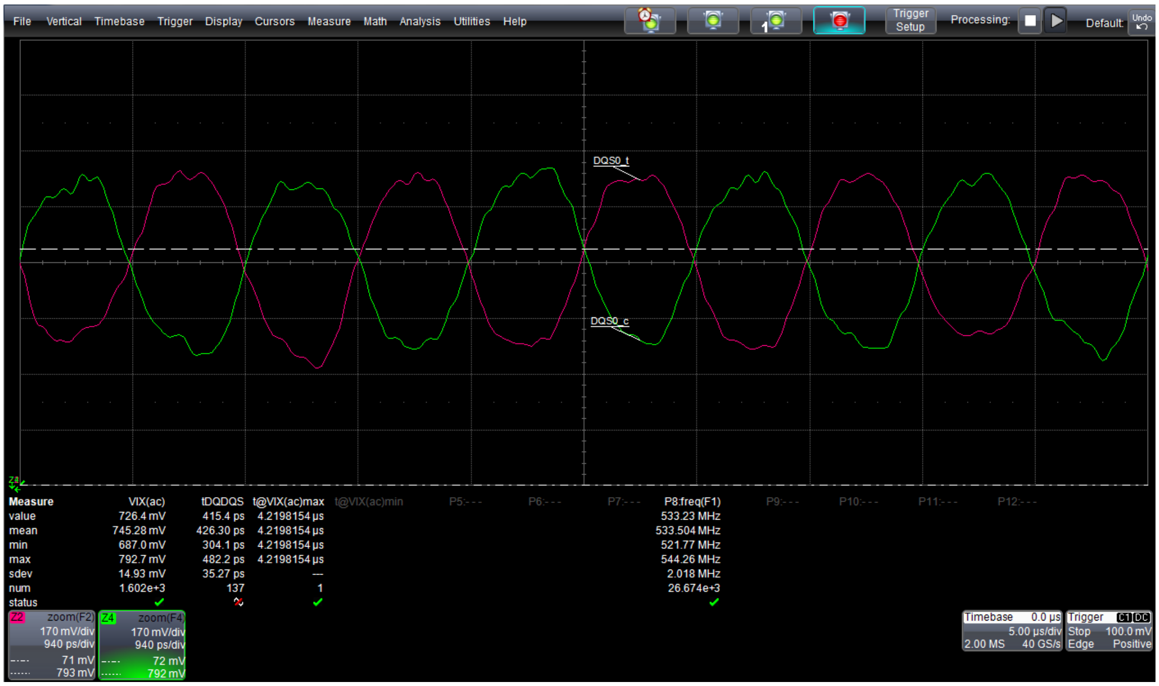


Figure 23. AC Differential Input Cross Point Voltage

Shown on this screen:

- Z2 is a zoom of F2, the acquired DQS_t signal after any probe deskew has been applied. The zoom is positioned at the location of the “worst case” VIX(ac) measurement indicated by t@VIX(ac)max. A trace label is applied on this trace according to the signal name assigned to DQS_t.
- Z4 is a zoom of F4, the acquired DQS_c signal after any probe deskew has been applied. The zoom is position at the location of the “worst case” VIX(ac) measurement indicated by t@VIX(ac)max. A trace label is applied on this trace according to the signal name assigned to DQS_c.

In the Measure table:

- **VIX(ac) (P1)** is measuring the voltage at which DQS_t and DQS_c intersect. The maximum value is the measured value for VIX(ac) max.
- **tDQDQS (P2)** is measuring the skew between DQ and DQS. Since this measurement is performed once per burst, this shows how many W bursts were in the acquired waveform.
- **t@VIX(ac)min (P3)** displays the location of where the maximum value of VIX(ac) occurred. This is used to position the zoom traces at the location of the “worst case results”.
- **freq(F1)** is measuring the frequency of the differential clock signal.

Electrical Tests on Read Bursts

VOH(ac)/VOL(ac), Differential AC output logic high/low

These tests are performed using the probe setup 2. VOH(ac) measures the local maximum and minimum value from Vref to Vref of the high pulse and VOL(ac) measures the local maximum and minimum value from Vref to Vref of the low pulse.

Note: Only VOH(ac) will be discussed below. The measurement methodology is exactly same for VOL(ac) except low pulses are used.

At the completion of the VOH(ac) test, the oscilloscope is in the following state:

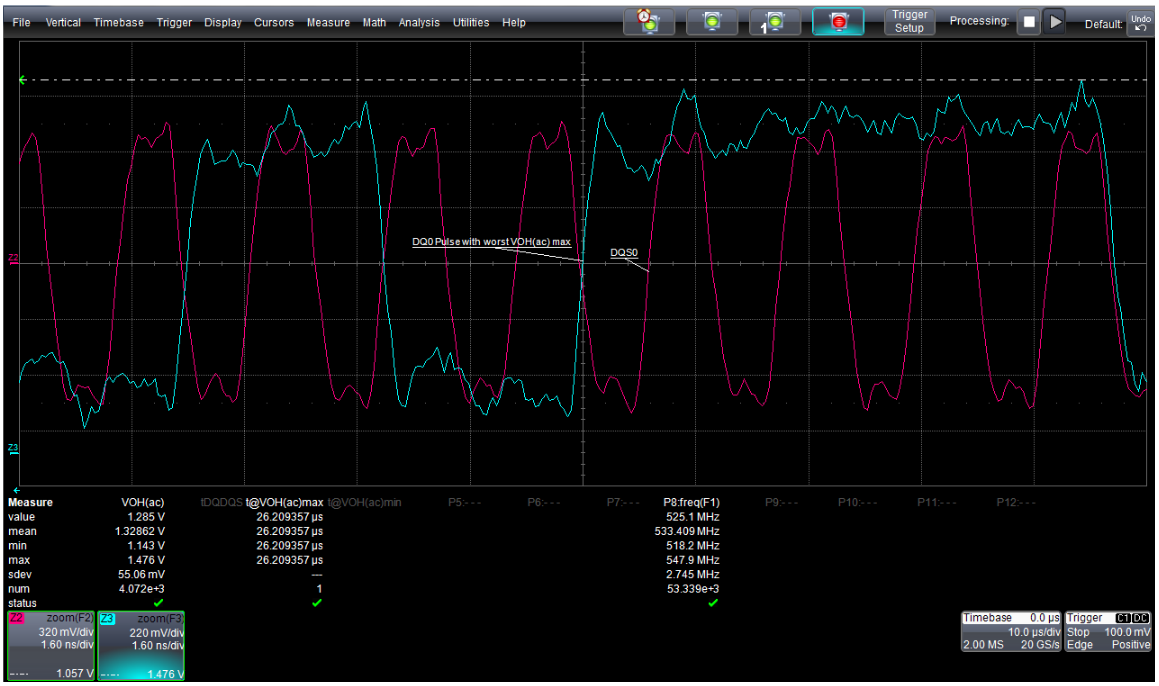


Figure 24. Differential AC Output Logic High/Low

Shown on this screen:

- Z2 is a zoom of F2, the acquired DQS signal after any probe deskew has been applied. The zoom is positioned at the location of the “worst case” VOH(ac) measurement indicated by t@VOH(ac)max. A trace label is applied on this trace according to the signal name assigned to DQS. This signal is not measured in this test and is only provided as a visual reference.
- Z3 is a zoom of F3, the acquired DQ signal after any probe deskew has been applied. The zoom is position at the location of the “worst case” VOH(ac) measurement indicated by t@VOH(ac)max. A trace label is applied on this trace according to the signal name assigned to DQ. This is the signal which is measured in this test.

In the Measure table:

- **VOH(ac) (P1)** is measuring the local maximum of DQ from Vref to Vref. The maximum value is the measured value for VOH(ac) Max of DQ. This test is informational only.
- **t@VOH(ac)min (P4)** displays the location of where the maximum value of VIH(ac) occurred. This is used to position the zoom traces at the location of the “worst case results”.
- **freq(F1)** is measuring the frequency of the differential clock signal.

SRQ, Output Slew Rate

This test is performed using probe setup 2. The purpose of this test is to characterize the slew rate on DQ and DQS of all of the R burst (output) in the acquisition. This test is performed on both rising (SRQ) and falling edges (SRF) and both the minimum and maximum values are measured.

Note: Only slew rate measured on the rising edge of DQ will be discussed below. The measurement methodology is exactly same for the falling edge except the slew rate is measured from VOH(ac) to VOL(ac) instead of VOH(ac) to VOL(ac). The measurement methodology is also identical for DQS.

At the completion of the SRQ test, the oscilloscope is in the following state:

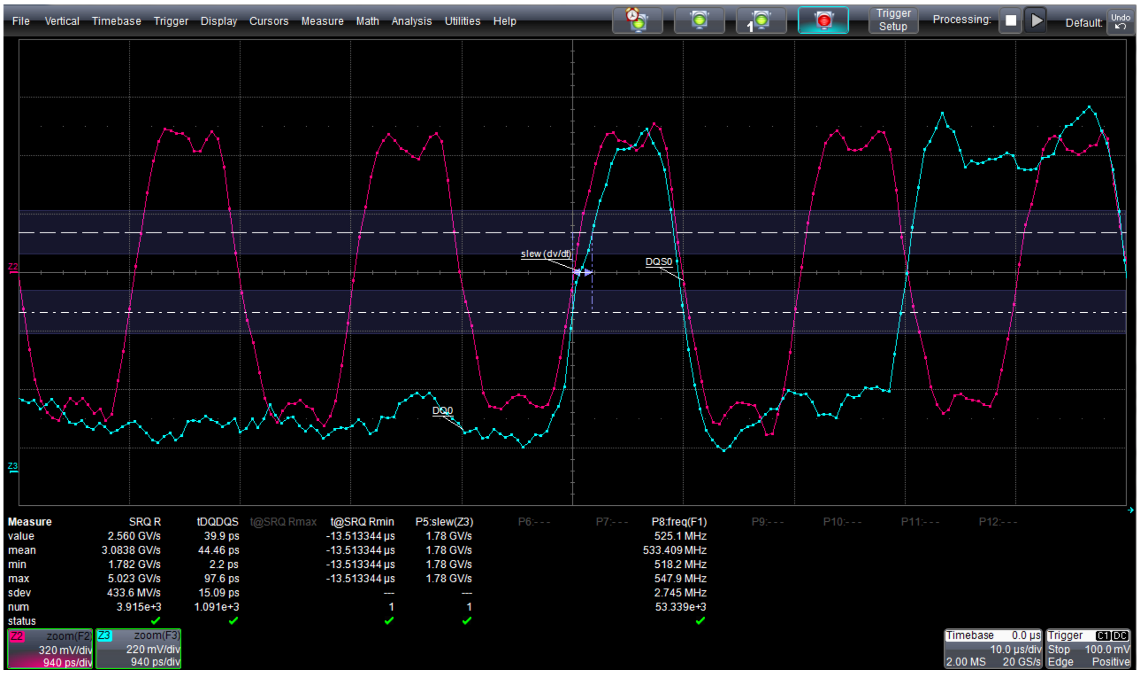


Figure 25. Output Slew Rate

Shown on this screen:

- Z2 is a zoom of F2, the acquired DQS signal after any probe deskew has been applied. The zoom is positioned at the location of the “worst case” SRQ R measurement indicated by t@SRQ Rmin. This signal is not measured in this test and is only provided as a visual reference.
- Z3 is a zoom of F3, the acquired DQ signal after any probe deskew has been applied. The zoom is position at the location of the “worst case” SRQ R measurement indicated by t@SRQ Rmin. This is the signal which is measured in this test.

In the Measure table:

- **SRQ R** (P1) is measuring the slew rate of DQ on the rising edges. The slew rate on the rising edge is measured from VOL(ac) to VOH(ac). The minimum value is the measured value for **SRQ R of DQ min**.
- **tDQDQS** (P2) is measuring the skew between DQ and DQS. Since this measurement is performed once per burst, this shows how many R bursts were in the acquired waveform.
- **t@SRQ Rmin** (P4) displays the location of where the minimum value of SRQ R occurred. This is used to position the zoom traces at the location of the “worst case results”.
- **P5: slew(Z3)** displays the minimum value of SRQ R and is used to display the slew rate measurement markers.
- **freq(F1)** is measuring the frequency of the differential clock signal.

VSWING, Output Signal Maximum Peak to Peak Swing

This test is performed using the probe setup 2. The purpose of this test is to characterize the peak to peak swing on DQ and DQS during all R bursts.

At the completion of the VSWING test, the oscilloscope is in the following state:

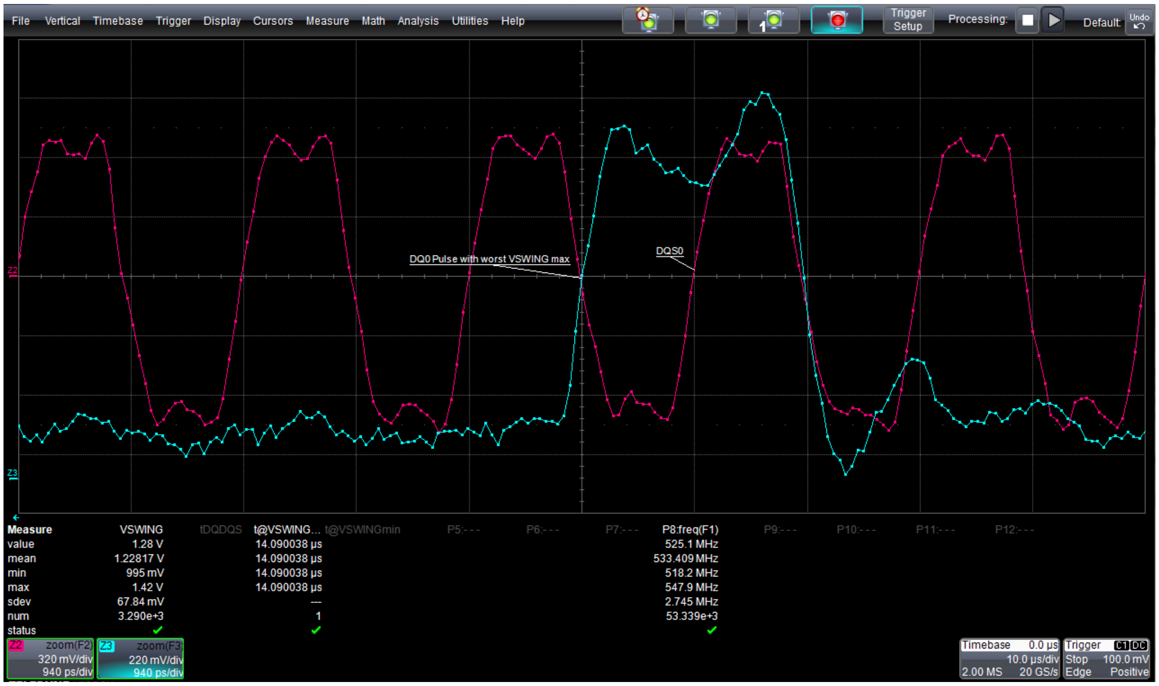


Figure 26. Output Maximum Peak to Peak Swing

Shown on this screen:

- Z2 is a zoom of F2, the acquired DQS signal after any probe deskew has been applied. The zoom is positioned at the location of the “worst case” VSWING measurement indicated by t@VSWING. A trace label is applied on this trace according to the signal name assigned to DQS. This signal is not measured in this test and is only provided as a visual reference.
- Z3 is a zoom of F3, the acquired DQ signal after any probe deskew has been applied. The zoom is position at the location of the “worst case” VSWING measurement indicated by t@VSWING. A trace label is applied on this trace according to the signal name assigned to DQ. This is the signal which is measured in this test.

In the Measure table:

- **VSWING (P1)** is measuring the peak to peak swing of each DQ pulse. This is taking the difference of VOH(ac) and VOL(ac). The maximum value is the measured value for VSWING Max of DQ. This test is informational only and is measured using the legacy method from DDR2
- **t@VSWING (P3)** displays the location of where the maximum value of VSWNG occurred. This is used to position the zoom traces at the location of the “worst case results”.
- **freq(F1)** is measuring the frequency of the differential clock signal.

Electrical Tests on Supply Signals

This electrical test is performed using the probe setup 6.

Vref(DC)

The purpose of this test is to characterize the Vref level and any noise on Vref signal.

The Vref(DC) level is the linear average of Vref over the duration of the acquisition. This average has to be within 0.49*VDD and 0.51*VDD. Additionally, Vref may only temporarily deviate from Vref(DC) by no more than +/- 1% VDD.

At the completion of the Vref test, the oscilloscope is in the following state:

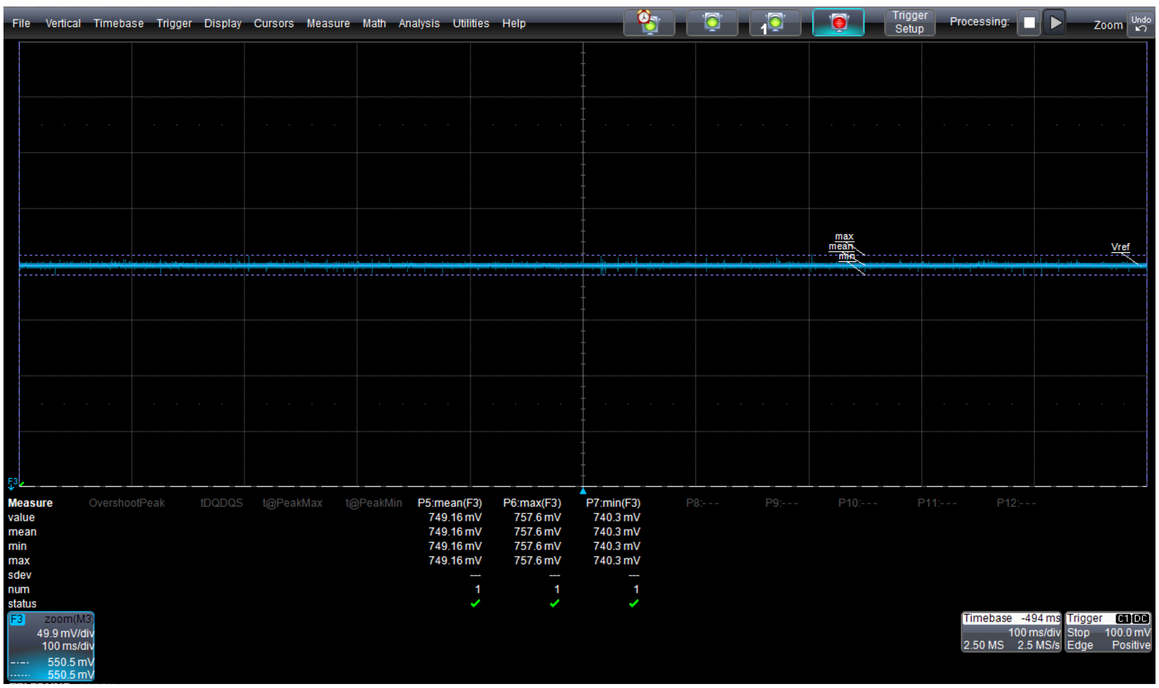


Figure 27. Vref Level

Shown on this screen:

- F3 is a zoom of C3, the acquired Vref signal. Traces labels are placed at the max, min, and mean locations.

In the Measure table:

- **mean(F3)** is measuring the mean of the Vref signal over the duration of the acquisition. This is the Vref(DC) value and is consider to be passing if it is within 0.49*VDD and 0.51*VDD.
- **max(F3)** is measuring the maximum value of the Vref signal. This is the measured value for **Vref Max**. It is considering to be passing if it is less than 1%VDD from Vref(DC).
- **min(F3)** is measuring the minimum value of the Vref signal. This is the measured value for **Vref Min**. It is considering to be passing if it is less than 1%VDD from Vref(DC).

Timing Tests on Write Bursts

tDQSS, CK to DQS Skew

This test is performed using probe setup 2. The purpose of this test is to characterize the allowed range for a rising DQS edge relative to CK on W bursts. This test is very similar to tDQSCK, which is measured on R bursts. Both the maximum and minimum values are measured. For DDR3 and DDR3L, the skew is measured between CK rising at Vref to the *nearest* DQS rising at Vref. For LPDDR3, the skew is measured between CK rising at Vref to the *next* DQS rising at Vref

At the completion of the tDQSS test, the oscilloscope is in the following state:

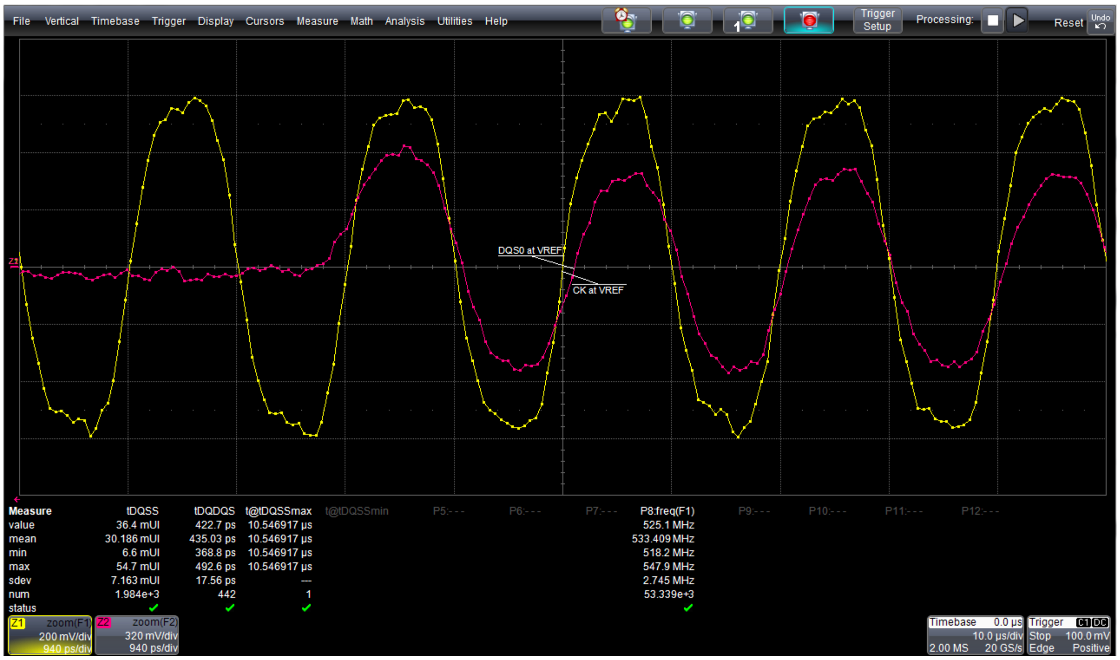


Figure 28. CK to DQS Skew

Shown on this screen:

- Z1 is a zoom of F1, the acquired CK signal after any probe deskew has been applied. The zoom is position at the location of the "worst case" tDQSS measurement indicated by t@tDQSSmax. A trace label is applied on this trace at Vref.
- Z2 is a zoom of F2, the acquired DQS signal after any probe deskew has been applied. The zoom is positioned at the location of the "worst case" tDQSS measurement indicated by t@tDQSSmax. A trace label is applied at Vref.

In the Measure section:

- **tDQSS** (P1) is measuring the skew between CK and DQS. Essentially the time between the two trace labels is measured. The maximum value is the measured value for **tDQSS max** and is reported in mtCK(avg).
- **tDQDQS** (P2) is measuring the skew between DQ and DQS. Since this measurement is performed once per burst, this shows how many W bursts were in the acquired waveform.
- **t@tDQSSmax** (P3) displays the location of where the maximum value of tDQSS occurred. This is used to position the zoom traces at the location of the "worst case results".
- **t@tDQSSmax** (P3) displays the location of where the maximum value of tDQSS occurred. This is used to position the zoom traces at the location of the "worst case results".
- **freq(F1)** is measuring the frequency of the differential clock signal.

tDQSH/tDQSL, DQS Input High/Low Pulse Width

This test is performed using probe setup 2. These tests measure the high (tDQSH) and low (tDQSL) pulse widths of each DQS signal during a W burst. Both the maximum and minimum tDQSH/tDQSL values are measured. This tests are very similar to tQSH and tQSL, which are measured on R bursts.

Note: Only tDQSH will be discussed below. The measurement methodology is the same for the tDQSL expect the measurement is made on DQS from falling edge to a rising edge instead of a rising edge to a falling edge.

At the completion of the tDQSH test, the oscilloscope is in the following state:

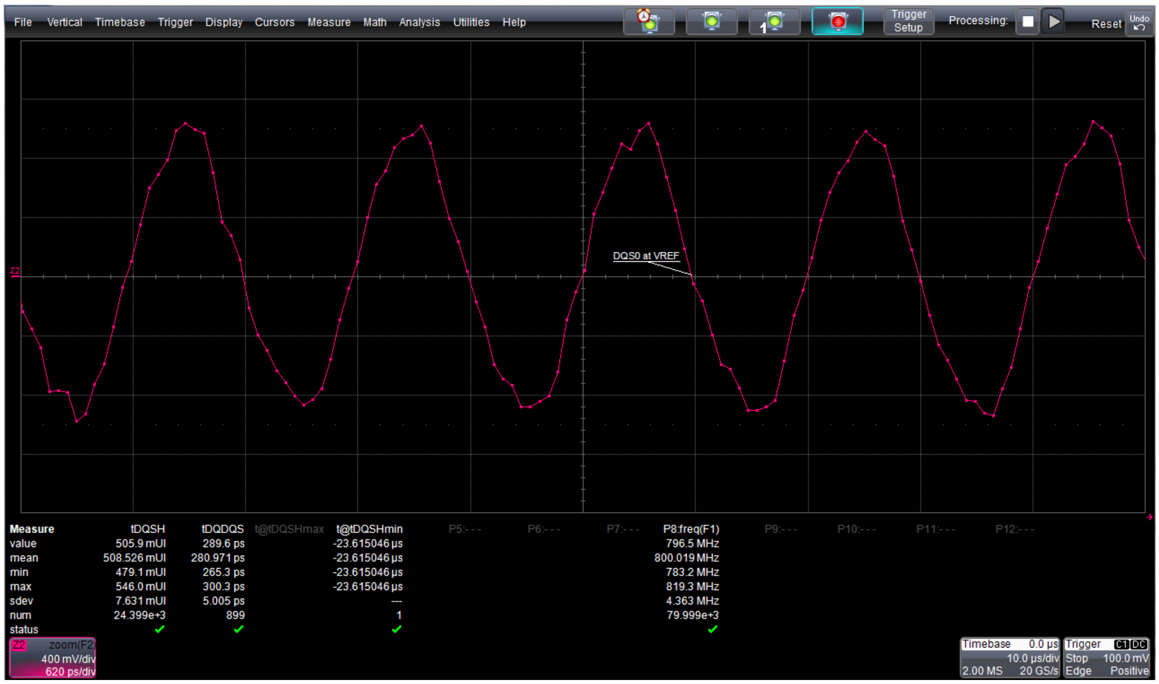


Figure 29. DQS Input High/Low Pulse Width

Shown on this screen:

- Z2 is a zoom of F2, the acquired DQS signal after any probe deskew has been applied. The zoom is positioned at the location of the “worst case” tDQSH measurement indicated by t@tDQSHmin. A trace label is applied at Vref.

In the Measure table:

- **tDQSH** (P1) is measuring the high time of DQS. The high time is determined by measuring the time DQS crosses Vref on a rising edge at to the time DQS crosses the next associated falling edge at Vref. The minimum value is the measured value for **tDQSH min** and is reported in mtCK(avg).
- **tDQDQS** (P2) is measuring the skew between DQ and DQS. Since this measurement is performed once per burst, this shows how many W bursts were in the acquired waveform.
- **t@tDQSHmin** (P4) displays the location of where the minimum value of tDQSH occurred. This is used to position the zoom traces at the location of the “worst case results”.
- **freq(F1)** is measuring the frequency of the differential clock signal.

tDIPW, DQ Input Pulse Width

This test is performed using probe setup 2. This test is measuring the pulse widths of the DQ signal during the W burst. The minimum value is measured on both high and low pulses.

At the completion of the tDIPW test, the oscilloscope is in the following state:

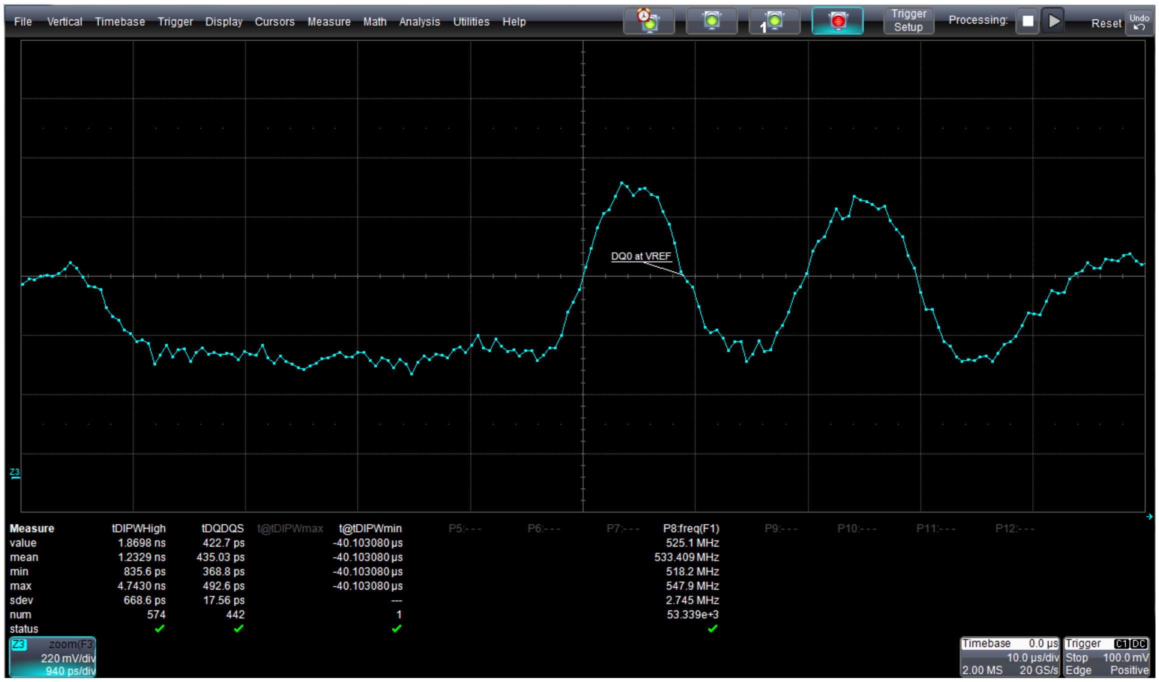


Figure 30. DQ Input Pulse Width

Shown on this screen:

- Z3 is a zoom of F3, the acquired DQ signal after any probe deskew has been applied. The zoom is positioned at the location of the “worst case” tDIPW measurement indicated by t@tDIPWmin. A trace label is applied at Vref on this trace according to the signal name assigned to DQ.

In the Measure table:

- **tDIPWHigh** (P1) is measuring the high time of DQ. The high time is determined by measuring the time DQ crosses Vref on a rising edge (centered on the screen) at to the time DQ crosses the next associated falling edge at Vref (indicated by the trace label). The minimum value is the measured value for **tDIPW High min** and is reported in ps.
- **tDQDQS** (P2) is measuring the skew between DQ and DQS. Since this measurement is performed once per burst, this shows how many W bursts were in the acquired waveform.
- **t@tDIPWmin** (P4) displays the location of where the minimum value of tDIPW occurred. This is used to position the zoom traces at the location of the “worst case results”.
- **freq(F1)** is measuring the frequency of the differential clock signal.

tDSS/tDSH, DQS to CK Setup/Hold Time

This test is performed using probe setup 2. The purpose of this test is to characterize the setup and hold time for a falling DQS edge to the rising CK edge on W bursts. The minimum value is measured for both tDSS and tDSH.

Note: Only tDSS will be discussed below. The measurement methodology is the same for the tDSH expect the hold time is measured rather than the setup time.

At the completion of the tDSS test, the oscilloscope is in the following state:

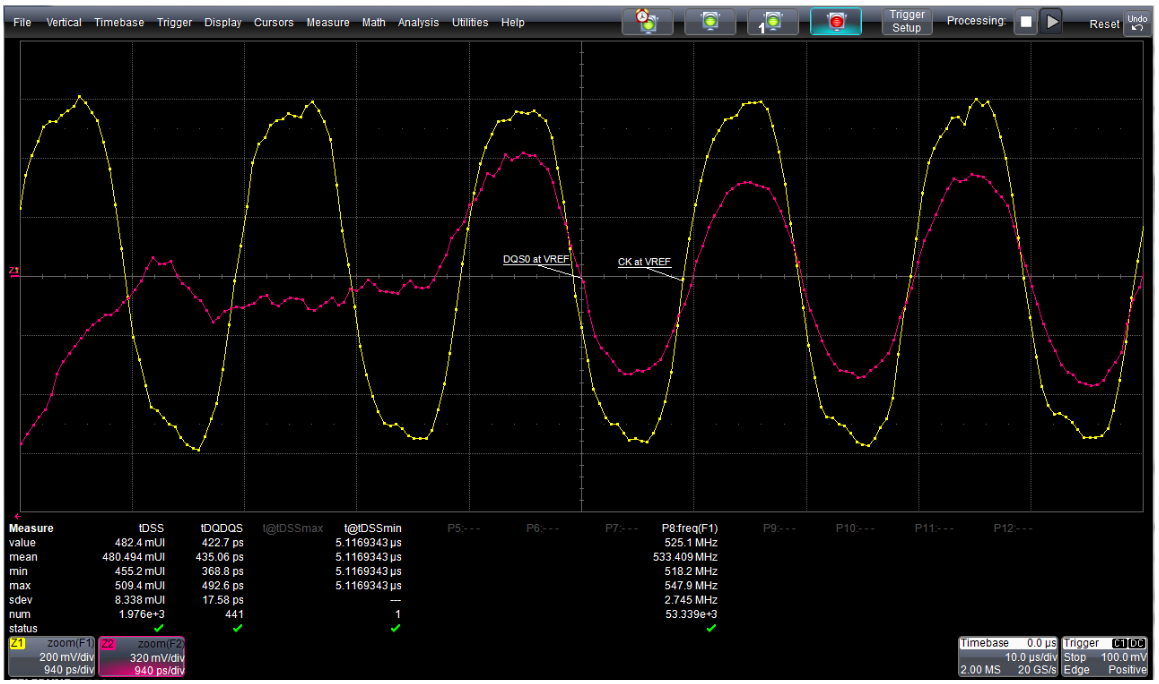


Figure 31. DQS to CK Setup/Hold Time

Shown on this screen:

- Z1 is a zoom of F1, the acquired CK signal after any probe deskew has been applied. The zoom is position at the location of the “worst case” tDSS measurement indicated by t@tDSSmax. A trace label is applied on this trace at Vref.
- Z2 is a zoom of F2, the acquired DQS signal after any probe deskew has been applied. The zoom is positioned at the location of the “worst case” tDSS measurement indicated by t@tDSSmax. A trace label is applied at Vref.

In the Measure table:

- **tDSS** (P1) is measuring the setup time from when the DQS falling edge crossed Vref to when the Ck rising edge crosses Vref. Essentially the time between the two trace labels is measured. The minimum value is the measured value for **tDSS min** and is reported in mtCK(avg).
- **tDQDQS** (P2) is measuring the skew between DQ and DQS. Since this measurement is performed once per burst, this shows how many W bursts were in the acquired waveform.
- **t@tDSSmin** (P4) displays the location of where the minimum value of tDSS occurred. This is used to position the zoom traces at the location of the “worst case results”.

tDS(base)/tDH(base), DQ to DQS Setup/Hold Time

This test is performed using probe setup 2. The purpose of this test is to characterize the setup and hold time between DQ and DQS on W bursts. The minimum value is measured for both tDS(base) and tDH(base).

The base value is equal to the total setup/hold time minus derating (delta) factor. The derating factor provides limit compensation for the signal's measured slew rate and is dependent upon the measured slew rate and AC level.

Note: Only tDS will be discussed below. The measurement methodology is the same for the tDH expect the hold time is measured rather than the setup time.

At the completion of the tDS test, the oscilloscope is in the following state:

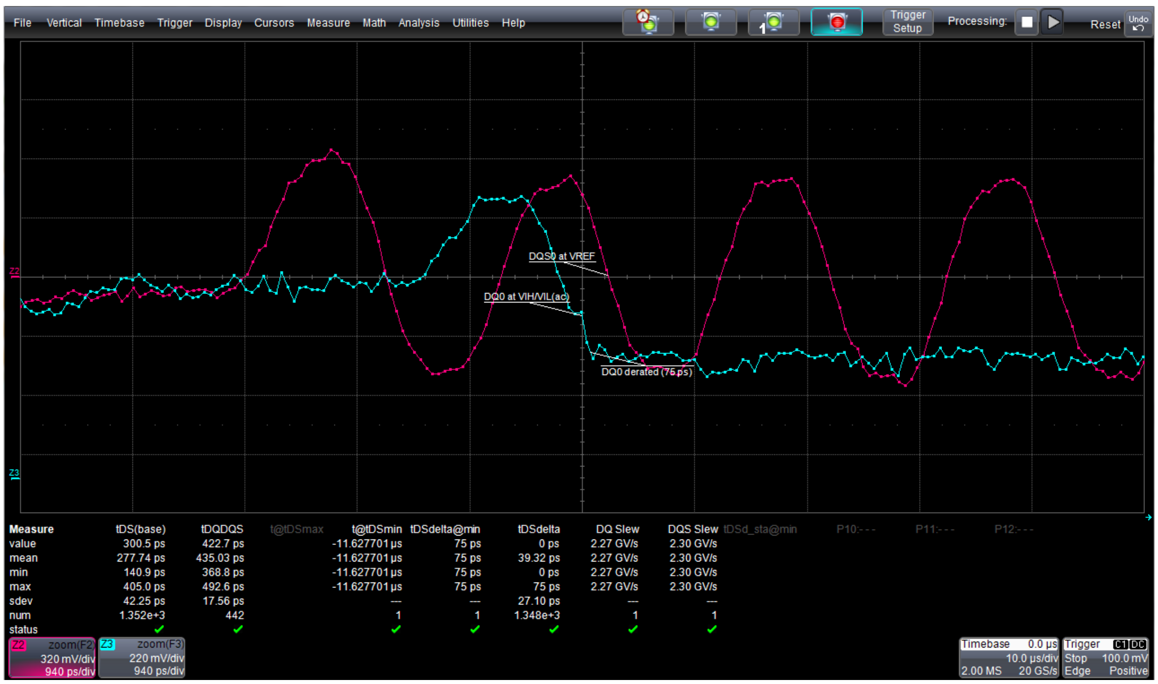


Figure 32. DQ to DQS Setup/Hold Time

Shown on this screen:

- Z2 is a zoom of F2, the acquired DQS signal after any probe deskew has been applied. The zoom is positioned at the location of the "worst case" tDS measurement indicated by t@tDSmin. A trace label is applied at Vref on this trace according to the signal name assigned to DQS.
- Z3 is a zoom of F3, the acquired DQ signal after any probe deskew has been applied. The zoom is positioned at the location of the "worst case" tDS measurement indicated by t@tDSmin. A trace label is applied at VIH/VIL(ac) and at the derated value on this trace according to the signal name assigned to DQ.

In the Measure table:

- **tDS(base)** (P1) is measuring the base setup time which is the value compared to the limit. The base setup time is equal to the total setup time minus the derating (delta) factor. On a rising edge the total setup time is measured between DQ at VIH(ac)min to DQS at Vref and on a falling edge between DQ at VIL(ac)max to DQS at Vref. The derating value (P6) is then subtracted from this measured value. Essentially it is the time between DQS at Vref and the trace label for DQ derated. The minimum value is the measured value for **tDS(base) min** and is reported in ps.
- **tDQDQS** (P2) is measuring the skew between DQ and DQS. Since this measurement is performed once per burst, this shows how many W bursts were in the acquired waveform.
- **t@tDSmin** (P4) displays the location of where the minimum value of tDS occurred. This is used to position the zoom traces at the location of the “worst case results”.
- **tDSdelta@min** (P5) displays the derating value at the minimum tDS value. This value is calculated using a lookup table for the measured DQ (P7) and DQS (P8) slew rates.
- **tDSdelta** (P6) displays the calculated derating values across the entire waveform, based on the measured DQ (P7) and DQS (P8) slew rates.
- **DQ Slew** (P7) measures the DQ slew rate at the minimum tDS value. The slew rate on a rising edge is measured between Vref and VIH(ac)min and the slew rate on a falling edge is measured between Vref and VIL(ac)max.
- **DQS Slew** (P8) measures the DQS slew rate at the minimum tDS value. The slew rate on a rising edge is measured between Vref and VIH(ac)min and the slew rate on a falling edge is measured between Vref and VIL(ac)max.

tWPRE/tWPST, Write Pre/Postamble Time

These tests are performed using probe setup 2. The purpose is to characterize the Preamble and Postamble times during all W bursts detected in the acquisition. tWPRE is measuring the timing between when preamble starts (DQS comes out of idle) and where the preamble ends (DQS at Vref). tWPST is measuring the timing between when the postamble starts (DQS at Vref) and where the postamble ends (DQS begins to returns to idle). Both of these tests use an interpolation algorithm to determine the point where the signal begins and depending upon the signal shape this can lead to some inaccuracies.

Note: Only tWPRE will be discussed below.

At the completion of the tWPRE test, the oscilloscope is in the following state:

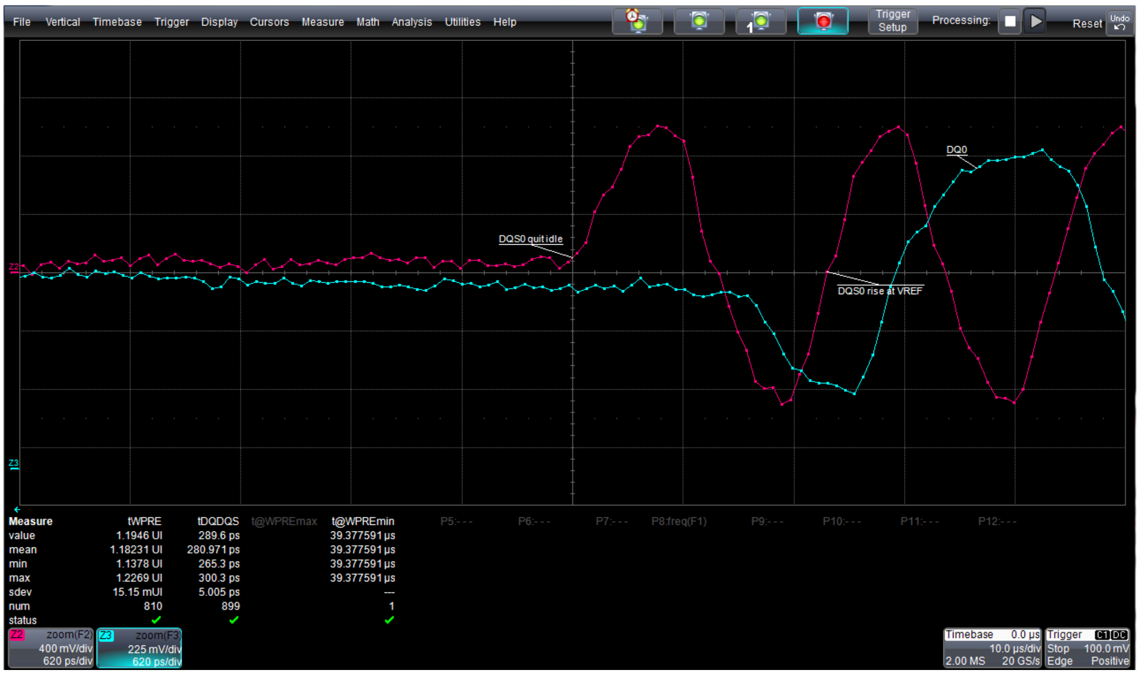


Figure 33. Write Burst Pre/Postamble Time

Shown on this screen:

- Z2 is a zoom of F2, the acquired DQS signal after any probe deskew has been applied. The zoom is positioned at the location of the “worst case” tWPRE measurement indicated by t@WPREmin. A trace label is applied to indicate where the interpolation algorithm has determined where the device is no longer idle and Vref.
- Z3 is a zoom of F3, the acquired DQ signal after any probe deskew has been applied. The zoom is positioned at the location of the “worst case” tWPRE measurement indicated by t@WPREmin. This signal is not measured in this test and is only provided as a visual reference.

In the Measure table:

- **tWPRE** (P1) is measuring the time from DQS begins to leave to idle to the first rising edge on DQS at Vref. The idle level quit time is indicated by the trace label, which is found through interpolation. Essentially the time between the two trace labels is measured. The minimum value is the measured value for **tWPRE min** reported in mtCK(avg).
- **tDQDQS** (P2) is measuring the skew between DQ and DQS. Since this measurement is performed once per burst, this shows how many W bursts were in the acquired waveform.
- **t@WPREmin** (P4) displays the location of where the minimum value of tWPRE occurred. This is used to position the zoom traces at the location of the “worst case results”.

tIS(base)/tIH(base), ADD and CTRL Setup/Hold Time

This test is performed using probe setup 3.The purpose of this test is to characterize the setup and hold time between the ADD/CTRL signal and CK on W bursts. The minimum value is measured for both tIS(base) and tIH(base). The base value is equal to the total setup/hold time minus derating (delta) factor. The derating factor provides limit compensation for the signal's measured slew rate and is dependent upon the measured slew rate and AC level.

Note: Only tIS will be discussed below. The measurement methodology is the same for the tIH expect the hold time is measured rather than the setup time.

At the completion of the tIS test, the oscilloscope is in the following state:

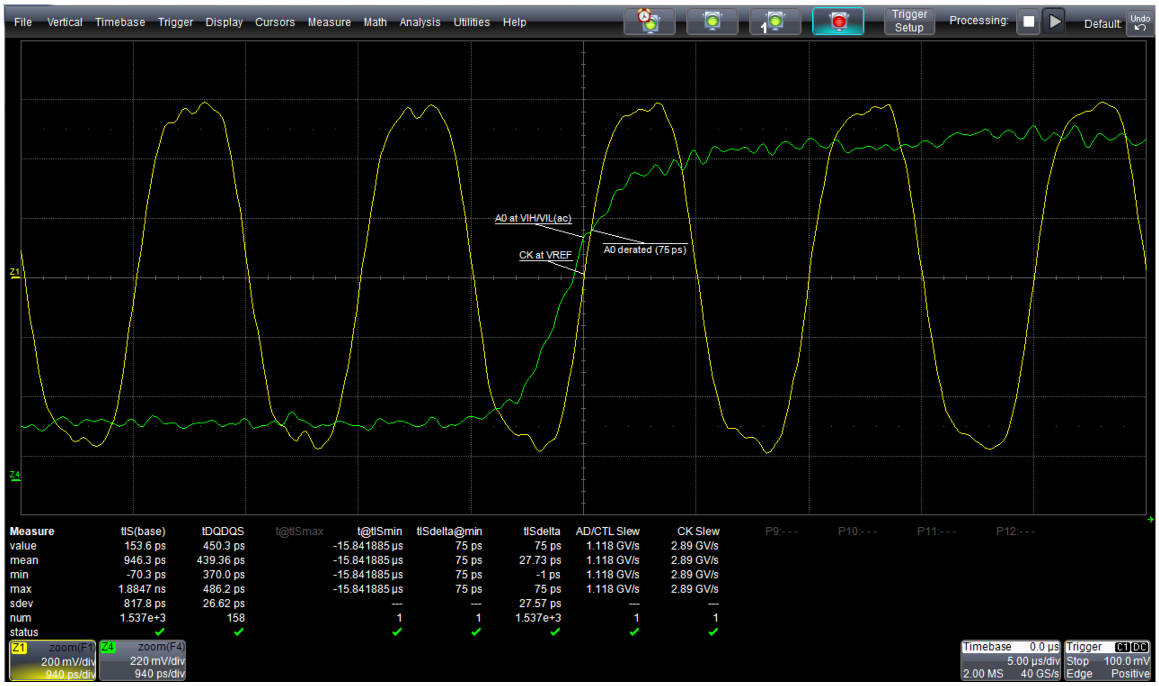


Figure 34. ADD and CTRL Setup/Hold Time

Shown on this screen:

- Z1 is a zoom of F1, the acquired CK signal after any probe deskew has been applied. The zoom is positioned at the location of the "worst case" tIS measurement indicated by t@tISmin. A trace label is applied at Vref on this trace.
- Z4 is a zoom of F4, the acquired ADD/CTRL signal after any probe deskew has been applied. The zoom is positioned at the location of the "worst case" tIS measurement indicated by t@tISmin. A trace label is applied at VIH/VIL(ac) and at the derated value on this trace according to the signal name assigned to ADD/CTRL.

In the Measure table:

- **tIS(base)** (P1) is measuring the base setup time which is the value compared to the limit. The base setup time is equal to the total setup time minus the derating (delta) factor. On a rising edge the total setup time is measured between ADD/CTRL at VIH(ac)min to CK at Vref and on a falling edge between ADD/CTRL at VIL(ac)max to CK at Vref. The derating value (P6) is then subtracted from this measured value. Essentially it is the time between CK at Vref and the trace label for ADD/CTRL derated. The minimum value is the measured value for **tIS(base) min** and is reported in ps.
- **tDQDQS** (P2) is measuring the skew between DQ and DQS. Since this measurement is performed once per burst, this shows how many W bursts were in the acquired waveform.
- **t@tISmin** (P4) displays the location of where the minimum value of tIS occurred. This is used to position the zoom traces at the location of the “worst case results”.
- **tISdelta@min** (P5) displays the derating value at the minimum tIS value. This value is calculated using a lookup table for the measured ADD/CTRL (P7) and CK (P8) slew rates.
- **tISdelta** (P6) displays the calculated derating values across the entire waveform, based on the measured ADD/CTRL (P7) and CK (P8) slew rates.
- **AD/CTLSlew** (P7) measures the ADD/CTRL slew rate at the minimum tIS value. The slew rate on a rising edge is measured between Vref and VIH(ac)min and the slew rate on a falling edge is measured between Vref and VIL(ac)max.
- **CKSlew** (P8) measures the CK slew rate at the minimum tIS value. The slew rate on a rising edge is measured between Vref and VIH(ac)min and the slew rate on a falling edge is measured between Vref and VIL(ac)max.

tIPW, Address and Control Input Pulse Width

This test is measuring the pulse widths of the ADD/CTRL signal during the W burst. The minimum value is measured on both high and low pulses.

At the completion of the tIPW test, the oscilloscope is in the following state:

Figure 35. ADD and CTRL Input Pulse Width

Shown on this screen:

- Z4 is a zoom of F4, the acquired ADD/CTRL signal after any probe deskew has been applied. The zoom is positioned at the location of the “worst case” tIPW measurement indicated by t@tIPWmin. A trace label is applied at Vref on this trace according to the signal name assigned to ADD/CTRL.

In the Measure table:

- **tIPWHigh** (P1) is measuring the high time of ADD/CTRL. The high time is determined by measuring the time ADD/CTRL crosses Vref on a rising edge (centered on the screen) at to the time ADD/CTRL crosses the next associated falling edge at Vref (indicated by the trace label). The minimum value is the measured value for **tIPW High min** and is reported in ps.
- **tDQDQS** (P2) is measuring the skew between DQ and DQS. Since this measurement is performed once per burst, this shows how many W bursts were in the acquired waveform.
- **t@tIPWmin** (P4) displays the location of where the minimum value of tIPW occurred. This is used to position the zoom traces at the location of the “worst case results”.

Timing Tests on Read Bursts

tDQSQ, DQS to DQ Skew

This test is performed using probe setup 2. The purpose of this test is to characterize the latest valid transition of DQ. This test measure the maximum skew between DQS at Vref and DQ at Vref for all DQ transitions during a R burst.

At the completion of the tDQSQ test, the oscilloscope is in the following state:

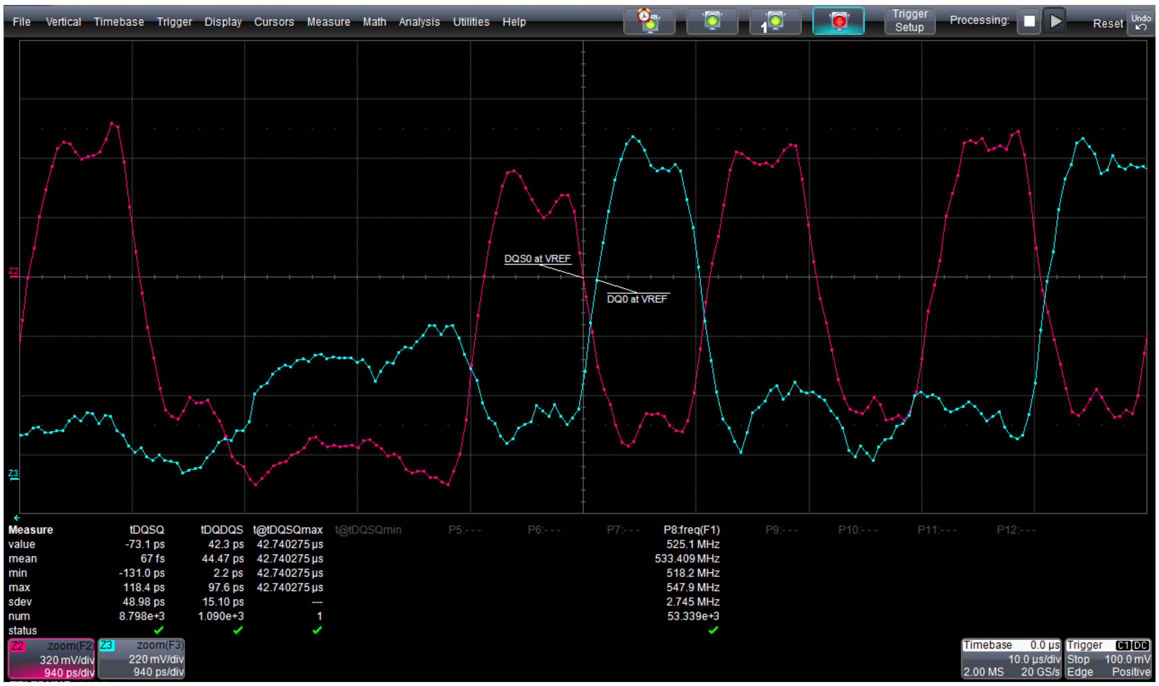


Figure 36. DQS to DQ Skew on Read Bursts

Shown on this screen:

- Z2 is a zoom of F2, the acquired DQS signal after any probe deskew has been applied. The zoom is positioned at the location of the “worst case” tDQSQ measurement indicated by t@tDQSQmax. A trace label is applied at Vref.
- Z3 is a zoom of F3, the acquired DQ signal after any probe deskew has been applied. The zoom is position at the location of the “worst case” tDQSQ measurement indicated by t@tDQSQmax. A trace label is applied at Vref.

In the Measure table:

- **tDQSQ** (P1) is measuring the skew between DQS at Vref and DQ at Vref for each DQ transition. Essentially the time between the two trace labels is measured. The maximum value is the measured value for **tDQSQ Max** reported in mUI.
- **tDQDQS** (P2) is measuring the skew between DQ and DQS. Since this measurement is performed once per burst, this shows how many R bursts were in the acquired waveform.
- **t@tDQSQmax** (P3) displays the location of where the maximum value of tDQSQ occurred. This is used to position the zoom traces at the location of the “worst case results”.
- **freq(F1)** is measuring the frequency of the differential clock signal.

tQSH/tQSL, DQS Output High/Low Time

These tests are performed using probe setup 2. The tests measure the high time (tQSH) and low time (tQSL) for each valid DQS transition during a R burst. Only the minimum tQSH/tQSL values are measured. These tests are very similar to tDQSH and tDQSL, which are measured on W bursts.

Note: Only tQSL will be discussed below. The measurement methodology is the same for the tQSH expect the measurement is made on DQS from rising edge to a falling edge instead of a falling edge to a rising edge.

At the completion of the tQSL test, the oscilloscope is in the following state:

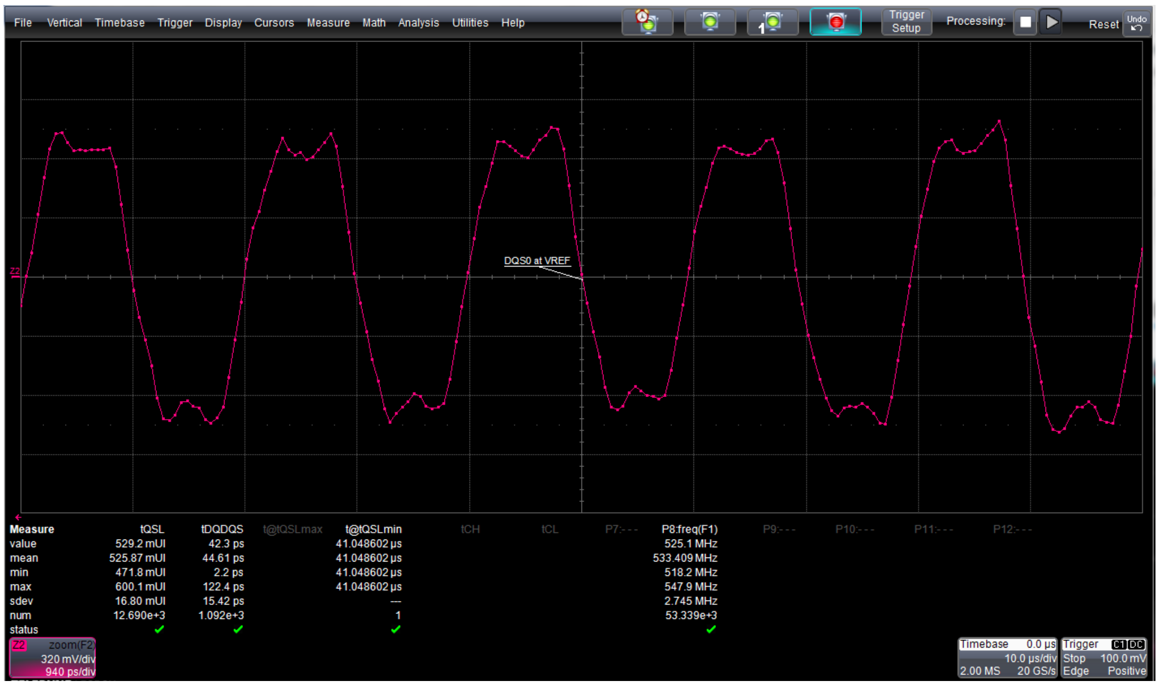


Figure 37. DQS Output High/Low Time

Shown on this screen:

- Z2 is a zoom of F2, the acquired DQS signal after any probe deskew has been applied. The zoom is positioned at the location of the "worst case" tQSL measurement indicated by t@tQSLmin. A trace label is applied at Vref on this trace according to the signal name assigned to DQS.

In the Measure table:

- **tQSL** (P1) is measuring the low time of DQS. The low time is determined by measuring the time DQS crosses Vref on a falling edge at to the time DQS crosses the next associated rising edge at Vref. The minimum value is the measured value for **tQSL min** reported in mtCK(avg).
- **tDQDQS** (P2) is measuring the skew between DQ and DQS. Since this measurement is performed once per burst, this shows how many R bursts were in the acquired waveform.
- **t@tQSLmin** (P4) displays the location of where the minimum value of tQSL occurred. This is used to position the zoom traces at the location of the "worst case results".
- **freq(F1)** is measuring the frequency of the differential clock signal.

tQH, DQ Output Hold Time

This test is performed using probe setup 2. The purpose of this test is to characterize the earliest invalid transition of DQ. This measures the minimum time from DQS at Vref to the next DQ transition at Vref.

At the completion of the tQH test, the oscilloscope is in the following state:

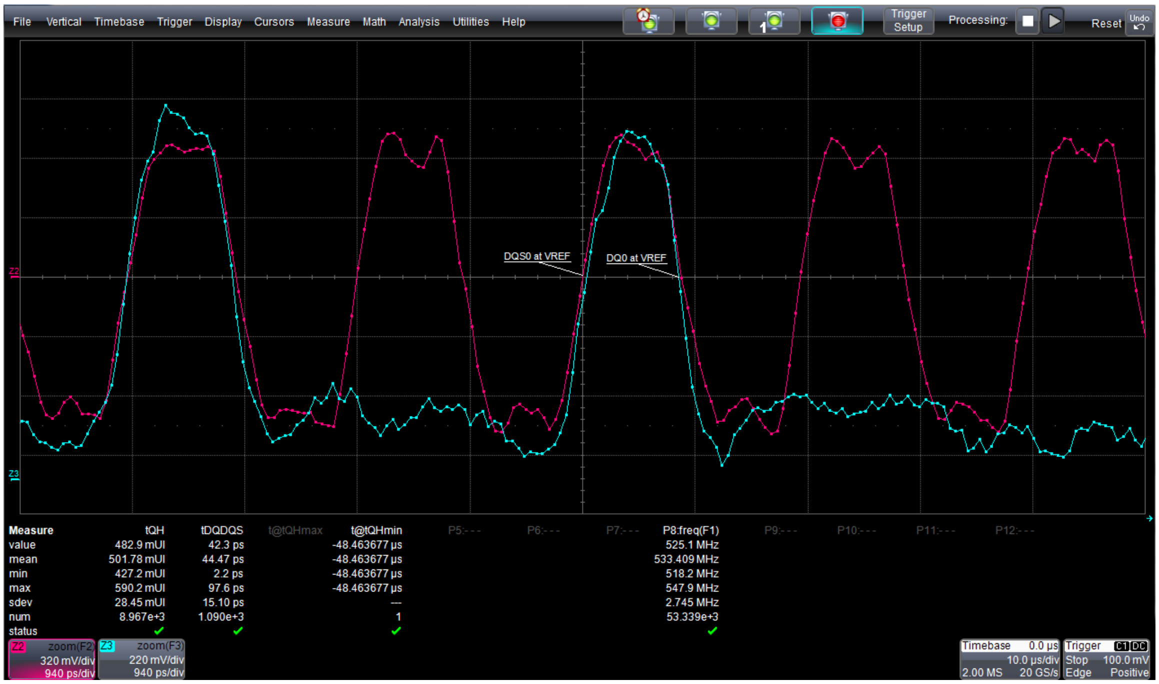


Figure 38. DQ Output Hold Time

Shown on this screen:

- Z2 is a zoom of F2, the acquired DQS signal after any probe deskew has been applied. The zoom is positioned at the location of the "worst case" tQH measurement indicated by t@tQHmin. A trace label is applied at Vref on this trace according to the signal name assigned to DQS.
- Z3 is a zoom of F3, the acquired DQ signal after any probe deskew has been applied. The zoom is position at the location of the "worst case" tQH measurement indicated by t@tQHmin. A trace label is applied at Vref on this trace according to the signal name assigned to DQ.

In the Measure table:

- **tQH** (P1) is measuring the hold time of DQ. The hold time is determined by measuring the time from DQS at Vref to the next DQ transition at Vref. Essentially the time between the two trace labels is measured. The minimum value is the measured value for **tQH Min** reported in mtCK(avg).
- **tDQDQS** (P2) is measuring the skew between DQ and DQS. Since this measurement is performed once per burst, this shows how many R bursts were in the acquired waveform.
- **t@tQHmin** (P4) displays the location of where the minimum value of tQH occurred. This is used to position the zoom traces at the location of the "worst case results".
- **freq(F1)** is measuring the frequency of the differential clock signal.

tDQSCK, CK to DQS Skew

This test is performed using probe setup 2. The purpose of this test is to characterize the allowed range for a rising data strobe edge relative to CK on R bursts. This test is very similar to tDQSS, which is measured on W bursts. Both the maximum and minimum values are measured. For DDR3 and DDR3L, this measures the time from CK rising at Vref to the nearest DQS rising at Vref. For LPDDR3, this measure the time from the first DQS rising edge in the burst at Vref to the previous CK rising edge at Vref.

Note: In LPDDR3 tDQSCK can span multiple clock periods. When tDQSCK > tCK the penultimate (second to last) CK rising edge at Vref is used. When tDQSCK<tCK the previous CK rising edge at Vref is used. The user can modify this using the *tDQSCK<tCK*.

At the completion of the tDQSCK test, the oscilloscope is in the following state:

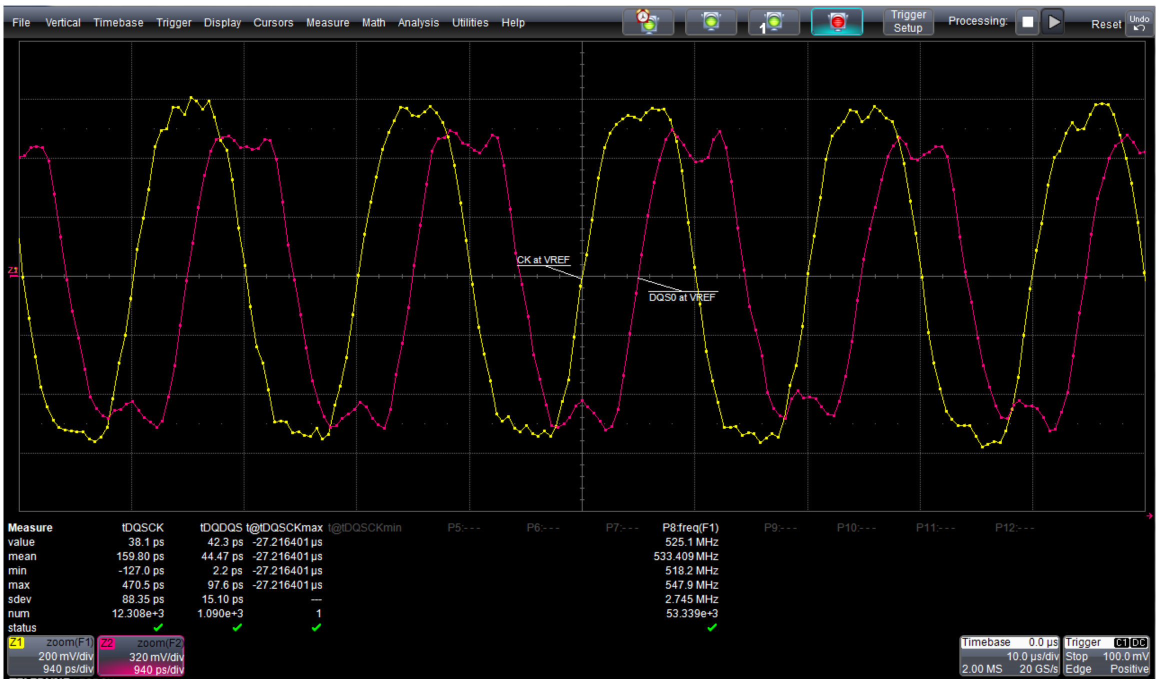


Figure 39. CK to DQS Skew

Shown on this screen:

- Z1 is a zoom of F1, the acquired CK signal after any probe deskew has been applied. The zoom is position at the location of the "worst case" tDQSCK measurement indicated by t@tDQSCKmax. A trace label is applied on this trace at Vref.
- Z2 is a zoom of F2, the acquired DQS signal after any probe deskew has been applied. The zoom is positioned at the location of the "worst case" tDQSCK measurement indicated by t@tDQSCKmax. A trace label is applied at Vref.

In the Measure section:

- **tDQSCK** (P1) is measuring the skew between CK and DQS. Essentially the time between the two trace labels is measured. The maximum value is the measured value for **tDQSCK max**. The limit is derated to account for any clock jitter present.
- **tDQDQS** (P2) is measuring the skew between DQ and DQS. Since this measurement is performed once per burst, this shows how many R bursts were in the acquired waveform.
- **t@tDQSCKmax** (P4) displays the location of where the minimum value of tDQSCK occurred. This is used to position the zoom traces at the location of the "worst case results".
- **freq(F1)** is measuring the frequency of the differential clock signal.

tHZ/tLZ, High/Low Impedance Time

The tests are performed using probe setup 2. The purpose is to characterize the High and Low Impedance times. These tests measure the timing between when the device quits driving (tHZ) or begins driving (tLZ) and CK at Vref. tHZ only tests the maximum value and tLZ tests both a minimum and a maximum value. These tests are measured on both DQ and DQS. Both tests use an interpolation algorithm to determine the point where the signal begins and depending upon the signal shape this can lead to some inaccuracies.

Note: Only tLZ(DQ) will be discussed below. The only difference is tLZ measures the time from when DQ/DQS begins driving from CK; tHZ measures the time from when DQ/DQS quits driving from CK. The methodology is the same for DQS.

At the completion of the tLZ(DQ) test, the oscilloscope is in the following state:

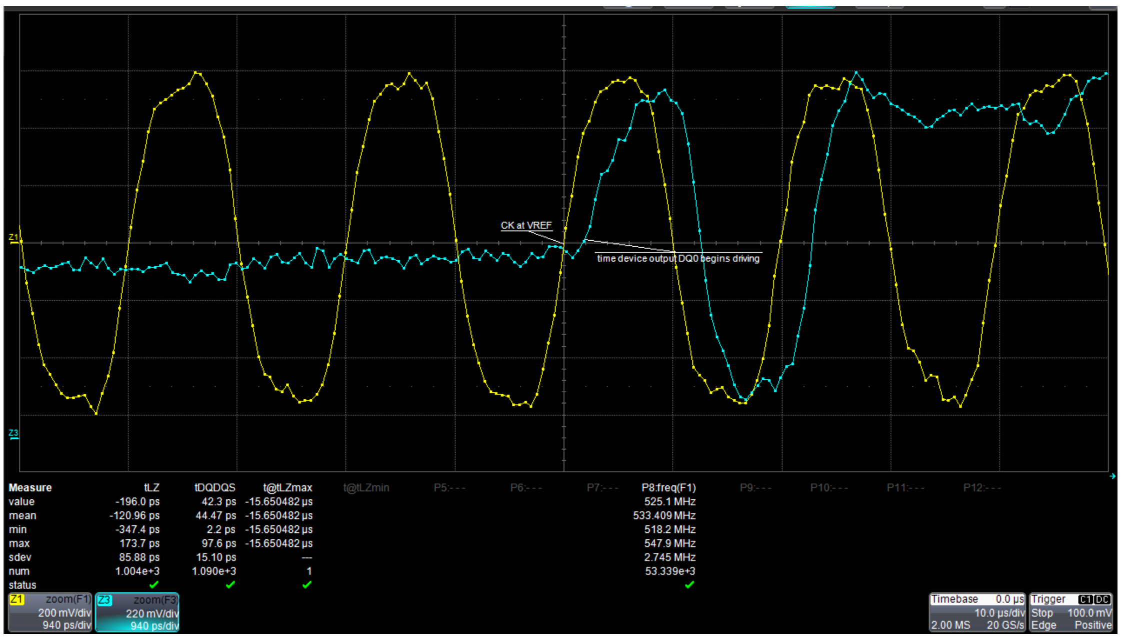


Figure 40. High/Low Impedance Time

Shown on this screen:

- Z1 is a zoom of F1, the acquired CK signal after any probe deskew has been applied. The zoom is position at the location of the “worst case” tLZ measurement indicated by t@tLZmax. A trace label is applied on this trace at Vref.
- Z3 is a zoom of F3, the acquired DQ signal after any probe deskew has been applied. The zoom is position at the location of the “worst case” tLZ measurement indicated by t@tLZmax. A trace label is applied to indicate where the interpolation algorithm has determined where the device is no longer driving. This is the signal which is measured in this test.

In the Measure table:

- **tLZ** (P1) is measuring the time from CK at Vref to the time DQ begins driving. This time is indicated by the trace label which is found through interpolation. Essentially the time between the two trace labels is measured. The maximum value is the measured value for **tLZ(DQ) max**. The limit is derated to account for any clock jitter present.
- **tDQDQS** (P2) is measuring the skew between DQ and DQS. Since this measurement is performed once per burst, this shows how many R bursts were in the acquired waveform.
- **t@tLZmax** (P3) displays the location of where the maximum value of tHZ occurred. This is used to position the zoom traces at the location of the “worst case results”.
- **freq(F1)** is measuring the frequency of the differential clock signal

tRPRE/tRPST, Read Preamble

This test is performed using probe setup 2. The purpose of these tests are to characterize the Preamble and Postamble times during all R bursts detected in the acquisition. tRPRE is measuring the timing between when preamble starts (DQS comes out of idle) and where the preamble ends (DQS at Vref). tRPST is measuring the timing between when the postamble starts (DQS at Vref) and where the postamble ends (DQS begins to returns to idle). Both of these test use an interpolation algorithm to determine the point where the signal begins and depending upon the signal shape this can lead to some inaccuracies.

Note: Only tRPRE will be discussed below. As stated the only difference between tRPRE and tRPST is whether the preambles or postambles are measured.

At the completion of the tRPRE test, the oscilloscope is in the following state:

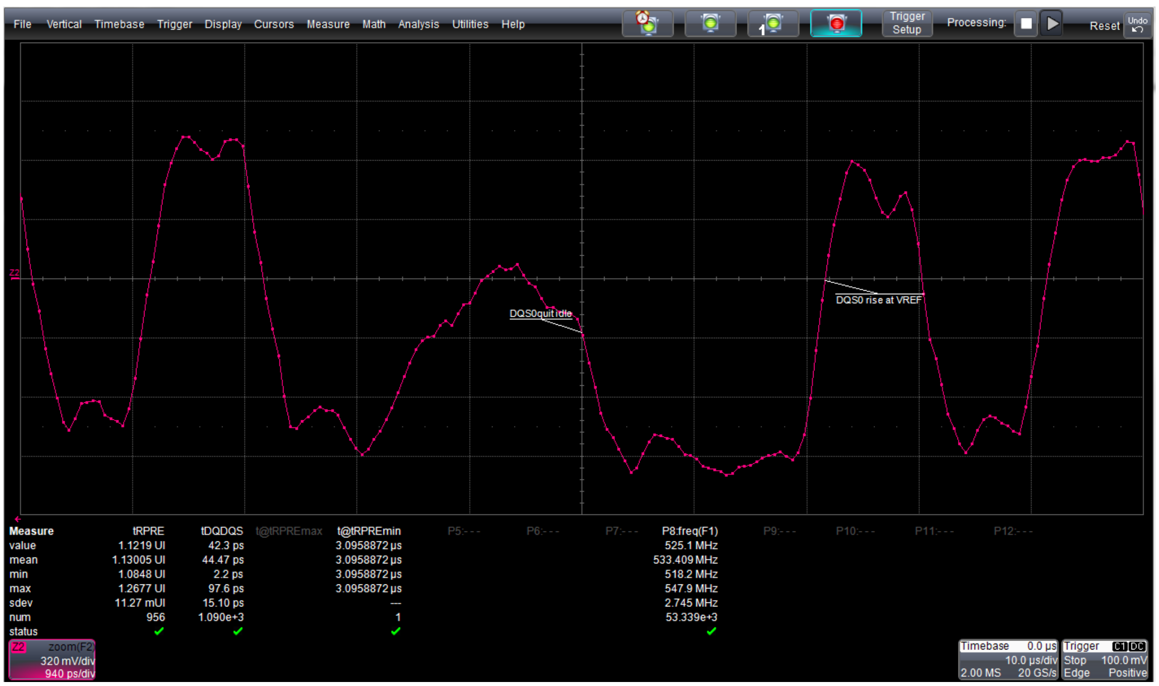


Figure 41. Read Preamble

Shown on this screen:

- Z2 is a zoom of F2, the acquired DQS signal after any probe deskew has been applied. The zoom is positioned at the location of the “worst case” tRPRE measurement indicated by t@tRPREmin. A trace label is applied to indicate where the interpolation algorithm has determined where the device is no longer idle and Vref.

In the Measure table:

- **tRPRE** (P1) is measuring the time from when time DQS quits driving to the next rising edge on DQS at Vref. The idle quit time is indicated by the trace label which is found through interpolation. Essentially the time between the two trace labels is measured. The minimum value is the measured value for **tRPRE min** reported in mtCK(avg).
- **tDQDQS** (P2) is measuring the skew between DQ and DQS. Since this measurement is performed once per burst, this shows how many R bursts were in the acquired waveform.
- **t@tRPREmin** (P4) displays the location of where the minimum value of tRPRE occurred. This is used to position the zoom traces at the location of the “worst case results”.
- **freq(F1)** is measuring the frequency of the differential clock signal

QPHY-DDR3 Variables

Custom Speed Grade in MT/s

This variable allows the user to define a custom speed grade to be used. This speed grade is used to set the oscilloscope timebase and sampling rate, see **Clock Period Per Screen Division** for more information. The default value for this variable is **0**. Using the default value, QPHY will read the speed grade from the selected limit set.

Waveform Path

This variable allows the user to specify the path on the oscilloscope to save and recall waveforms. **When Use Stored Waveforms** is set to **No**, the acquired waveforms will be saved in this path in a subfolder with the name provided as the Device Under Test in the Session Info prompt at the beginning of the test. See **Appendix A** for details on the File Name Conventions For Saved Waveform Data. **When Use Stored Waveforms** is set to **Yes**, QPHY will load saved waveforms from this path using a subfolder with the name provided as the Device Under Test in the Session Info prompt. The default value for this variable is **D:\Waveforms\DDR3**.

Script Execution Settings

Enable Prompt before Signal Acquisition

When set to **True** a prompt will appear to begin the signal acquisition sequence. This will allow the user to generate read/write bursts at the start of the acquisition or modify the trigger conditions before signal acquisition. The default value for this variable is **False**.

Silent Mode

This variable allows the user to run QPHY without any user interaction when it is set to **Yes**. The default value for this variable is **No**.

Stop On Test

When set to **Yes**, the script stops after each test allowing the user to view the results. The setup is saved so the oscilloscope settings can be modified by the user to allow for further debug results. Upon completion of debugging, testing can be seamlessly resumed with one click of a button. The default value for this variable is **No**.

Use Chip Select

When set to Yes, the script will use the chip select signal to correctly identify read and write bursts in multi-ranked systems. The chip select line is used in conjunction with the Overall Read Latency and Overall Write Latency variables to correctly identify the proper read and write bursts. In order to use this variable an additional probe is required to be connected to CS. The default value for this variable is **No**.

Signal Names

These variables give the user control over the signal names which appear in the test report and screenshots.

DQ Signal Name

This variable allows the user to assign a name to the DQ signal to appear in the test report and screenshots. The default signal name is **DQ0**.

DQS Signal Name

This variable allows the user to assign a name to the DQS signal to appear in the test report and screenshots. The default signal name is **DQS0**.

DQS_t Signal Name

This variable allows the user to assign a name to the DQS_t signal to appear in the test report and screenshots. The default signal name is **DQS0_t**.

DQS_c Signal Name

This variable allows the user to assign a name to the DQS_c signal to appear in the test report and screenshots. The default signal name is **DQS0_c**.

ADD/CTRL Signal Name

This variable allows the user to assign a name to the ADD/CTRL signal to appear in the test report and screenshots. The default signal name is **A0**.

CK_t Signal Name

This variable allows the user to assign a name to the CK_t signal to appear in the test report and screenshots. The default signal name is **CK0_t**.

CK_c Signal Name

This variable allows the user to assign a name to the CK_c signal to appear in the test report and screenshots. The default signal name is **Ck0_c**.

Chip Select Signal Name

This variable allows the user to assign a name to the CS signal to appear in the test report and screenshots. The default signal name is **CS0#**.

VirtualProbe Setup

These variables must be adjusted if the user wants to use VirtualProbe.

VirtualProbe Control

This variable allows the user to enable VirtualProbing and to determine during which group of tests it should be applied. The user can choose to apply VirtualProbe during tests on a Read burst or a Write burst. In order to use VirtualProbe the oscilloscope must have the VirtualProbe option. The default value is **Off**.

VirtualProbe Tool Selection

This variable allows the user to choose between VirtualProbe at Receiver (VP@Rcvr) or VirtualProbe when **VirtualProbe Control** is enabled. The default value is **VP@Rcvr**.

VP at Receiver Path

This variable allows the user to specify the path on the oscilloscope to save/recall VirtualProbe at Receiver setup files from.

VP@Rcvr setup file name

These variables define the name of the VP@Rcvr setup file which will be used for each signal (DQse, DQSdiff, or CKdiff). When setting up VP@Rcvr use, F9 for the CKdiff signal, F10 for the DQSdiff signal, and F11 for the DQse signal. The setup file name should include the .lss extension.

VirtualProbe Path

This variable allows the user to specify the path on the oscilloscope to save/recall VirtualProbe setup files from. When creating a VirtualProbe setup file the following VirtualProbe Setups should correlate as following:

Setup A	Setup B	Setup C	Setup D
C1	C2	C3	C4

VirtualProbe setup file name

This variable defines the name of the VirtualProbe setup which will be used for all signals under test.

Demo Settings

These variables must be adjusted if the user wishes to run QPHY using saved waveforms.

Use Stored Waveforms
When enabled QPHY will run using previously stored waveforms. The waveforms will be recalled using the defined **Waveform Path.** The default value is **No**.

Recalled Waveform File Index (5 digits)
QPHY will recall the saved waveform file using the defined 5 digit index of the file. The default value is **00000**.

Define format used to set trace names
This variable defines how QPHY will store and recall waveforms. If **LeCroy** is used then the files will be automatically saved/recalled using the format defined in Error! Reference source not found.. If **Dialog** is selected the user will be prompted to enter the file names to be saved/recalled. The default setting is **LeCroy**.

Use Stored Trace for Speed Grade
This option allows QPHY to be set to measure the clock frequency (which is used to check the selected speed grade) only once during a run. The default selection is **No**.

Advanced Settings

These variables are designed to give advanced users more control over the QualiPHY script.

Clock Period Per Screen Division
Oscilloscope timebase and sampling rate are set to acquire the given number of clock cycle per display horizontal division at a given DUT Speed Grad in MT/s and for a Max. Number of Samples Per Clock Period. The default is **3341** clock periods (this gives a 10us/div timebase at 667 MT/s and 3.3MS max for 100 samples per period).

Timebase = [Clock Period Per Screen Division] / ([DUT Speed Grade in MT/s] / 2 * 1e6)

Maximum Samples = [Max. Number Of Samples Per Clock Period] * [Clock Period Per Screen Division] * 10

Number of Cycles for Clock test
The JEDEC standard requires 200 cycles for the Clock compliance test. This variable allows the user to enter any positive whole number. The default value is **200** cycles.

Half Cycle before Write Preambles
This variable allows QPHY to account for an additional half cycle which is added before the write preamble by some controllers. The default value is **Yes**.

Max. Number Of Samples Per Clock Period

The oscilloscope timebase and sampling rate is set to acquire the given number of points per clock period. See the Clock Period Per Screen Division topic for more details. Choose between 10, 20, 50, 100, 200, 500 or 1000. The default value is **100**.

Advanced Settings – Read/Write Separation

These variables are designed to give advanced users more control over the limits which are used to separate Read and Write bursts.

QPHY-DDR3 is measuring the skew between DQ and DQS in order to classify read and write bursts. For a burst to be detected as a read or write, the measured skew must fall within the defined upper and lower limits.

For a read burst the limit values should be centered about 0 since DQ and DQS are phase aligned during a read burst. For a write burst the limit values should be centered about 0.5 since DQ and DQS are a quarter cycle out of phase during a write burst. The default values are optimized to work for the vast majority of typical signals. However, for unique cases these variables can be used to account for reflections or known skew in a system.

These variables are used as multipliers and are held constant across each speed grade. In order to determine the exact limit each is limit value multiplied by the bit period (inverse of the transfer rate). Below shows an example for DDR3-1333.

Speed Grade	T/s	Bit Period	Read Lower Limit	Read Upper Limit	Write Lower Limit	Write Upper Limit
DDR3-1333	1.33e9	7.5e-10	-113 ps	113 ps	218 ps	533 ps

Read Burst Separation Upper Limit
This defines the multiplier used for the upper limit bound for a read burst. The default value is **0.15**.

Read Burst Separation Lower Limit
This defines the multiplier used for the lower limit bound for a read burst. The default value is -**0.15**.

Write Burst Separation Upper Limit
This defines the multiplier used for the upper limit bound for a write burst. The default value is **0.71**.

Write Burst Separation Lower Limit
This defines the multiplier used for the lower limit bound for a write burst. The default value is **0.29**.

Advanced Settings – Standard Levels

SE AC Input Levels for ADD/CMD

This variable allows the user to select the AC level which is used for the ADD/CMD signal. When set to **Auto** the AC levels are selected according to the following table.

	800	1066	1333	1600	1866	2133
DDR3	AC175	AC175	AC150	AC150	AC135	AC135
DDR3L	AC160	AC160	AC135	AC135	AC130	-
LPDDR3	-	-	AC150	AC150	AC135	AC135

SE DC Input Levels for ADD/CMD

This variable allows the user to select the DC level which is used for the ADD/CMD signal. When set to **Auto** the DC levels are selected according to the following table.

DDR3	DC100
DDR3L	DC90
LPDDR3	DC100

SE AC Input Levels for DQ

This variable allows the user to select the AC level which is used for the DQ signal. When set to **Auto** the AC levels are selected according to the following table.

	800	1066	1333	1600	1866	2133
DDR3	AC175	AC175	AC150	AC150	AC135	AC135
DDR3L	AC160	AC160	AC135	AC135	AC130	-
LPDDR3	-	-	AC150	AC150	AC135	AC135

SE DC Input Levels for DQ

This variable allows the user to select the DC level which is used for the DQ signal. When set to **Auto** the DC levels are selected according to the following table.

DDR3	DC100
DDR3L	DC90
LPDDR3	DC100

Advanced Settings – Custom Levels

Standard or Custom Levels

This variable allows the user to use either **Standard** or **Custom** Levels. Standard uses the levels defined by the JEDEC specification according to what is configured in the **Standard Levels** variable section. Custom uses the VIH/VIL AC/DC levels defined by the custom levels variables. The default value for this variable is **Standard**.

VDD, VDDQ, VIH(ac), VIH(dc), VIL(ac), VIL(dc), Vref, VSS

These variables allow the user to enter custom values to be used for each level. The units for each variable are in mV. These variables are only used when **Custom** levels are in use.

Advanced Settings – Latency Settings

Overall Read Latency

This is used to specify the Delay between DDR command (Read) to first data bit of related read burst. This is needed when using the Chip Select line to correctly identify read and write bursts in multi-ranked systems. This latency is measured in clock periods. The default value is **5**.

Overall Write Latency

This is used to specify the Delay between DDR command (Write) to first data bit of related read burst. This is needed when using the Chip Select line to correctly identify read and write bursts in multi-ranked systems. This latency is measured in clock periods. The default value is **5**.

Probe Setup - Common Variables

This section will cover variables which are common to all Probe Setups. Variables which are specific to each individual Probe Setup are cover in a section dedicated to that Probe Setup.

Probe Tip Selection

This variable will allow the user to select which probe tip is being used. Possible selections include SI, PT, SMA/SMP, SP, and HiTemp. The default selection is **SI**.

Channel Gain

Allows the user to manually specify the vertical scale in V/div.

Channel Index

Allows the user to manually specify the channel index.

Channel Invert

Allows the user to invert the selected signal.

Channel Offset

Allows the user to manually specify the offset in Volts.

Probe Setup: CKdiff

These variables control the probe setup for the configuration using a differential clock (CK) only.

CAS Latency, CAS Write Latency, Speed Bin

These variables are used to define the tCK(avg) limits as defined in tables 62-67 in JESD79-3F. These variables are only used by QPHY when **Speed Bin Parameters Automatic Selection** is set to **No**. The default value for CAS Latency (CL) is **5**, for CAS Write Latency (CWL) is **5**, and for Speed Bin is **DDR3-1600H**.

Speed Bin Parameters Automatic Selection

This variable allows QPHY to automatically select a valid combination of CL, CWL, and Speed Bin set to **Yes**. When set to **No** QPHY will used the appropriate variables as they are defined. The default value is **Yes**.

Probe Setup: CKdiff-DQSdiff-DQse

These variables control the probe setup for the configuration using a differential clock (CK), single-ended Data (DQ), and differential strobe (DQS).

Input Slew Rate

This variable allows the user to control which signals are tested during the input slew rate tests. The user can choose to test DQ, DQS, and CK or only one of the signals. The default setting is to test **DQ, DQS,** and **CK**.

tDQSCK<tCK

This variable only applies for the tDQSCK measurement in LPDDR3. This variable allows the user to define if tDQSCK is less than tCK. When tDQSCK > tCK the penultimate (second to last) CK rising edge at Vref is used. When tDQSCK<tCK the previous CK rising edge at Vref is used. The default setting is **No**.

Probe Setup: CKdiff-DQSdiff-DQse-ADD/CTRLse

These variables control the probe setup for the configuration using a differential clock (CK), a single-ended Data (DQ), a differential strobe (DQS), and a single-ended address(ADD)/control(CTRL) signal.

Input Slew Rate

This variable allows the user to control which signals are tested during the input slew rate tests. The user can choose to test ADD, DQ, DQS, and CK or only one of the signals. The default setting is to test **ADD** only.

QPHY-DDR3 Limit Sets

DDR3-800
This corresponds to the JEDEC JESD79-3F DDR3 standard specification limits for 800 MT/s.

DDR3-1066
This corresponds to the JEDEC JESD79-3F DDR3 standard specification limits for 1066 MT/s.

DDR3-1333
This corresponds to the JEDEC JESD79-3F DDR3 standard specification limits for 1333 MT/s.

DDR3-1600
This corresponds to the JEDEC JESD79-3F DDR3 standard specification limits for 1600 MT/s.

DDR3-1866
This corresponds to the JEDEC JESD79-3F DDR3 standard specification limits for 1866 MT/s.

DDR3-2133
This corresponds to the JEDEC JESD79-3F DDR3 standard specification limits for 2133 MT/s.

DDR3L-800
This corresponds to the JEDEC JESD79-3-1A.01 DDR3L standard specification limits for 800 MT/s.

DDR3L-1066
This corresponds to the JEDEC JESD79-3-1A.01 DDR3L standard specification limits for 1066 MT/s.

DDR3L-1333
This corresponds to the JEDEC JESD79-3-1A.01 DDR3L standard specification limits for 1333 MT/s.

DDR3L-1600
This corresponds to the JEDEC JESD79-3-1A.01 DDR3L standard specification limits for 1600 MT/s.

DDR3L-1866
This corresponds to the JEDEC JESD79-3-1A.01 DDR3L standard specification limits for 1866 MT/s.

LPDDR3-1333
This corresponds to the JEDEC JESD209-3B LPDDR3 standard specification limits for 1333 MT/s.

LPDDR3-1600
This corresponds to the JEDEC JESD209-3B LPDDR3 standard specification limits for 1600 MT/s.

LPDDR3-1866
This corresponds to the JEDEC JESD209-3B LPDDR3 standard specification limits for 1866 MT/s.

LPDDR3-2133
This corresponds to the JEDEC JESD209-3B LPDDR3 standard specification limits for 2133 MT/s.

Appendix A: Naming Conventions for Saved Waveforms

QPHY-DDR3 saves the waveforms from each acquisition using a specific file name convention. This specific waveform name definition allows the user to re-run any acquisition to recreate specific test results. When running QPHY-DDR3 in demo mode the variables need to be setup up appropriately to let QPHY know which waveform should be recalled.

Here is a typical QPHY-DDR3 waveform name: C2_CKDQ0DQS3_DQS3 _00014.trc

- **C2**: This is the channel used to acquire the signal. In this case C2 was used. When running in Demo mode this portion of the waveform must match the *Channel Index* variable.

  Possible values: C1, C2, C3, C4

- **CKDQ0DQS3**: This is the probe setup used during the acquisition. When running in Demo mode this portion of the waveform must match the Probe Setup for the test being run.

  Possible Values: CK (CK diff probe Setup), CKDQxDQSx (CK-DQ-DQS 3 probe setup), CKDQxDQSxAx (CK-DQ-DQS-Add 4 probe setup), etc.

- **DQS3**: This is the signal name for this trace as it was set using the *Signal Name* variable. When running in Demo mode this portion of the waveform must match the *Signal Name* variable.

  Possible values: DQ0-63, DQS0-15, etc.

- **00014**: This is the file index. QPHY will automatically increment this by one on each run. When running in Demo mode this portion of the waveform must match the *Recalled Waveform File Index* variable.

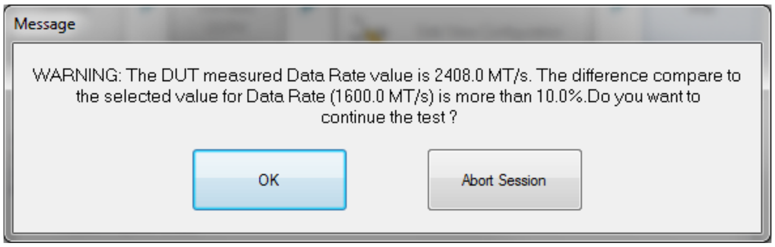
  Possible values: Any five digit number

Portion of Trace Name	Meaning
C2	Channel Index
CKDQ0DQS3	Probe Setup
DQS3	Signal Name
00014	File Index

Appendix B: Common Warnings

Clock Speed Grade

At the beginning of each run QPHY measures the clock speed. This is used to verify that the appropriate limit set is being used. The warning message occurs when the measured speed grade is greater than 10% different than the selected speed grade. When attempting to run on saved waveforms, if the displayed data rate is zero this is an indication that the waveforms were not properly loaded by QPHY.



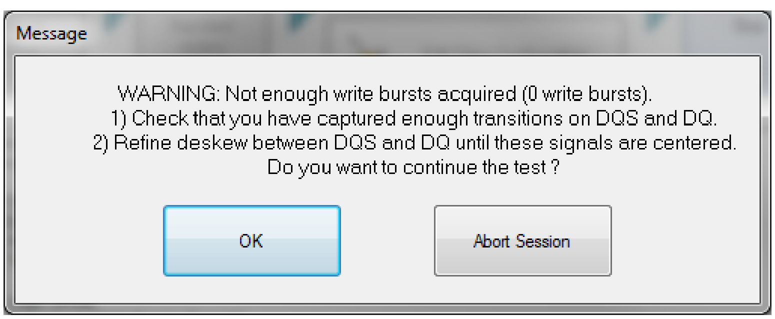
Clock Speed Grade Warning

<u>Solution</u>

Check to make sure the appropriate limit set has been selected, or if using custom speed grade, set the *Custom Speed Grade* variable.

Read/Write Burst

At the beginning of each acquisition QPHY will check to see that enough R or W bursts are captured in the acquisition. This warning appears when less than 10 R or W bursts are not detected. When there are less than 10 bursts detected the measurements will not have much of a statistical significance. If only R burst tests are selected than the script will only check for R burst and vice versa with W burst.

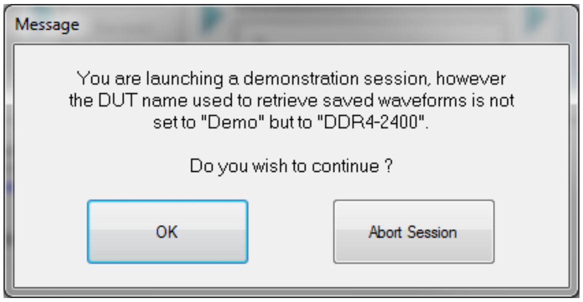


R/W Burst Detection Warning

<u>Solution</u>

Verify that the device has enough DQ and DQS transitions. Either the acquisition length or the burst density can be increased. To increase the acquisition length, adjust the *Clock Period Per Screen Division* variable.

DUT Name
When running in Demo mode, QualiPHY will issue a warning if the DUT name is not “Demo”. The DUT name entered should match the name of the folder containing the saved waveforms.



DUT Name Warning

<u>Solution</u>
Ensure that the DUT name matches the folder in which you have the saved waveforms. If it does, press “OK”.

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