TELEDYNE LECROY
Everywhereyoulook™

QPHY-LPDDR2

LPDDR2 Serial Data Compliance Software

Instruction Manual

Revision B – November, 2017

Relating to:

XStreamDSO™ v.8.5.x.x and later

QualiPHY Software v.8.5.x.x and later

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About This Manual

This manual assumes that you are familiar with using an oscilloscope–in particular the Teledyne LeCroy oscilloscope that will be used with QualiPHY–and that you have purchased the QPHY-LPDDR2 software option. Some of the images in this manual may show QualiPHY products other than QPHY-LPDDR2, or were captured using different model oscilloscopes, as they are meant to illustrate general concepts only. Rest assured that while the user interface may look different from yours, the functionality is identical.

Introduction

About QualiPHY

QualiPHY is highly automated compliance test software meant to help you develop and validate the PHY (physical-electrical) layer of a device, in accordance with the official documents published by the applicable standards organizations and special interest groups (SIGs). You can additionally set custom variables and limits to test compliance to internal standards.

QualiPHY is composed of a “framework” application that enables the configuration and control of separate tests for each standard through a common user interface. Features include:

- **Multiple Data Source Capability**
- **User-Defined Test Limits**: Tighten limits to ensure devices are well within the passing region, even if subsequently measured with different equipment.
- **Flexible Test Results Reporting** that includes XML Test Record Generation. Understand a device performance distribution, or obtain process related information from the devices under test.

About QPHY-LPDDR2

QPHY-LPDDR2 is an automated test package performing all of the real time oscilloscope tests for Double Data Rate in accordance with JEDEC Standard No. 209-2B.

The software can be run on any Teledyne LeCroy oscilloscope with at least 2.5 GHz bandwidth and 20 GS/s sampling rate.

Required Equipment

- Teledyne LeCroy real-time oscilloscope, ≥ 2.5 GHz BW, installed with:
    - XStreamDSO v.6.5.x.x minimum* with an activated QPHY-LPDDR2 option key
    - QualiPHY software v.6.5.x.x minimum with an activated QPHY-LPDDR2 component

  ***Note**: The versions of XStreamDSO and QualiPHY software must match, so upgrade your version of QualilPHY if you have upgraded your oscilloscope firmware. The versions listed above are the minimum versions required for this product. The QualiPHY software may be installed on a remote PC, but all other software must be run on the oscilloscope.
- Three or more ≥ 4 GHz bandwidth probes (voltage swing must be at least ± 2.5 Vp-p.)

  Note: Minimum 6 GHz bandwidth probes recommended.
- PCF200 Probe Deskew and Calibration Fixture (included with –PS probe systems)

Remote Host Computer System Requirements

Usually, the oscilloscope is the host computer for the QualiPHY software, and all models that meet the acquisition requirements will also meet the host system requirements. However, if you wish to run the QualiPHY software from a remote computer, these minimum requirements apply:

- Operating System:
  - Windows 7 Professional
  - Windows 10 Professional
- 1 GHz or faster processor
- 1 GB (32-bit) or 2 GB (64-bit) of RAM
- Ethernet (LAN) network capability
- Hard Drive:
  - At least 100 MB free to install the framework application
  - Up to 2 GB per standard installed to store the log database (each database grows from a few MB to a maximum of 2 GB)

See Set Up Remote Control for configuration instructions.

QPHY-LPDDR2 Basic Functionality

Signals Measured

The compliance test probes the following signals (# is the negative polarity of the differential signal):

CK, CK# Input

Differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output (read) data is referenced to the crossings of CK and CK# (both directions of crossing).

DQ Input/Output

Bi-directional data bus input/output.

DQS, DQS# Input/Output

Data strobe output with read data, input with write data. This signal is in phase with read data and 90 degrees out of phase with write data.

ADD/CTRL

Address and control signals can be measured in addition to the clock, data and strobe. Bank Address (BA0 – BA2), Chip Select (CS), Command Inputs (RAS, CAS and WE), Clock Enable (CKE) and On Die Termination (ODT) can all be specified as the signal under test.

Burst Access

The functionality is extracted from JEDEC Standard No. 209-2B.

Read and write accesses to the LPDDR2 SDRAM are burst oriented; accesses start at a selected location and continue for a burst length of four, eight, or sixteen in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command.

Prior to normal operation, the LPDDR2 SDRAM must be initialized.

Burst Read

The Burst Read command is initiated by having CS_n LOW, CA0 HIGH, CA1 LOW and CA2 HIGH at the rising edge of the clock. The command address bus inputs, CA5r-CA6r and CA1f-CA9f, determine the starting column address for the burst. The Read Latency (RL) is defined from the rising edge of the clock on which the Read Command is issued to the rising edge of the clock from which the tDQSCK delay is measured. The first valid datum is available RL * tCK + tDQSCK + tDQSQ after the rising edge of the clock where the Read Command is issued. The data strobe output is driven LOW tRPRE before the first rising valid strobe edge. The first bit of the burst is synchronized with the first rising edge of the data strobe. Each subsequent data-out appears on each DQ pin edge aligned with the data strobe. The RL is programmed in the mode registers

The minimum time from the burst read command to the burst write command is defined by the Read Latency (RL) and Burst Length (BL The minimum time from the burst read command to the burst write command is defined by a read-to-write-turn-around-time, which is four clocks in case of BL = 4 operation, six clocks in case of BL = 8 operation.

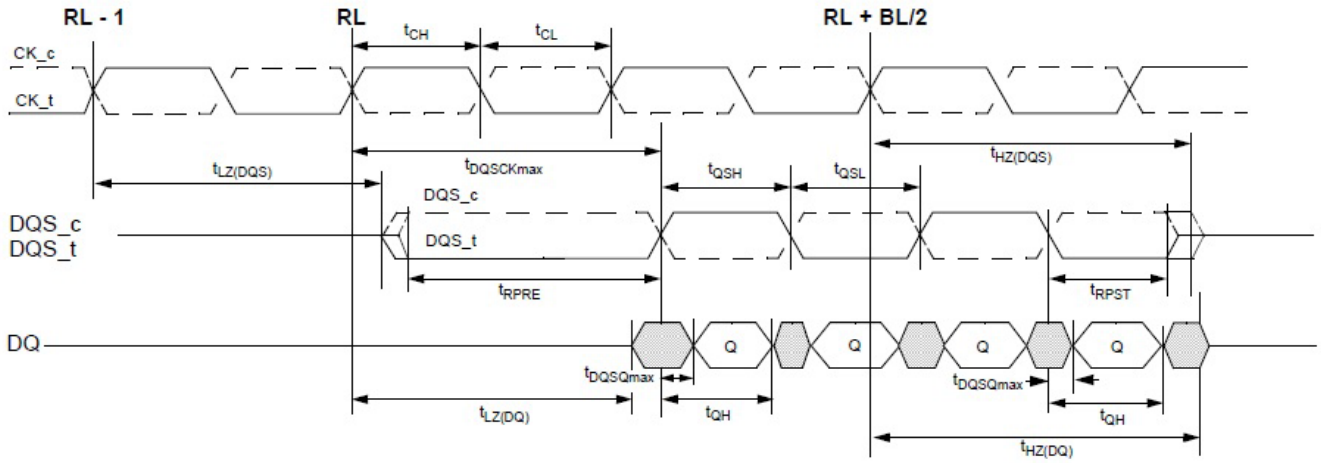


Figure 1. Data output (read) timing [JESD209-2D figure 23]

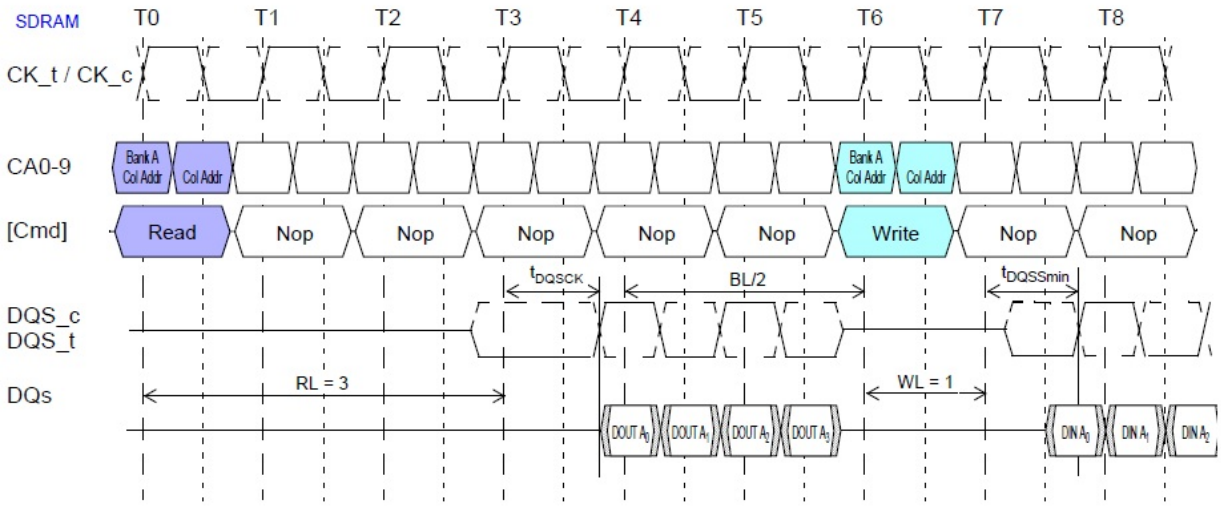


Figure 2. Burst read followed by burst write [JESD209-2D figure 32]

Burst Write

The Burst Write command is initiated by having CS_n LOW, CA0 HIGH, CA1 LOW and CA2 LOW at the rising edge of the clock. The command address bus inputs, CA5r-CA6r and CA1f-CA9f, determine the starting column address for the burst. The Write Latency (WL) is defined from the rising edge of the clock on which the Write Command is issued to the rising edge of the clock from which the tDQSS delay is measured. The first valid datum shall be driven WL * tCK + tDQSS from the rising edge of the clock from which the Write command is issued. The data strobe signal (DQS) should be driven LOW tWPRE prior to the data input. The data bits of the burst cycle must be applied to the DQ pins tDS prior to the respective edge of the DQS and held valid until tDH after that edge. The burst data are sampled on successive edges of the DQS until the burst length is completed, which is 4-, 8-, or 16-bit burst.

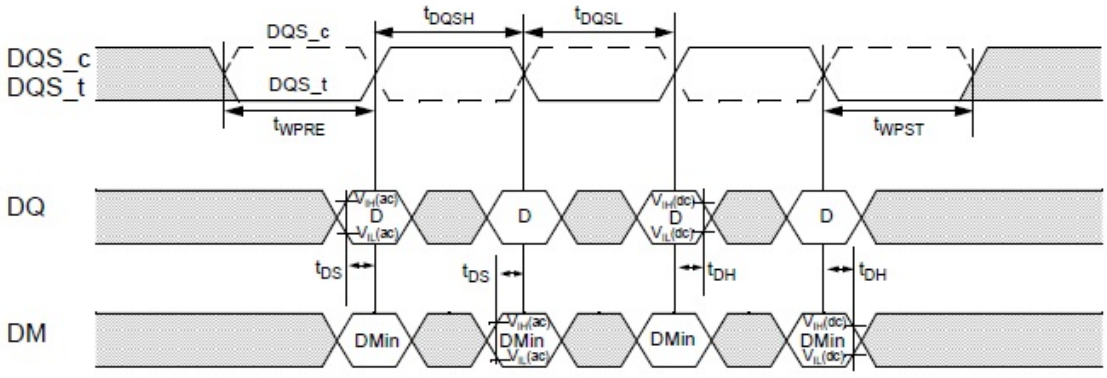


Figure 3. Data input (write) timing [JESD209-2D figure 40]

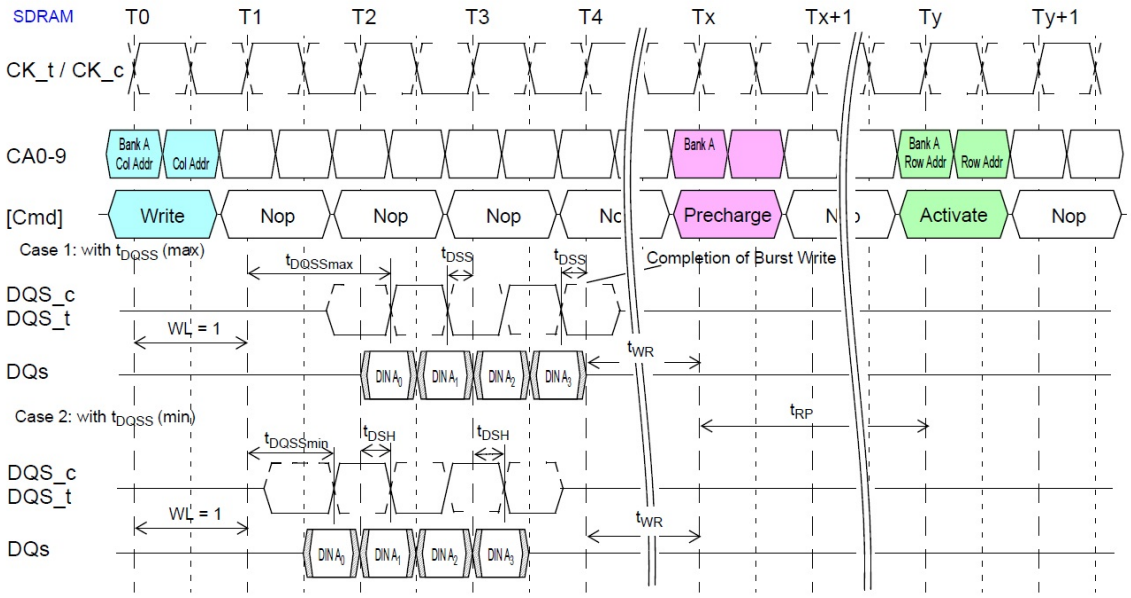


Figure 4. Burst write: WL = 1, BL = 4 [JESD209-2D figure 41]

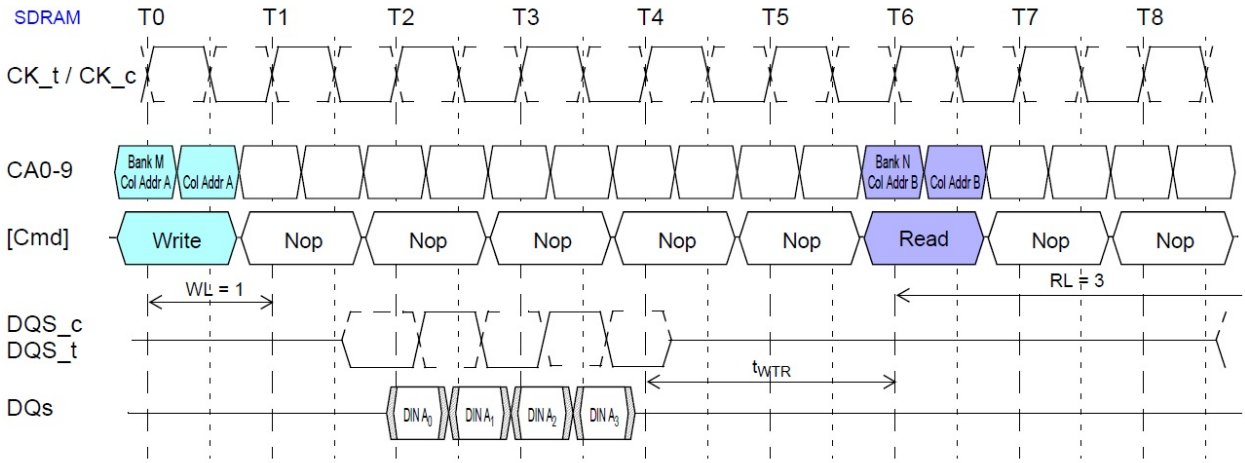


Figure 5. Burst write followed by burst read [JESD209-2D-2E figure 44]

Installation and Setup

QualiPHY is a Windows-based application that can be configured with one or more serial data compliance components. Each compliance component is purchased as a software option.

Install Base Application

Download the latest version of the QualiPHY software from:

teledynelecroy.com/support/softwaredownload under Oscilloscope Downloads > Software Utilities.

If the oscilloscope is not connected to the Internet, copy the installer onto a USB memory stick then transfer it to the oscilloscope desktop or a folder on a D:\ drive to execute it.

Run **QualiPHYInstaller.exe** and follow the installer prompts. Choose all the components you plan to activate. If you omit any components now, you will need to update the installation to activate them later.

By default, the oscilloscope appears as local host when QualiPHY is executed on the oscilloscope. Follow the steps under Add Connection to QualiPHY to check that the IP address is **127.0.0.1**.

Activate Components

The serial data compliance components are factory installed as part of the main application in your oscilloscope and are individually activated through the use of an alphanumeric code uniquely matched to the oscilloscope's serial number. This option key code is what is delivered when purchasing a software option.

To activate a component on the oscilloscope:

1. From the menu bar, choose **Utilities > Utilities Setup**.
2. On the Options tab, click **Add Key**.
3. Use the Virtual Keyboard to **Enter Option Key**, then click **OK**.

   If activation is successful, the key code now appears in the list of Installed Option Keys.
4. Restart the oscilloscope application by choosing **File > Exit**, then double-clicking the **Start DSO** icon on the desktop.

Set Up Dual Monitor Display

Teledyne LeCroy recommends running QualiPHY on an oscilloscope equipped with Dual Monitor Display capability. This allows the waveform and measurements to be shown on the oscilloscope LCD display while the QualiPHY application and test results are displayed on a second monitor.

See the oscilloscope Operator's Manual or Getting Started Manual for instructions on setting up dual monitor display.

Set Up Remote Control

QualiPHY software can be executed from a remote host computer, controlling the oscilloscope through a LAN Connection. To set up remote control:

- The oscilloscope must be connected to a LAN and assigned an IP address (fixed or dynamic).
- The host computer must be on the same LAN as the oscilloscope.

Configure Oscilloscope for Remote Control

1. From the menu bar, choose **Utilities → Utilities Setup...**
2. Open the **Remote** tab and set Remote Control to **TCP/IP**.
3. Verify that the oscilloscope shows an IP address.

Add Connection to QualiPHY

1. On the host PC, download and run **QualiPHYInstaller.exe**.
2. Start QualiPHY and click the **General Setup** button.
3. On the **Connection** tab, click **Scope Selector**.
4. Click **Add** and choose the connection type. Enter the oscilloscope IP address from Step 3 above. Click **OK**.
5. When the oscilloscope is properly detected, it appears on the Scope Selector dialog. Select the connection, and click **OK**.

   QualiPHY is now ready to control the oscilloscope.

Select Connection

Multiple oscilloscopes may be accessible to a single remote host. In that case, go to General Setup and use the Scope Selector at the start of the QPHY session to choose the correct connection.

QualiPHY tests the oscilloscope connection when starting a test. The system warns you if there is a connection problem.

Using QualiPHY

This section provides an overview of the QualiPHY user interface and general procedures. For detailed information about the QPHY-LPDDR2 software option, see QPHY-LPDDR2 Testing.

Accessing the Software

Once QualiPHY is installed and activated, it can be accessed from the oscilloscope menu bar by choosing **Analysis > QualiPHY**, or by double-clicking the **QualiPHY desktop icon** on a remote computer.

The QualiPHY framework dialog illustrates the overall software flow, from general set up through running individual compliance tests. Work from left to right, making all desired settings on each sub-dialog.

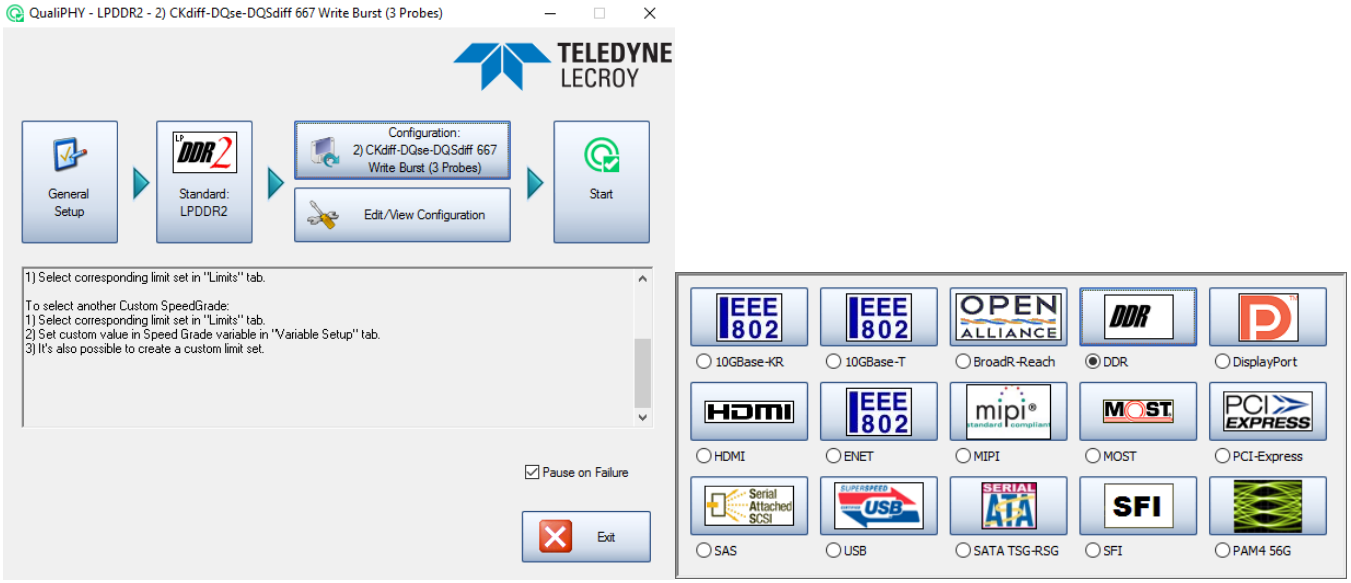


Figure 6. QualiPHY framework dialog and Standard selection menu

The sub-dialogs are organized into tabs each containing configuration controls related to that part of the process. These are described in more detail in the following sections.

If **Pause on Failure** is checked, QauliPHY prompts to retry a measure whenever a test fails.

Report Generator launches the manual report generator dialog.

The **Exit** button at the bottom of the framework dialog closes the QualiPHY application.

General Setup

The first sub-dialog contains general system settings. These remain in effect for each session, regardless of Standard, until changed.

Connection tab

Shows **IP Address** of the test oscilloscope (local host 127.0.0.1 if QualiPHY is run from the oscilloscope). The **Scope Selector** allows you to choose the oscilloscope used for testing when several are connected to the QualiPHY installation. See Set Up Remote Control for details.

Session Info tab

Optional information about the test session that may be added to reports, such as: **Operator Name**, **Device Under Test** (DUT), **Temperature** (in °C) of the test location, and any additional **Comments**. There is also an option to **Append Results** or **Replace Results** when continuing a previous session.

To optimize report generation, enter at least a DUT name at the beginning of each session.

Report tab

Settings related to automatic report generation. Choose:

- **Reporting behavior** of:
  - "Ask to generate a report after tests," where you'll be prompted to create a new file for each set of test results.
  - "Never generate a report after tests," where you'll need to manually execute the Report Generator to create a report.
  - "Always generate a report after tests," to autogenerate a report of the latest test results.
- **Default** report output type of XML, HTML, or PDF.
- A generic **Output file name**, including the full path to the report output folder.

Optionally, check **Allow style sheet selection in Report Generator** to enable the use of a custom .xslt when generating reports (XML and HTML output only). The path to the .xslt is entered on the Report Generator dialog.

Report Generator launches the Report Generator dialog, which contains the same settings as the Report tab, only applied to individual reports.

Advanced tab

This tab launches the **X-Replay Mode** dialog. See X-Replay Mode.

About tab

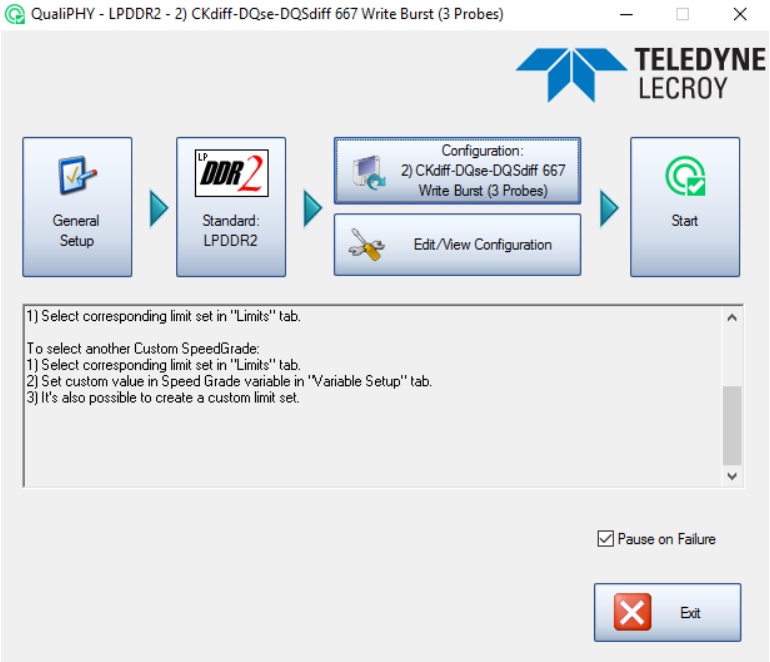
Information about your QualiPHY installation.

QualiPHY Test Process

Once general system settings are in place, these are the steps for running test sessions.

Set Up Test Session

1. Connect the oscilloscope to the DUT. See QPHY-LPDDR2 Testing Physical Setup.
2. Access the QualiPHY software to display the framework dialog.



3. If running QualiPHY remotely, click **General Setup** and open the **Scope Selector** to select the correct oscilloscope connection.
4. If you have more than one component activated, click **Standard** and select the desired standard to test against. Otherwise, your one activated component will appear as the default selection.

   Note: Although all the QualiPHY components appear on this dialog, only those selected when installing QualiPHY are enabled for selection.

5. Click the **Configuration** button and select the test configuration to run. These pre-loaded configurations are set up to run all the tests required for compliance and provide a quick, easy way to begin compliance testing. See QPHY-LPDDR2 Test Configurations for a description of your configurations.

   You can also create custom configurations for internal compliance tests by copying and modifying the pre-loaded configurations. See Customizing QualiPHY for details.

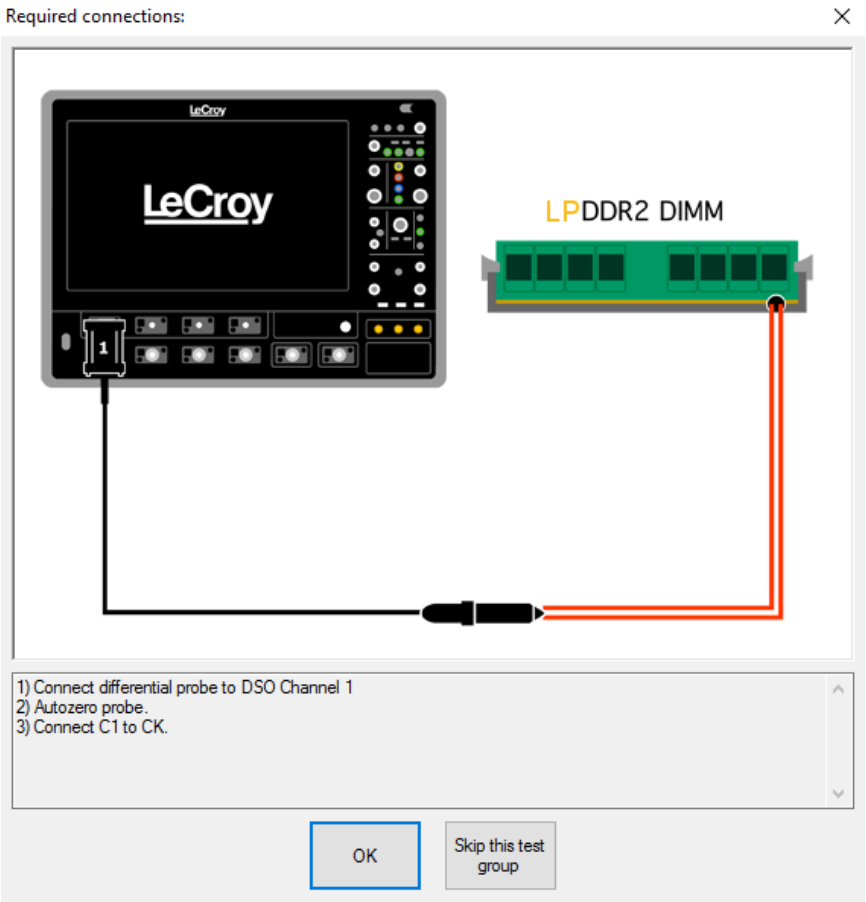
6. **Close** the Edit/View Configuration dialog to return to the framework dialog.

Run Tests

1. On the framework dialog, click **Start** to begin testing.

   When tests are in progress, this button changes to **Stop**. Click it at any time to stop the test in process. You'll be able to resume from the point of termination or from the beginning of the test.

2. Follow the pop-up window prompts. QualiPHY guides you step-by-step through each of the tests described in the standard specification, including diagrams of the connection to the DUT for each required test mode.



3. When all tests are successfully completed, both progress bars on the framework dialog are completely green and the message "All tests completed successfully" appears. If problems are encountered, you'll be offered options to:

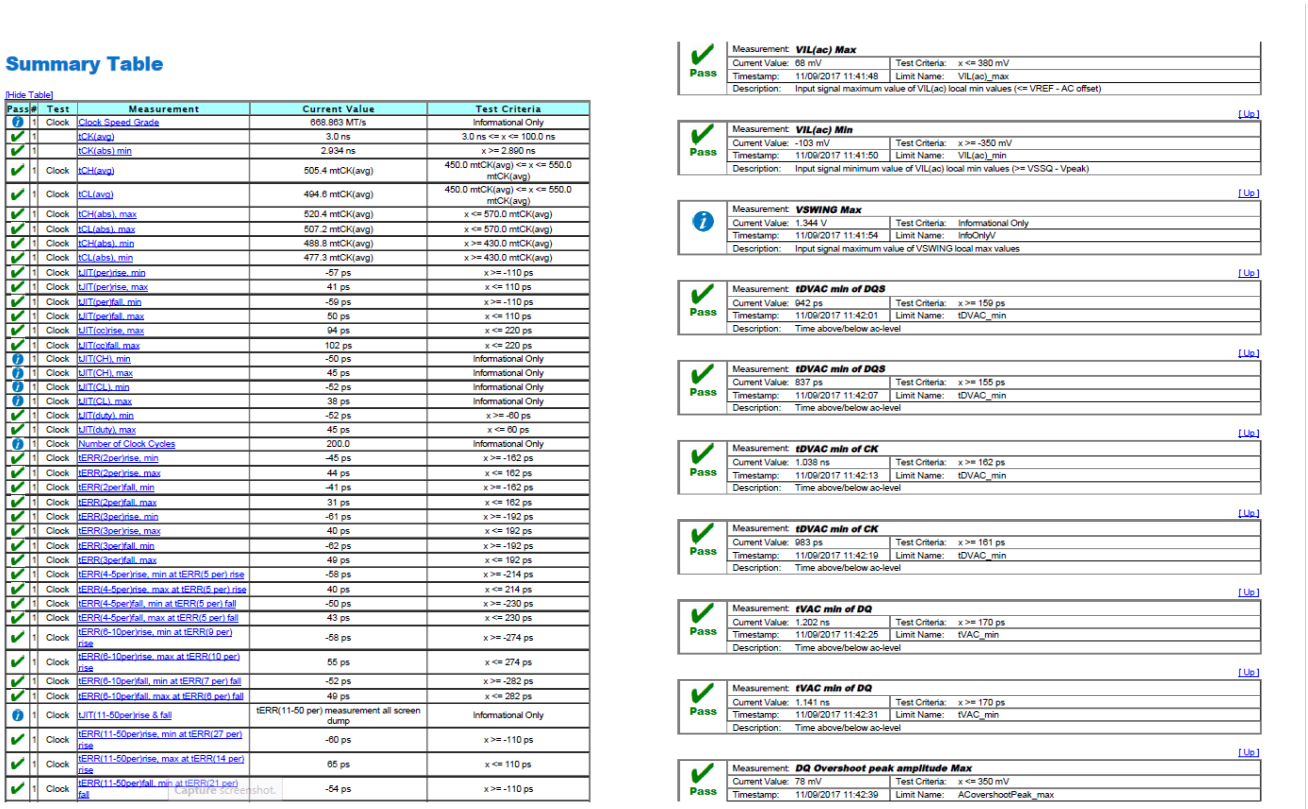
   - **Retry** the test from the latest established point defined in the script
   - **Ignore and Continue** with the next test
   - **Abort Session**

Generate Reports

The QualiPHY software automates report generation. On the framework dialog, go to **General Setup > Report** to pre-configure reporting behavior. You can also manually launch the **Report Generator** from the framework dialog once a test is run.

The Report Generator offers the same selections as the Report tab, only applied to each report individually, rather than as a system setting. This enables you to save reports for each test session, rather than overwrite the generic report file. There are also options to link a custom style sheet (.xslt) to the report, or to Exclude Informative Results.

The Test Report includes a summary table with links to the detailed test result pages.



Summary Table

[Hide Table]

Pass	#	Test	Measurement	Current Value	Test Criteria
ℹ	1	Clock	Clock Speed Grade	668.863 MT/s	Informational Only
✔	1		tCK(avg)	3.0 ns	3.0 ns <= x <= 100.0 ns
✔	1		tCK(abs) min	2.934 ns	x >= 2.890 ns
✔	1	Clock	tCH(avg)	505.4 mtCK(avg)	450.0 mtCK(avg) <= x <= 550.0 mtCK(avg)
✔	1	Clock	tCL(avg)	494.6 mtCK(avg)	450.0 mtCK(avg) <= x <= 550.0 mtCK(avg)
✔	1	Clock	tCH(abs), max	520.4 mtCK(avg)	x <= 570.0 mtCK(avg)
✔	1	Clock	tCL(abs), max	507.2 mtCK(avg)	x <= 570.0 mtCK(avg)
✔	1	Clock	tCH(abs), min	488.8 mtCK(avg)	x >= 430.0 mtCK(avg)
✔	1	Clock	tCL(abs), min	477.3 mtCK(avg)	x >= 430.0 mtCK(avg)
✔	1	Clock	tJIT(per)rise, min	-57 ps	x >= -110 ps
✔	1	Clock	tJIT(per)rise, max	41 ps	x <= 110 ps
✔	1	Clock	tJIT(per)fall, min	-59 ps	x >= -110 ps
✔	1	Clock	tJIT(per)fall, max	50 ps	x <= 110 ps
✔	1	Clock	tJIT(cc)rise, max	94 ps	x <= 220 ps
✔	1	Clock	tJIT(cc)fall, max	102 ps	x <= 220 ps
ℹ	1	Clock	tJIT(CH), min	-50 ps	Informational Only
ℹ	1	Clock	tJIT(CH), max	45 ps	Informational Only
ℹ	1	Clock	tJIT(CL), min	-52 ps	Informational Only
ℹ	1	Clock	tJIT(CL), max	38 ps	Informational Only
✔	1	Clock	tJIT(duty), min	-52 ps	x >= -60 ps
✔	1	Clock	tJIT(duty), max	45 ps	x <= 60 ps
ℹ	1	Clock	Number of Clock Cycles	200.0	Informational Only
✔	1	Clock	tERR(2per)rise, min	-45 ps	x >= -162 ps
✔	1	Clock	tERR(2per)rise, max	44 ps	x <= 162 ps
✔	1	Clock	tERR(2per)fall, min	-41 ps	x >= -162 ps
✔	1	Clock	tERR(2per)fall, max	31 ps	x <= 162 ps
✔	1	Clock	tERR(3per)rise, min	-61 ps	x >= -192 ps
✔	1	Clock	tERR(3per)rise, max	40 ps	x <= 192 ps
✔	1	Clock	tERR(3per)fall, min	-62 ps	x >= -192 ps
✔	1	Clock	tERR(3per)fall, max	49 ps	x <= 192 ps
✔	1	Clock	tERR(4-5per)rise, min at tERR(5 per) rise	-58 ps	x >= -214 ps
✔	1	Clock	tERR(4-5per)rise, max at tERR(5 per) rise	40 ps	x <= 214 ps
✔	1	Clock	tERR(4-5per)fall, min at tERR(5 per) fall	-50 ps	x >= -230 ps
✔	1	Clock	tERR(4-5per)fall, max at tERR(5 per) fall	43 ps	x <= 230 ps
✔	1	Clock	tERR(6-10per)rise, min at tERR(9 per) rise	-58 ps	x >= -274 ps
✔	1	Clock	tERR(6-10per)rise, max at tERR(10 per) rise	55 ps	x <= 274 ps
✔	1	Clock	tERR(6-10per)fall, min at tERR(7 per) fall	-52 ps	x >= -282 ps
✔	1	Clock	tERR(6-10per)fall, max at tERR(8 per) fall	49 ps	x <= 282 ps
ℹ	1	Clock	tJIT(11-50per)rise & fall	tERR(11-50 per) measurement all screen dump	Informational Only
✔	1	Clock	tERR(11-50per)rise, min at tERR(27 per) rise	-60 ps	x >= -110 ps
✔	1	Clock	tERR(11-50per)rise, max at tERR(14 per) rise	65 ps	x <= 110 ps
✔	1	Clock	tERR(11-50per)fall, min at tERR(21 per) fall	-54 ps	x >= -110 ps

Capture screenshot.

Pass — Measurement: ***VIL(ac) Max*** — Current Value: 68 mV — Test Criteria: x <= 380 mV — Timestamp: 11/09/2017 11:41:48 — Limit Name: VIL(ac)_max — Description: Input signal maximum value of VIL(ac) local min values (<= VREF - AC offset)

[Up]

Pass — Measurement: ***VIL(ac) Min*** — Current Value: -103 mV — Test Criteria: x >= -350 mV — Timestamp: 11/09/2017 11:41:50 — Limit Name: VIL(ac)_min — Description: Input signal minimum value of VIL(ac) local min values (>= VSSQ - Vpeak)

[Up]

ℹ — Measurement: ***VSWING Max*** — Current Value: 1.344 V — Test Criteria: Informational Only — Timestamp: 11/09/2017 11:41:54 — Limit Name: InfoOnlyV — Description: Input signal maximum value of VSWING local max values

[Up]

Pass — Measurement: ***tDVAC min of DQS*** — Current Value: 942 ps — Test Criteria: x >= 159 ps — Timestamp: 11/09/2017 11:42:01 — Limit Name: tDVAC_min — Description: Time above/below ac-level

[Up]

Pass — Measurement: ***tDVAC min of DQS*** — Current Value: 837 ps — Test Criteria: x >= 155 ps — Timestamp: 11/09/2017 11:42:07 — Limit Name: tDVAC_min — Description: Time above/below ac-level

[Up]

Pass — Measurement: ***tDVAC min of CK*** — Current Value: 1.038 ns — Test Criteria: x >= 162 ps — Timestamp: 11/09/2017 11:42:13 — Limit Name: tDVAC_min — Description: Time above/below ac-level

[Up]

Pass — Measurement: ***tDVAC min of CK*** — Current Value: 983 ps — Test Criteria: x >= 161 ps — Timestamp: 11/09/2017 11:42:19 — Limit Name: tDVAC_min — Description: Time above/below ac-level

[Up]

Pass — Measurement: ***tVAC min of DQ*** — Current Value: 1.202 ns — Test Criteria: x >= 170 ps — Timestamp: 11/09/2017 11:42:25 — Limit Name: tVAC_min — Description: Time above/below ac-level

[Up]

Pass — Measurement: ***tVAC min of DQ*** — Current Value: 1.141 ns — Test Criteria: x >= 170 ps — Timestamp: 11/09/2017 11:42:31 — Limit Name: tVAC_min — Description: Time above/below ac-level

[Up]

Pass — Measurement: ***DQ Overshoot peak amplitude Max*** — Current Value: 78 mV — Test Criteria: x <= 350 mV — Timestamp: 11/09/2017 11:42:39 — Limit Name: ACovershootPeak_max

Figure 7.The Test Report Summary Table and Details pages

Reports are output to the folder D:\QPHY\Reports, or C:\LeCroy\QPHY\Reports if QualiPHY is installed on a remote PC.

You can add your own logo to the report by replacing the file *\QPHY\StyleSheets\CustomerLogo.jpg.

The recommended maximum size is 250x100 pixels at 72 ppi, 16.7 million colors, 24 bits. Use the same file name and format.

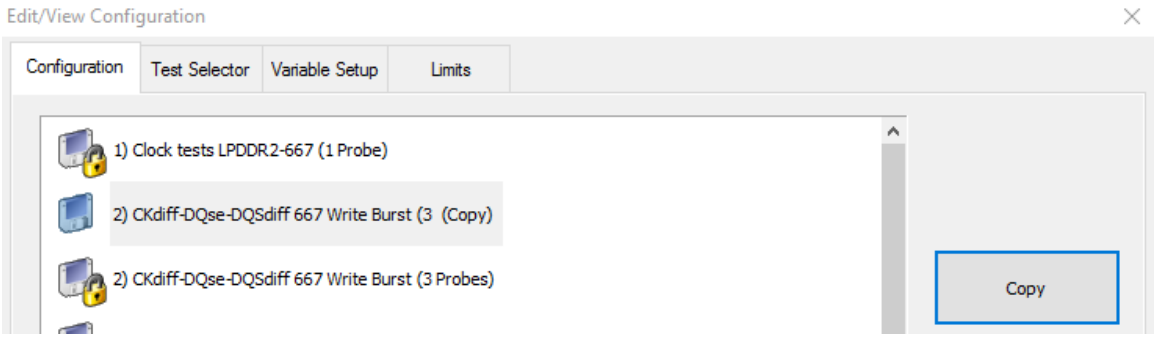
Customizing QualiPHY

Create custom test configurations by copying one of the standard configurations and modifying it. The pre-loaded configurations cannot be modified.

Copy Configuration

1. Access the QualiPHY framework dialog and select a **Standard**.
2. Click **Edit/View Configuration** and select the configuration upon which to base the new configuration. This can be a pre-loaded configuration or another copy.
3. Click **Copy** and enter a name and description. Once a custom configuration is defined, it appears on the Configuration tab with the defined name.

   Note: Until you enter a new name, the new configuration is shown followed by “(Copy)”.



4. Select the new, custom configuration and follow the procedures below to continue making changes.

   Note: When any configuration is changed, the Save As button at the bottom of the Configuration tab becomes active. When a custom configuration is changed, the Save button also becomes active to apply the changes to the existing configuration, rather than make another copy.

Select Tests

On the **Test Selector** tab, check the tests that make up the configuration. Each test is defined by the LPDDR2 standard. A description of each test is displayed when it is selected.

To loop an individual test or group of tests, select it from the list, then choose to **Loop selected test** until stopped or enter the number of repetitions. When defining a number of repetitions, enter the number of repetitions before selecting the checkbox.

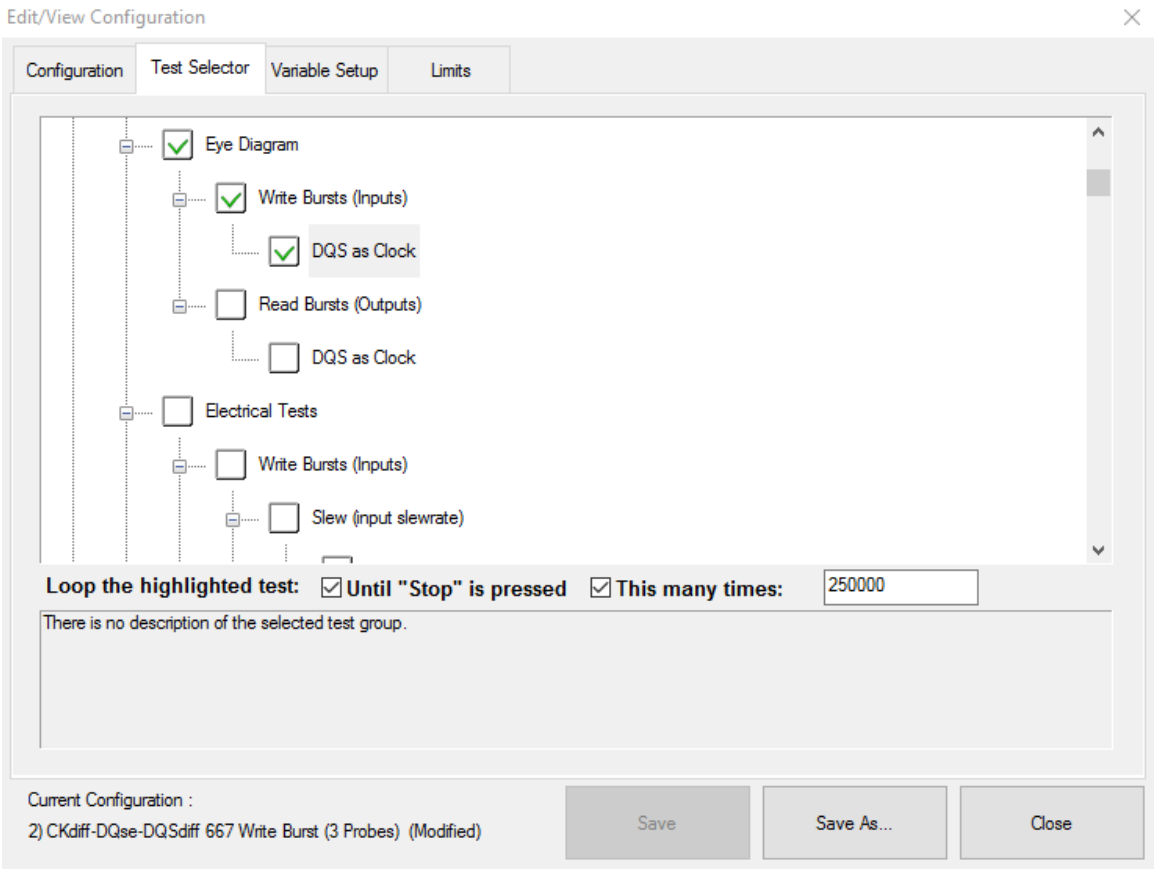


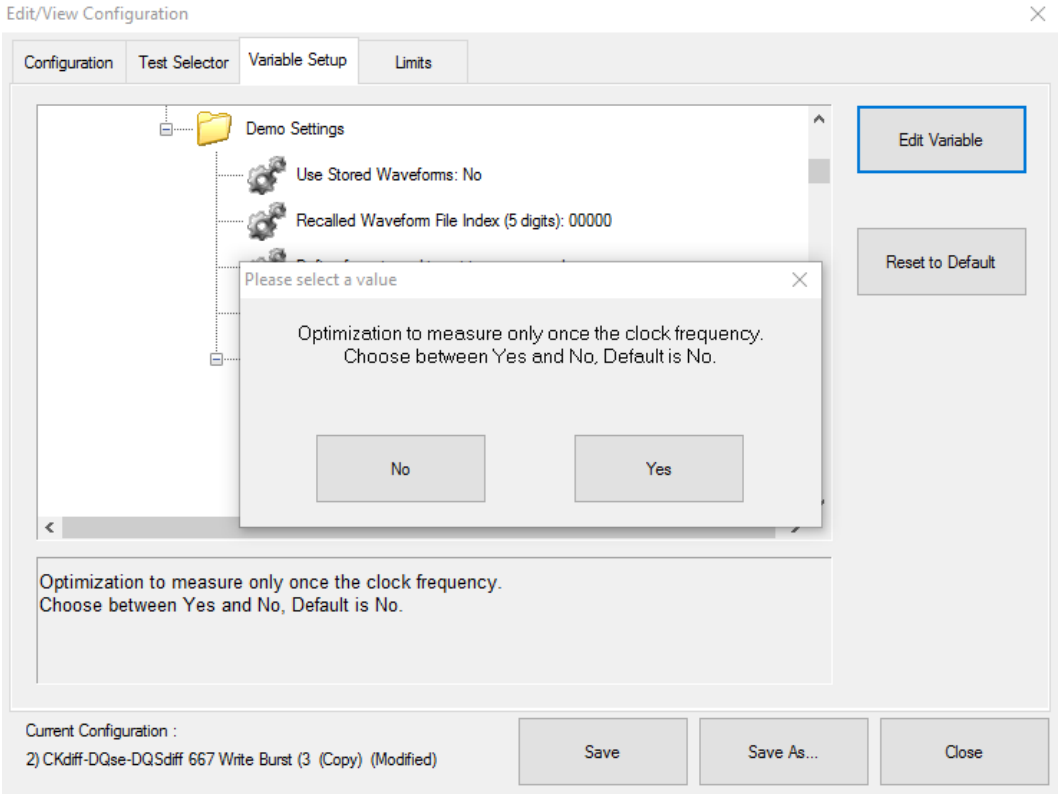
Figure 8. Configuration Test Selector Tab

Edit Variables

The Variable Setup tab contains a list of test variables. See QPHY-LPDDR2 Variables for a description of each.

To modify a variable:

1. Select the variable on the Variable Setup tab, then click **Edit Variable**. (You can also choose to Reset to Default at any time.)
2. The conditions of this variable appear on a pop-up. Choose the new condition to apply.



Edit Test Limits

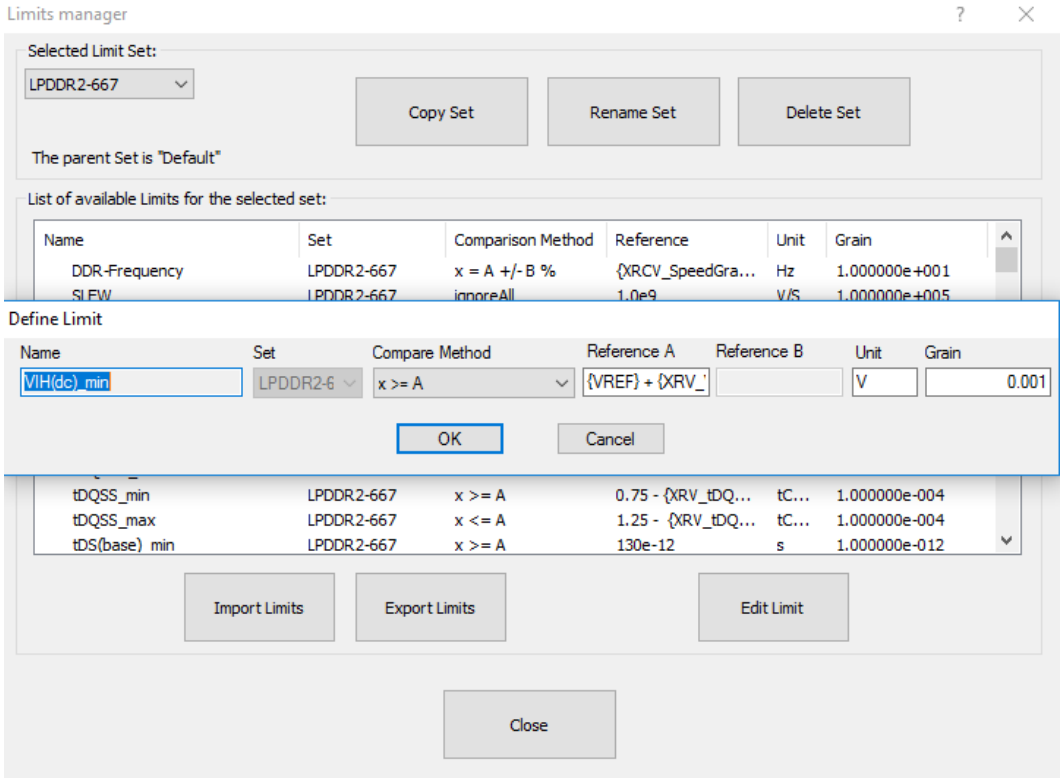
The Limits tab shows the Limit Set currently associated with the configuration. Any limit set can be associated with a custom configuration by selecting it in this field.

The Limits Manager shows the settings for every test limit in a limit set. Those in the default set are the limits defined by the standard.

To create a custom limit set:

1. On the Limits tab, click **Limits Manager**.
2. With the default set selected, click **Copy Set** and enter a name.

   Note: You can also choose to copy and/or modify another custom set that has been associated with this configuration.
3. Double click the limit to be modified, and in the pop-up enter the new values.



You can also **Import Limits** from a .csv file. Navigate to the file location after clicking the button.

Tip: Likewise, Export Limits creates a .csv file from the current limit set. You may wish to do this and copy it to format the input .csv file.

X-Replay Mode

The X-Replay mode window is an advanced (“developer”) view of QualiPHY. The tree in the upper-left frame enables you to navigate to processes in the LPDDR2 test script, in case you need to review the code, which appears in the upper-right frame.

Two other particularly useful features are:

- A **list of recent test sessions** in the lower-left frame. While you can only generate a report of the current test session in the QualiPHY wizard, in X-Replay Mode you can generate a report for any of these recent sessions. Select the session and choose **Report > Create Report** from the menu bar.
- The **QualiPHY log** in the bottom-right frame. The frame can be split by dragging up the lower edge. The bottom half of this split frame now shows the **raw Python output**, which can be useful if ever the script needs debugging.

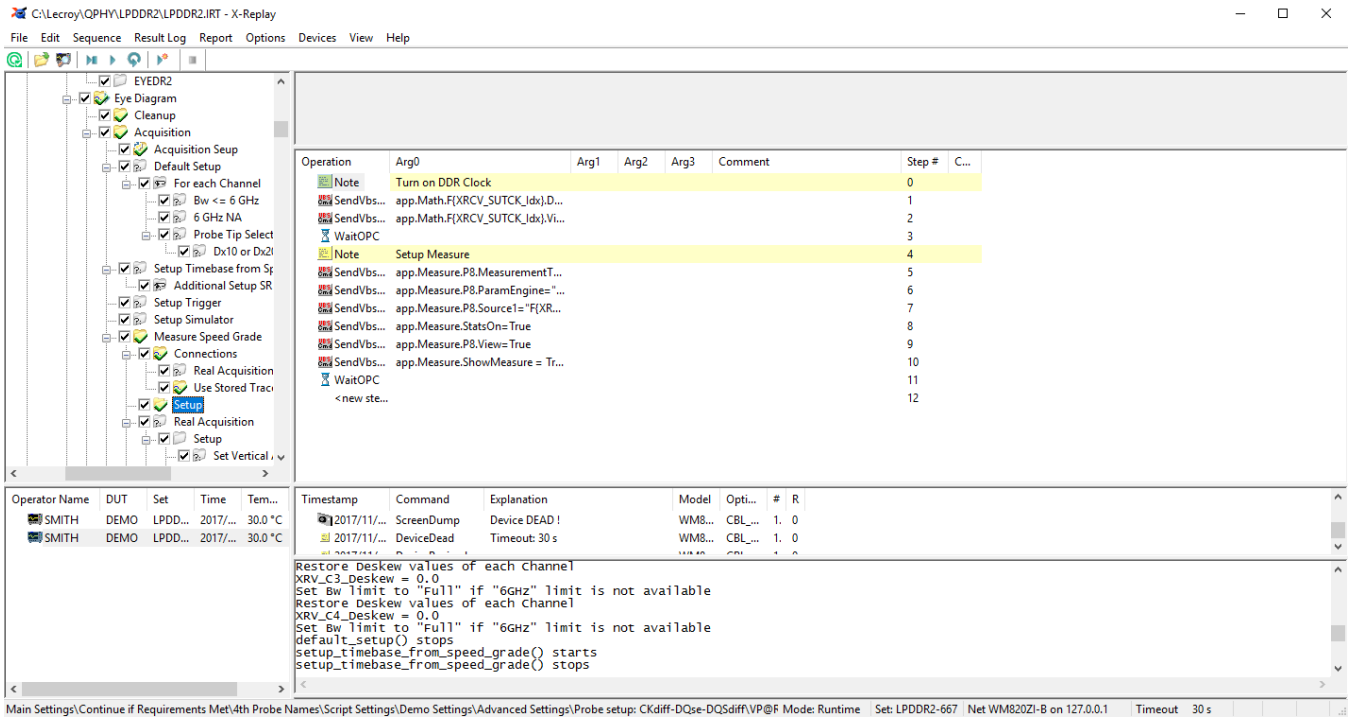


Figure 9. X-Replay Mode window

QPHY-LPDDR2 Testing

Test Preparation

Before beginning any test or data acquisition, the oscilloscope should be warmed for at least 20 minutes.

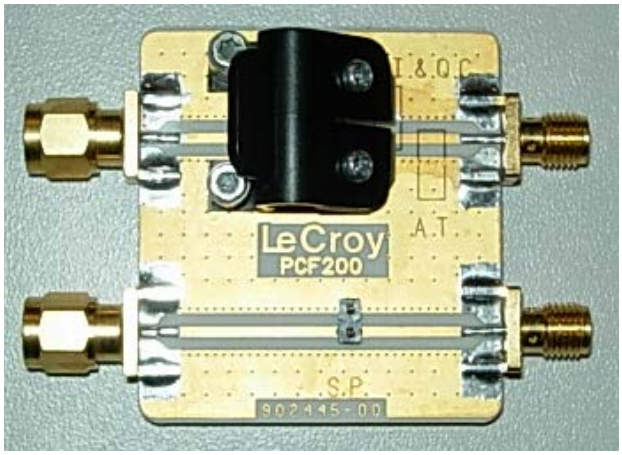
Calibration is automatically performed by the oscilloscope software; no manual calibration is required. The calibration procedure will be run again if the temperature of the oscilloscope changes by more than a few degrees.

Deskewing the Probes

For DDR measurements, it is crucial to make sure that probes are properly deskewed before running QPHY-LPDDR2 to ensure proper signal timing. Ideally, the same settings should be used when deskewing as when acquiring signals for analysis. This will ensure that the channels are deskewed using the same setup as when running conformance tests. Deskew values are saved and stored by QualiPHY at the beginning of each run.

Required Equipment

- PCF200 (included with “-PS” probe systems)



- Square-Pin (SP) tip (included with D4x0-PS, D6x0-PS, and Dxx30-PS)
- 50 Ω terminator

  Note: Alternatively an LPA-K-A adapter and a SMA cable could be used

Methodology

Before beginning the procedure, be sure to warm the oscilloscope for at least 20 minutes.

1. Connect the PCF200 to the oscilloscope's fast edge output. The PCF200 fixture has two different signal paths that can be used, depending on the type of probe tip being used for the measurement:

   - The upper signal path is for deskewing Solder-In (SI), Quick-Connect (QC) and Adjustable Tip (AT) probe tips.
   - The lower circuit is for Square-Pin (SP) probe tips.

   Depending upon which probe tip is being used, connect the appropriate signal path to the fast edge output. For ease of connectivity it is recommended that SP tip is used. As long as the same tip is used to deskew each probe it does not matter which style of probe tip is used.

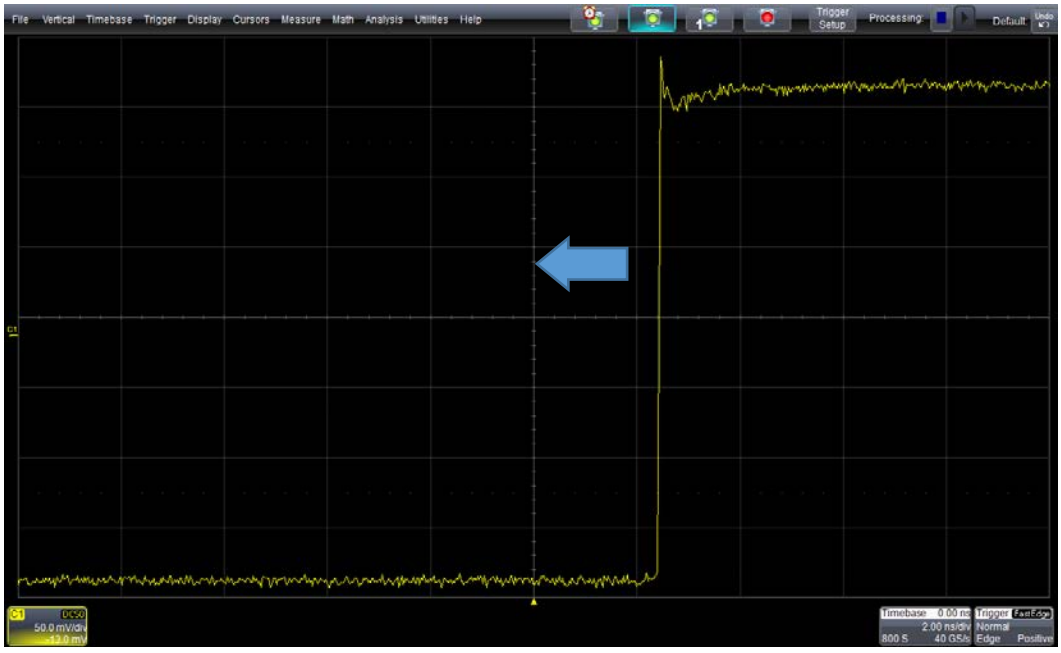
2. Connect probes electrically in a single-ended arrangement using their designated area on the fixture:

   - Connect the positive side of the probe to the signal trace (in between the two white strips). The positive polarity is indicated on the tip of the probe by a plus sign.
   - Connect the negative side to the ground plane (outside of the white strips).
   - In order to minimize reflections, apply a 50 Ω terminator to the end of the signal path in use. If a 50 Ω terminator is not available, an SMA cable can be used to terminate the PCF200 to one of the oscilloscope's outputs.

3. Set the oscilloscope **Trigger Source** to **Fast Edge**, **Trigger Type** to **Edge**.

4. Set a **Timebase** of approximately **10 ns/div** and **Timebase Delay** of **0.**

   Once everything is properly set up the oscilloscope display should look similar to the figure below. If there is no propagation delay due to the probe, and no internal oscilloscope channel propagation delay, the 50% trigger level will be at the center line of the oscilloscope grid.



5. From the channel setup dialog (C*n*):
    - Enable **Sinx/x** interpolation and set the **Averaging** to **50** sweeps.
    - Touch the **Deskew** field once to highlight it, then adjust the deskew value to move the rising edge of the trace to the center of the display.
6. Now, decrease the **Timebase** to around **20 ps/div** and once again adjust the **Deskew** value so that the 50% rising edge point is centered in time.

Repeat this procedure for each probe using the same probe tip.

Note: Before moving on to the next probe, reset Averaging to 1 sweep and turn off Sinx/x interpolation.

When QualiPHY is started the deskew values from each channel dialog are saved and stored by QPHY at the beginning of each run. However, at the end of the testing these values will be erased. By saving a panel setup it is possible to refer to the deskew values after testing has completed.

Connecting the Probes

Determining Signals to Access

The required signals to probe depend up on which tests are being run in QPHY-LPDDR2. The tests are broken up into different “Probe Setups” to allow the user to easily see which signals are required for a particular test. You can view each of the probe setups in the Test Selector tab.

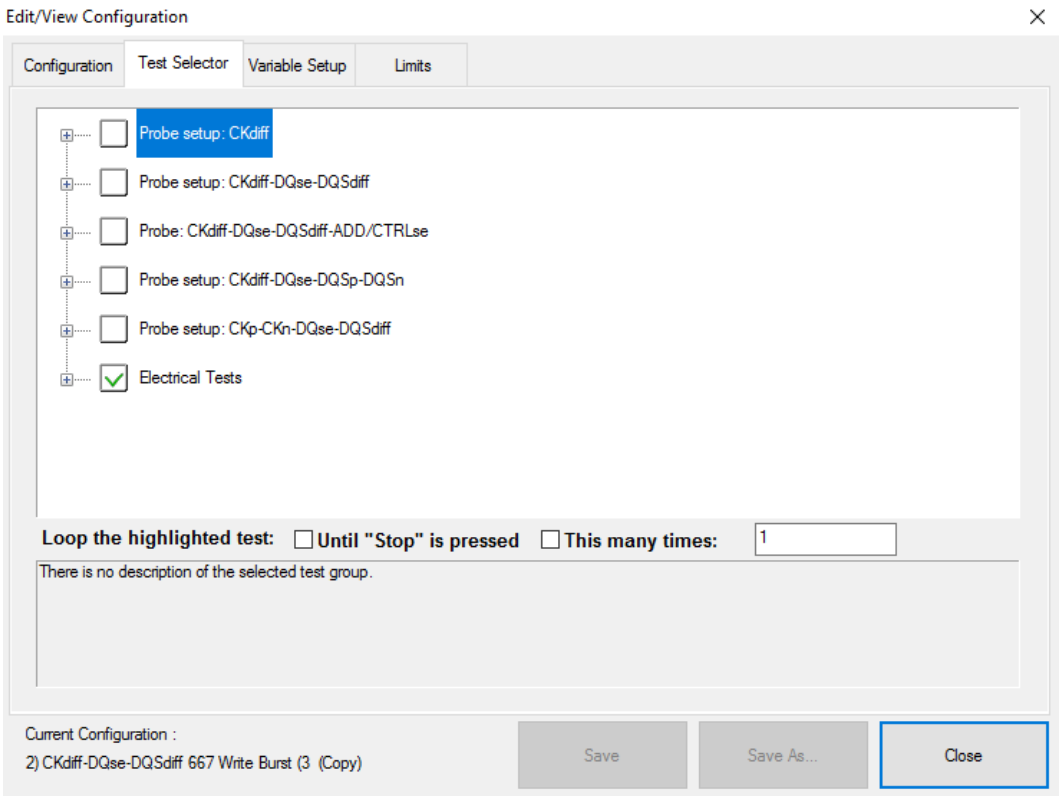


Figure 10. QPHY-LPDDR2 Probe Setups

Best Places to Probe

The DDR specification is defined at the balls of the DRAM so the probes should be placed as close to the DRAM as possible in order to closely follow the specification. This is important to minimize reflections on the signals. However, in some situations it can make sense to place the probes as close to the controller as possible. For example, if the user is a controller designer and is only interested in verifying the performance of the controller. It should be noted that some of the limits may not be applicable in this scenario.

One of the most desirable locations for probing is at the back side of the vias. This will generally result in good signal integrity; however, these may not always be accessible. Another alternative is to use an interposer such as the ones available from Nexus Technologies. No matter where the probes are placed it is essential to ensure that the probing points are equidistant from the DRAM. This will ensure that there is no additional skew introduced for timing measurements.

Read (R) and Write (W) Burst Requirements

R/W Burst Detection

QPHY-LPDDR2 separates R and W burst depending upon the skew between the data (DQ) and strobe (DQS) signals. For a W burst, QPHY expects to see that the DQ and DQS signals are approximately a quarter cycle out of phase. For an R burst, QPHY expects that the DQ and DQS signals are in phase.

R/W Burst Generation

It is recommended to capture a minimum of 10 R and 10 W bursts during each acquisition, but for greater statistical significance, it is encouraged to capture more. Programs which can communicate with the DRAM and controller are widely available online. One example is Memtest86+, which is available for download from memtest.org. When using Memtest, it is recommended to use test mode 7, which will randomly generate both R and W bursts. Additionally, a custom program can be used to stimulate the DUT.

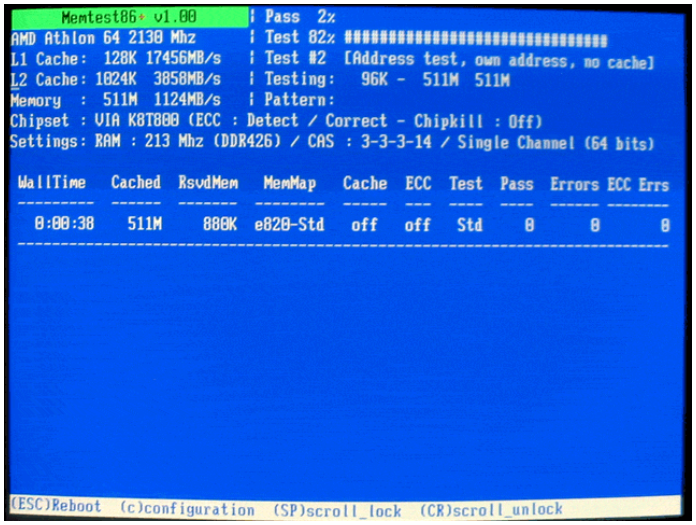


Figure 11. Memtest86+

Initial Signal Checking

Before running QPHY-LPDDR2, check the signals to verify that they make sense. This section covers some of the basic things which should be verified by the operator before running QPHY-LPDDR2.

Expected Channels

By default, QPHY-LPDDR2 expects to see the Clock (CK) on CH1, Strobe (DQS) on CH2 and Data (DQ) on CH3. This is what is shown in the connection diagram. The Input Channel variable can always be used to modify any of these channel assignments

Signal Amplitude

For best results, it is recommended that the signals take up 80% of the vertical grid.

Clock Frequency

By applying the Frequency measurement parameter to the CK signal, the user can verify that the DDR system is running at the expected transfer rate (Transfer Rate =Frequency * 2). This will also help in the limit selection. Do a quick visual inspection to ensure that the signal does not have any non-monotonic edges due to reflections.

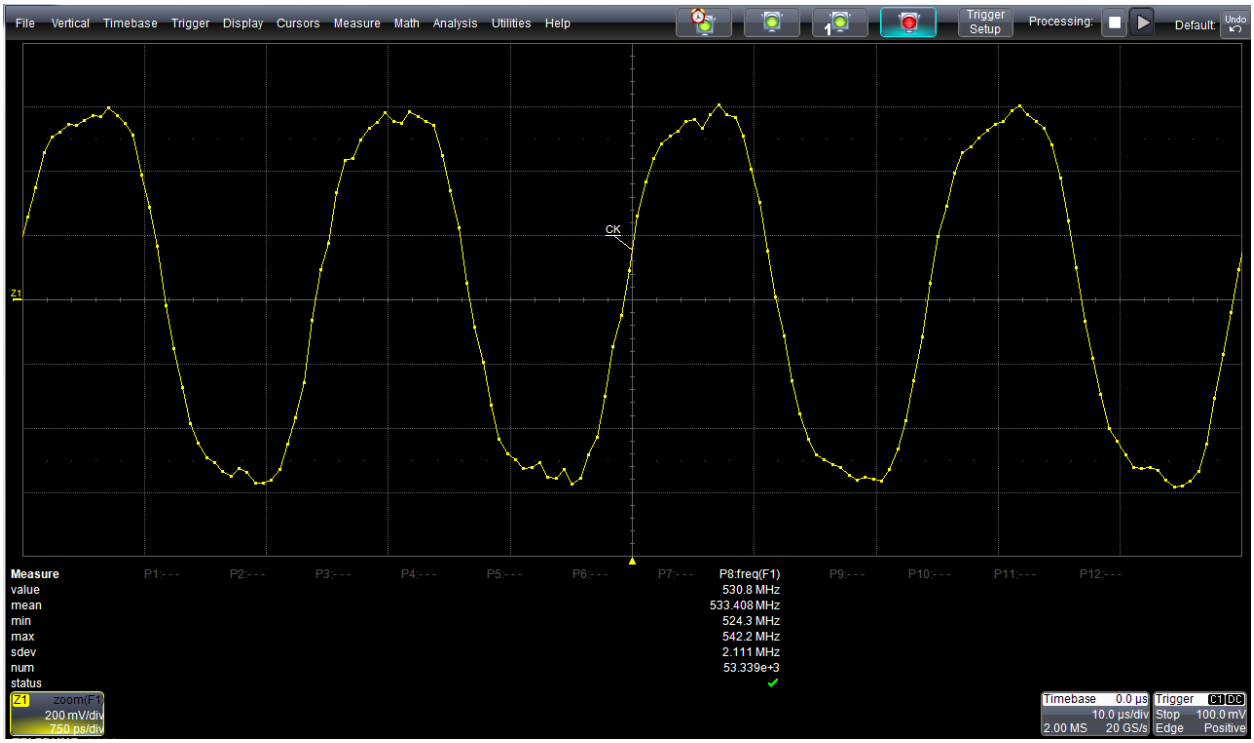


Figure 12. Verification of CK signal

Presence of R/W Burst

The operator should do a quick check to make sure their device is outputting the expected bursts. As a general rule of thumb, during a R burst DQ and DQS should be in phase and during a W burst DQ and DQS should be a quarter cycle out of phase. Additionally, the signal amplitude can be used to determine the presence of R and W bursts. If probing at the memory, R bursts will have a larger amplitude than W bursts.

Check Idle Levels

Before running QPHY-LPDDR2, validate the signal idle levels. Signal idle levels that are off will have an impact on the R/W burst detection, electrical, and timing measurements. DQS should have an idle level of ~ 0 mV. DQ should have an idle level of ~ VDD/2 (600 mV for LPDDR2).

QPHY-LPDDR2 Test Configurations

Clock tests LPDDR2-667 (1 Probe)

This configuration runs all of the clock tests using a single differential probe setup. All of the variables are set to their defaults. The limit set in use is DDR2-667. The tests run are:

Clock Tests

- tCK(avg), tCK(abs)
- tCH(avg), tCL(avg), tCH(abs), tCL(abs)
- tJIT(duty)
- tJIT(per)
- tJIT(CC)
- tERR(n per)

Electrical Tests

- Supply
    - Level

CKdiff-DQse-DQSdiff 667 Write Burst (3 Probes)

This configuration runs all LPDDR2 conformance tests available on write bursts when signals CKdiff-DQse-DQSdiff are connected. Use fixed Gain and Offset adapted to LPDDR2 levels. The tests run are:

Probe Setup CKdiff-DQse-DQSdiff

- Eye Diagram Tests
    - Write Bursts (Inputs), DQS as Clock
- Electrical Tests
    - Write Bursts (Inputs)
        - Slew
            - Slew R
            - Slew F
        - Logic Levels
            - VIH(ac)
            - VIL(ac)
            - VSWING
        - Time Above AC Level
            - tDVAC
            - tVAC
        - AC Over/Undershoot
            - AC Overshoot Peak Amplitude
            - AC Overshoot Area above VDDQ
            - AC Undershoot Peak Amplitude
            - AC Undershoot Area below VSSQ

        - AC Over/Undershoot_DQS_CK
            - AC Overshoot Peak Amplitude
            - AC Overshoot Area above VDDQ
            - AC Undershoot Peak Amplitude
            - AC Undershoot Area below VSSQ
    - Timing Tests
        - Write Bursts (Inputs)
            - Tests on bits (not using interpolation)
                - tDQSS
                - tDQSH
                - tDQSL
                - tDIPW
                - tDSS
                - tDSH
                - tDS (derated)
                - tDH (derated)
                - tDS (vref based)
                - tDH (vref based)

Probe Setup CKdiff-DQse-DQSp-DQS-n

- Electrical Tests
    - Write Bursts (Inputs)
        - Logic Levels
            - VSEH(ac)
            - VSEL(ac)
        - VIX(ac)
        - AC Over/Undershoot
            - AC Overshoot Peak Amplitude
            - AC Overshoot Area above VDDQ
            - AC Undershoot Peak Amplitude
            - AC Undershoot Area below VSSQ
        - Slew (input slewrate)
            - SlewR
            - SlewF

Electrical Tests

- Supply
    - Level

CKdiff-DQse-DQSdiff 667 Read Burst (3 Probes)

This configuration runs all LPDDR2 conformance tests available on read bursts when signals CKdiff-DQse-DQSdiff are connected. All of the variables are set to their defaults. The limit set in use is DDR2-667. The tests run are:

Probe Setup CKdiff-DQse-DQSdiff

- Eye Diagram
  - Read Bursts (Outputs)
- Electrical Tests
  - Read Bursts (Outputs)
    - Logic Levels
      - VOH(ac)
      - VOL(ac)
      - VSWING
    - SRQ (output slewrate)
      - Rise
      - Fall
- Timing Tests
  - Read Bursts (Outputs)
    - Tests on bits (no interpolation)
      - tDQSQ
      - tQSH
      - tQSL
      - tQHP
      - tQH
      - tQHS
      - tDQSCK

Electrical Tests

- Supply
  - Level

Eye Diagram (3 Probes Debug)

This configuration runs the Eye Diagram tests on both the read bursts and the write bursts using the probe setup CKdiff-DQse-DQSdiff. All of the variables are set to their defaults. The limit set in use is DDR2-667. The tests run are:

Probe Setup CKdiff-DQse-DQSdiff

- Eye Diagram – Write Bursts (Inputs)
- Eye Diagram – Read Bursts (Outputs)

Electrical Tests

- Supply
    - Level

Addr/Cmd Tests LPDDR2-667 (4 Probes)

This configuration runs all Address or Command line tests. Use fixed value for Gain and Offset adapted to LPDDR2 levels. All of the variables are set to their defaults. The limit set in use is DDR2-667. The tests run are:

Probe setup CKdiff-DQse-DQSdiff-ADD/CTRLse

- Electrical Tests
    - Write Bursts (Inputs)
        - Slew
            - Slew R
            - Slew F
        - Logic Levels
            - VIH(ac)
            - VIH(dc)
            - VIL(ac)
            - VIL(dc)
            - VSWING
        - AC Over/Undershoot
            - AC Overshoot Peak Amplitude
            - AC Overshoot Area above VDDQ
            - AC Undershoot Peak Amplitude
            - AC Undershoot Area below VSSQ

- Timing Tests
    - Write Bursts (Inputs)
        - tIS (base+derated)
        - tIH(base+derated)
        - tIPW
        - tIS(vref)
        - tIH(vref)

Electrical Tests

- Supply
    - Level

PrePostAmble Tests (3 Probes)

This configuration will run all LPDDR2 timing tests available on Preambles and Postambles when signals CKdiff-DQse-DQSdiff are connected. Use fixed value for Gain and Offset adapted to LPDDR2 levels. The results of these measurements depend on the manner in which the signal returns to idle and in some cases will not give the intended results. In addition, the method for measurement is not completely defined by the LPDDR2 specification (see JESD209-2E, figure 120). For these reasons, if you choose to run these tests, do with care. The tests run are:

Probe Setup CKdiff-DQse-DQSdiff

- Timing Tests
    - Read Bursts (Outputs)
        - PrePostable tests using interpolation
            - tHZ(DQ)
            - tLZ(DQ)
            - tHZ(DQS)
            - tLZ(DQS)
            - tRPRE
            - tRPST
    - Write Bursts (Inputs)
        - Tests on PrePostamble using interpolation
            - tWPRE
            - tWPST

Electrical Tests

- Supply
    - Level

Demo of All Tests

This configuration uses saved waveforms in oscilloscope D:\Waveforms\LPDDR2 to run all of the LPDDR2 tests listed above. All variables are set to their defaults, except Use Stored Waveforms is set to Yes and Use Stored Trace for Speed Grade is set to Yes. The limit set in use is LPDDR2-667.

QPHY-DDR2 Test Descriptions

These are the standard DDR2 compliance tests.

Clock Tests

All time measure on clock CK are done at level VREF.

tCK(avg), Average Clock Period

tCK(avg) is defined as the average clock period over any 200 consecutive clock periods.

tCK(avg) = SUM(tCKi) / 200 where i=1 to 200

Measured on both the rising and the falling edge.

tCK(abs), Absolute Clock Period

tCK(abs) is defined as the absolute clock period of each of 200 consecutive clock periods.

Measured on both the rising and the falling edge.

tCH(avg), Average High Pulse Width

tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses. See Figure 13.

tCH(avg) = SUM(tCHi) / (200 x tCK(avg)) where I = 1 to 200

tCL(avg), Average Low Pulse Width

tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

tCL(avg) = SUM(tCLi) / (200 x tCK(avg)) where i=1 to 200

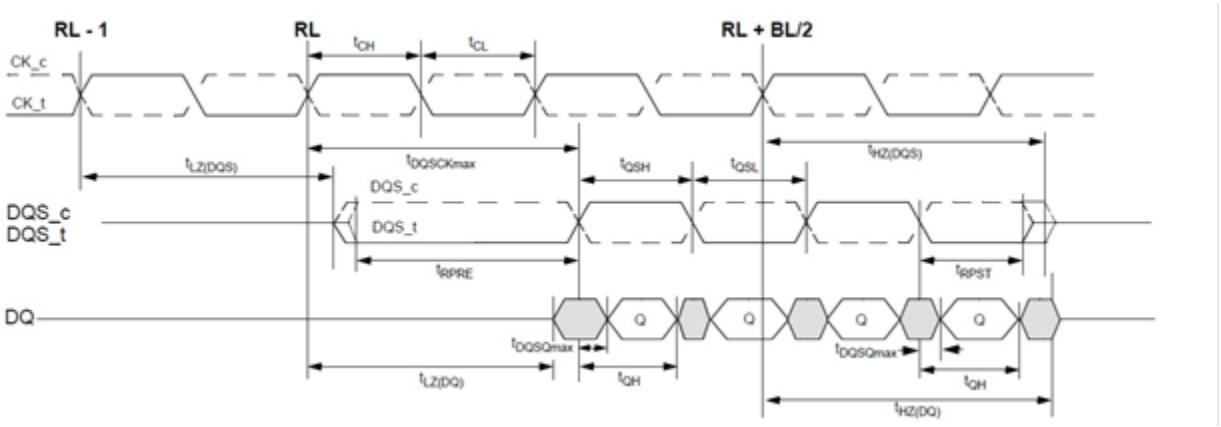


Figure 13. Data output (read) timing [JESD209-2D figure 23]

tCH(abs), Absolute High Pulse Width

tCH(abs) is defined as the absolute high pulse width, of each of 200 consecutive high pulses.

tCL(abs), Absolute Low Pulse Width

tCL(abs) is defined as the absolute low pulse width of each of 200 consecutive low pulses.

tJIT(duty), Half Period Jitter

tJIT(duty) is defined with absolute and average specification of tCH jitter and tCL jitter.

tJIT(duty),min = MIN((tCH(abs),min–tCH(avg),min), (tCL(abs),min–tCL(avg),min)) x tCK(avg)

tJIT(duty),max = MAX((tCH(abs),max–tCH(avg),max), (tCL(abs),max–tCL(avg),max)) x tCK(avg)

tJIT(per), Clock Period Jitter

tJIT(per) is defined as the largest deviation of any single tCK from tCK(avg). This test compares the average clock period (over 200 cycles) with each period inside the window. The smallest and largest values must be within limits.

tJIT(per) = Min/max of {tCKi - tCK(avg)} where i=1 to 200

Measured on both the rising and the falling edge.

There are different limits depending on whether the DLL is already locked or not:

- tJIT(per) defines the single period jitter when the DLL is already locked.
- tJIT(per,lck) uses the same definition for single period jitter, during the DLL locking period only.

A configuration variable allows to define which limit to use.

tJIT(cc), Cycle to Cycle Period Jitter

tJIT(cc) is defined as the difference in clock period between two consecutive clock cycles. This test compares the smallest and largest values of the difference between any two consecutive clock cycles inside a 200 cycles window.

tJIT(cc) = Min/max of {tCKi+1 – tCKi} where i = 1 to 199

Measured on both the rising and the falling edge.

There are different limit depending on whether the DLL is already locked or not:

- tJIT(cc) defines the cycle to cycle jitter when the DLL is already locked.
- tJIT(cc,lck) uses the same definition for cycle to cycle jitter, during the DLL locking period only.

A configuration variable allows to define which limit to use.

tERR(n per), Cumulative Error

tERR is defined as the cumulative error across multiple consecutive cycles from tCK(avg). This test compares the average clock period (over 200 cycles) with each n-bit period inside the window. The smallest and largest values must be within limits.

There are 12 different tests:
tERR(*n*per), (*n*→2,3,4,5,6,7,8,9,10,12,13,14…49,50)

tERR(*n*per) = Min/max of {SUM(tCK*i*) - *n* x tCK(avg)}

where *i*=1 to *n* and:

n = 2 for tERR(2per)

n = 3 for tERR(3per)

n = 4 for tERR(4per)

n = 5 for tERR(5per)

(and so forth until *n* = 12)

13 ≤ *n* ≤ 50 for tERR(11-50per)

Measured on both the rising and the falling edge.

Eye Diagram Tests

Write Burst (Inputs)

This is an informational only test that creates the eye diagram of all the write bursts found in the acquisition.

Read Burst (Outputs)

This is an informational only test that creates the eye diagram of all the read bursts found in the acquisition.

Electrical Tests on Write Bursts (Inputs)

Slew (input slew rate): SlewR and SlewF

Refer to section 8.6 of the JESD209-2D for single-ended input signals and to section 8.7 for slew rate for differential signals.

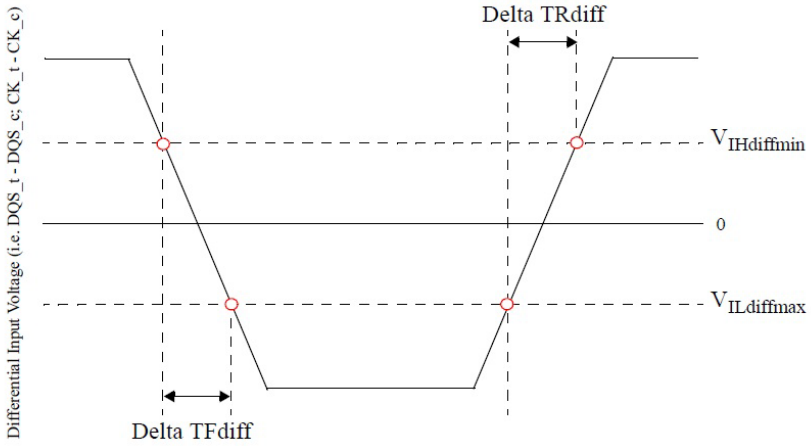


Figure 14. Differential Input Slew Rate Definitions [JESD209-2D figure 111]

Logic Levels

VIH(ac), maximum AC input logic high
Measures the local maximum value from VREF to VREF of the high pulse histogram. If multiple pulses are measured, take the lowest number and the highest number as the worst cases.

The lowest number must be greater than or equal to the minimum limit and the highest number must be less than or equal to the maximum limit.

VIH(dc), minimum DC input logic high
Measures the local minimum and maximum values from the first VIH(ac)min crossing point to the time corresponding to VIH(dc)min crossing a 1V/ns slewrate slope to VREF. If multiple pulses are measured, take the lowest, respectively the highest, number as the worst case.

The local minimum must be greater than or equal to the minimum limit. The local maximum must be less than or equal to the maximum limit.

VIL(ac), maximum AC input logic low
Measures the local minimum value from VREF to VREF of the low pulse histogram. If multiple pulses are measured, take the lowest number and the highest number as the worst cases.

The lowest number must be greater than or equal to the minimum limit and the highest number must be less than or equal to the maximum limit.

VIL(dc), minimum DC input logic low
Measures the local minimum and maximum values from the first VIL(ac)max crossing point to the time corresponding to VIL(dc)max crossing a 1V/ns slewrate slope to VREF. If multiple pulses are measured, take the lowest, respectively the highest, number as the worst case. The local minimum must be greater than or equal to the minimum limit. The local maximum must be less than or equal to the maximum limit.

VSEH(ac)
Single-ended high level for strobes. Performed only in 4 probe configurations.

VSEL(ac)
Single-ended low level for strobes. Performed only in 4 probe configurations.

VSWING(MAX), input signal maximum peak to peak swing
Measures the peak-to-peak value of the signal in a given Write frame. If multiple frames are measured, take, the highest number as the worst case. The measure must be less than or equal to the limit.

Time Above AC Level

tDVAC
Measures time above AC level for differential signals.

tVAC
Measures time above AC level for single-ended signals.

AC Over/Undershoot

These tests may be repeated for different signals.

AC Overshoot Peak Amplitude
Measures maximum peak amplitude allowed for overshoot area.

AC Overshoot Area above VDDQ
Measures maximum overshoot area above VDDQ. AC Overshoot Peak Amplitude is prerequisite to compute area.

AC Undershoot Peak Amplitude
Measures maximum peak amplitude allowed for undershoot area.

AC Undershoot Area Below VSSQ
Measures Maximum undershoot area below VSSQ. AC Undershoot Peak Amplitude is prerequisite to compute area.

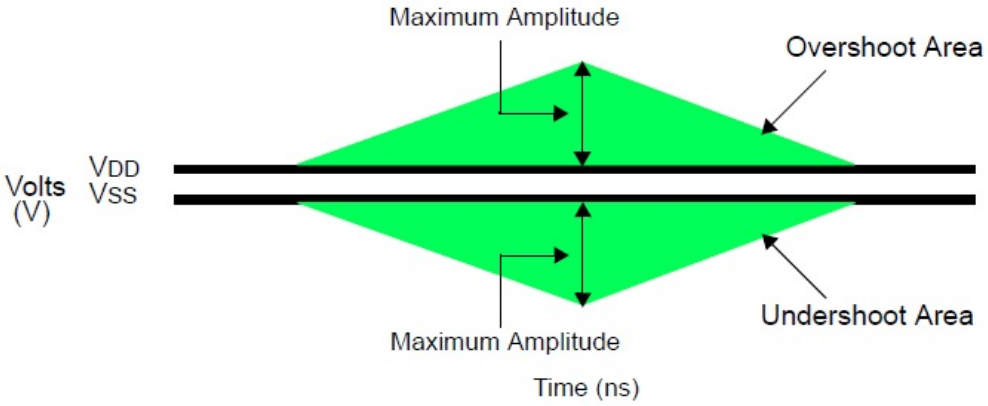


Figure 15. Differential signal levels [JESD209-2D figure 115]

VIX

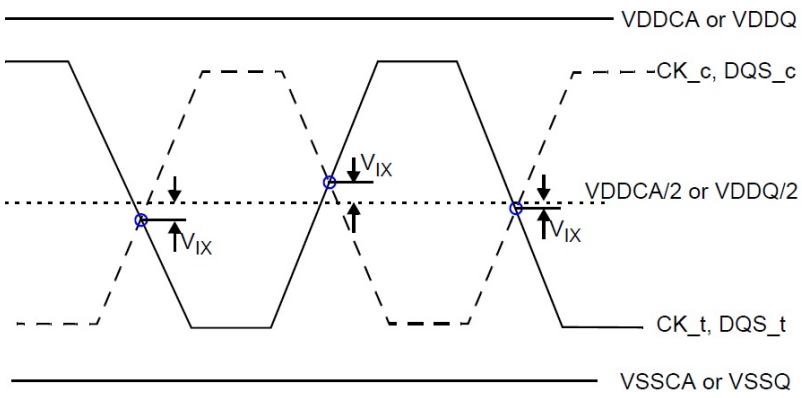


Figure 16. VIX Definition [JESD209-2D figure 111]

Electrical Tests on Read Bursts (Outputs)

Logic Levels

VOH(ac), AC output high measurement level

Measure the local maximum value from VREF to VREF of the high pulse histogram. If multiple pulses are measured, takes the lowest number and the highest number as the worst cases.

VOL(ac), AC output low measurement level

Measures the local minimum value from VREF to VREF of the low pulse histogram. If multiple pulses are measured, take the lowest number and the highest number as the worst cases.

VSWING, output signal maximum peak to peak swing

Measure the peak to peak value of the signal in a given Read burst. If multiple bursts are measured, take, the highest number as the worst case.

SRQ, Output Slew Rate (rising and falling edge)

Applies to all output signals (DQn data and DQSn data strobe signals). The output slew rate is measured from VOL(ac) to VOH(ac) for the rising edge and from VOH(ac) to VOL(ac) for the falling edge.

AC Over/Undershoot

Same tests as on Write bursts.

Timing Tests on Read Bursts (Outputs)

Tests on Bits (no interpolation)

tDQSQ, DQS-DQ Skew for DQS and Associated DQ signals
Maximum skew between the DQS line and the associated DQ line within a read burst. Measures timing from DQS at VREF to DQ rising at VIH(ac)min and falling at VIL(ac)max.

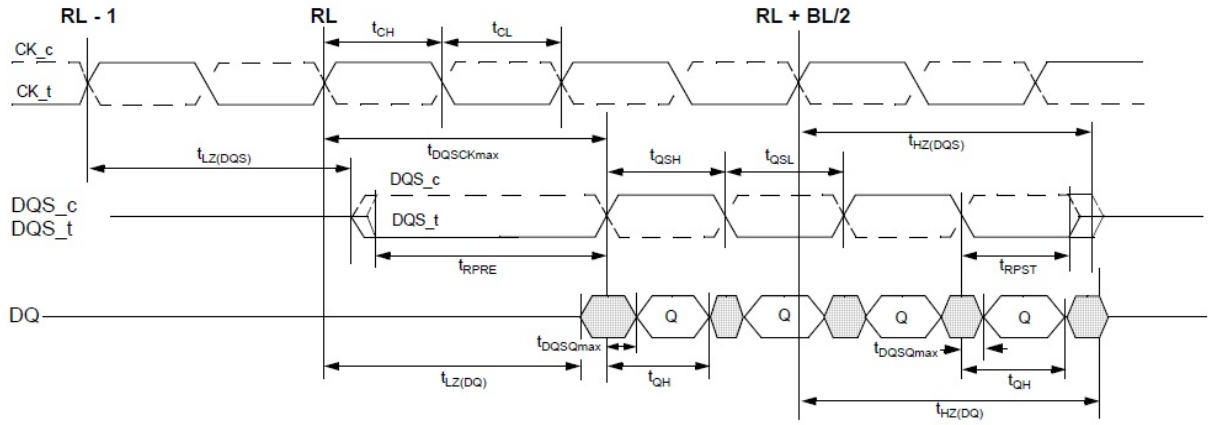


Figure 17. Data output (read) timing [JESD208-2B figure 23]

tQSH, DQS Input High Pulse Width
Measures DQS high pulse width at VREF level.

tQSL, DQS Input Low Pulse Width
Measures DQS low pulse width at VREF level.

tQHP, Data Half Period
Measures DQS output low or high pulse width.

tQH, DQ/DQS Output Hold Time from DQS
Measures the timing from DQS at VREF to DQ at VIH(dc) (rising edge) or VIL(dc) (falling edge).

tQH = tQHP – tQHS

tQHS, DQ Hold Skew Factor
Measures DQ at VIH(dc) or VIL(dc) to DQS at VREF

tDQSCK
Measures time from CK at VREF level to DQS at VREF level. This is a measure similar to tDQSS, but on the Read.

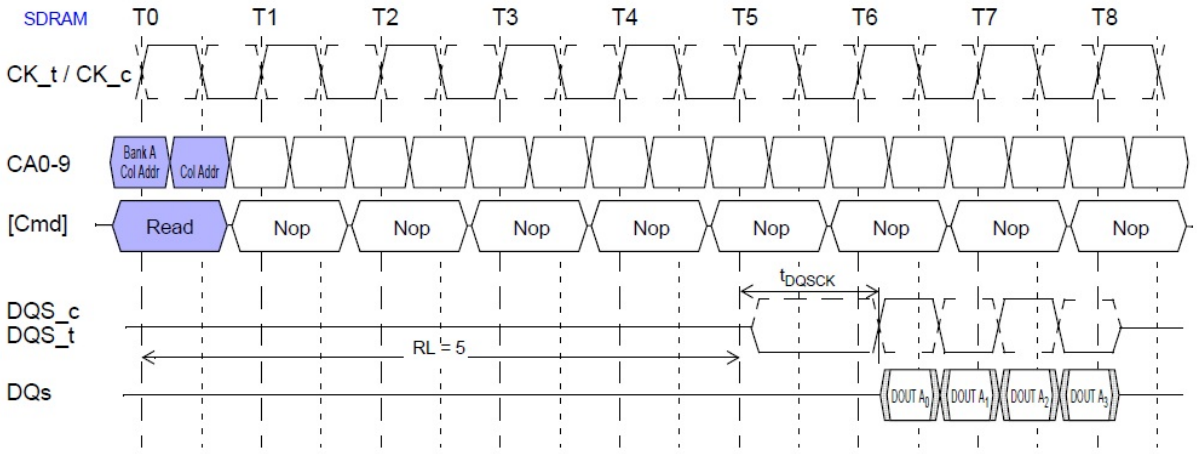


Figure 18. Burst read operation [JESD209-2D figure 25]

PrePostAmble Tests (using interpolation)

tHZ(DQ), DQ high impedance time from CK/CK#
This is the time from Vref of the CK/CK# signal to the point when the DQ is not being driven anymore (at the end of the burst).

tLZ(DQ), DQ low impedance time from CK/CK#
This is the time from when the DQ begins to be driven (at the beginning of the burst) to the nearest CK/CK# edge.

tHZ(DQS), DQS high impedance time from CK/CK#
This is the time from Vref of the CK/CK# signal to the point when the DQ is not being driven anymore (at the end of the burst).

tLZ(DQS), DQS low impedance time from CK/CK#
This is the time from when the DQS begins to be driven (at the beginning of the preamble) to the nearest CK/CK# edge.

tRPRE, Read Preamble
Time from when DQS begins to be driven (at the beginning of the preamble) to when it crosses Vref. This is only measured on a read cycle. tJIT(per) is prerequisite. A derating factor is applied to the limit depending on the clock jitter.

tRPST, Read Postamble
Time from when DQS crosses Vref (at the beginning of the postamble) to when DQS stops being driven (at the end of the postamble). This is only measured on a read cycle. tJIT(duty) is prerequisite. A derating factor is applied to the limit depending on the clock jitter.

Timing Tests on Write Bursts

Tests on Bits (no interpolation)

tDQSS, DQS latching rising transitions to associated CK edge
CK rising edge at VREF level to DQS rising edge at VREF level.

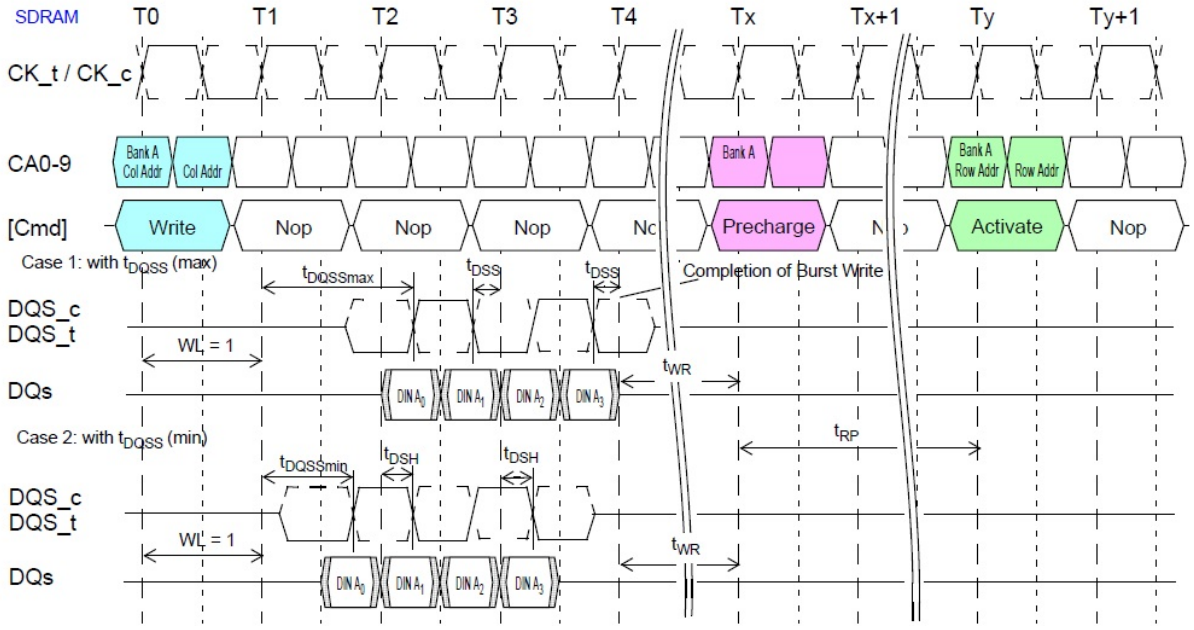


Figure 19. Burst write operation: WL=1 BL=4 [JESD209-2D figure 41]

tDQSH, DQS Input High Pulse Width
DQS input high pulse width at VREF level.

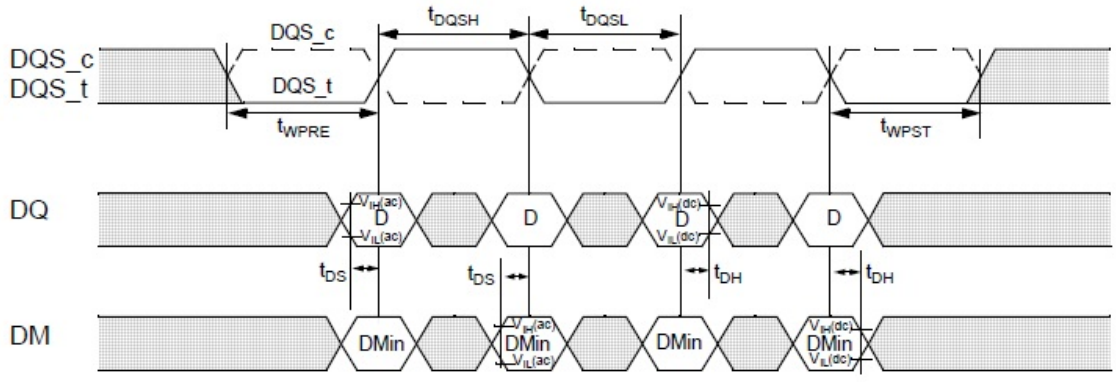


Figure 20. Data input (write) timing [JESD209-2D figure 40]

tDQSL, DQS Input Low Pulse Width
DQS input low pulse width at VREF level. See figure above.

tDSS, DQS Falling Edge to CK Setup Time
Time from DQS falling edge at VREF level to CK rising edge at VREF level. See figure above.

tDSH, DQS Falling Edge Hold Time from CK
DQS Falling Edge Hold Time from CK, time from CK rising edge at VREF level to DQS falling edge at VREF level.

tDS(derated and Vref based), DQ and DM Input Setup Time
Input waveform timing tDS with differential data strobe enabled, is referenced from the input signal crossing at the VIH(ac)min level to the differential data strobe crosspoint at VREF for a rising signal, and from the input signal crossing at the VIL(ac)max level to the differential data strobe crosspoint at VREF for a falling signal applied to the device under test.

DQS and DQS# signals must be monotonic between VIL(dc)max and VIH(dc)min.

Setup (tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIH(ac)min. Setup (tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIL(ac)max.

JESD209-2D Specific Note 8 (page 85 to 94) with tables 43 and 44 explain the limit compensation versus the slewrate of the measured signals. Timing limits are initially specified for input slewrate of 1V/ns for single-ended signals and 2V/ns for differential signal (for DQS and CK).

tDH(derated), DQ and DM Input Hold Time
Input waveform timing tDH with differential data strobe enabled, is referenced from the differential data strobe crosspoint at VREF to the input signal crossing at the VIH(dc)min level for a falling signal and from the differential data strobe crosspoint at VREF to the input signal crossing at the VIL(dc)max level for a rising signal applied to the device under test.

DQS and DQS# signals must be monotonic between VIL(dc)max and VIH(dc)min.

Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(dc)max and the first crossing of VREF(dc). Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(dc)min and the first crossing of VREF(dc).

JESD79-2E Specific Note 8 (page 85 to 94) with tables 43 and 44 explain the limit compensation versus the slewrate of the measured signals. Timing limits are initially specified for input slewrate of 1V/ns for single-ended signals and 2V/ns for differential signal (for DQS and CK).

tDH(vref based), DQ and DM Input Hold Time

Input waveform timing tDH with differential data strobe enabled, is referenced from the differential data strobe crosspoint at VREF to the input signal crossing at the VIH(dc)min level for a falling signal and from the differential data strobe crosspoint at VREF to the input signal crossing at the VIL(dc)max level for a rising signal applied to the device under test. See figure below.

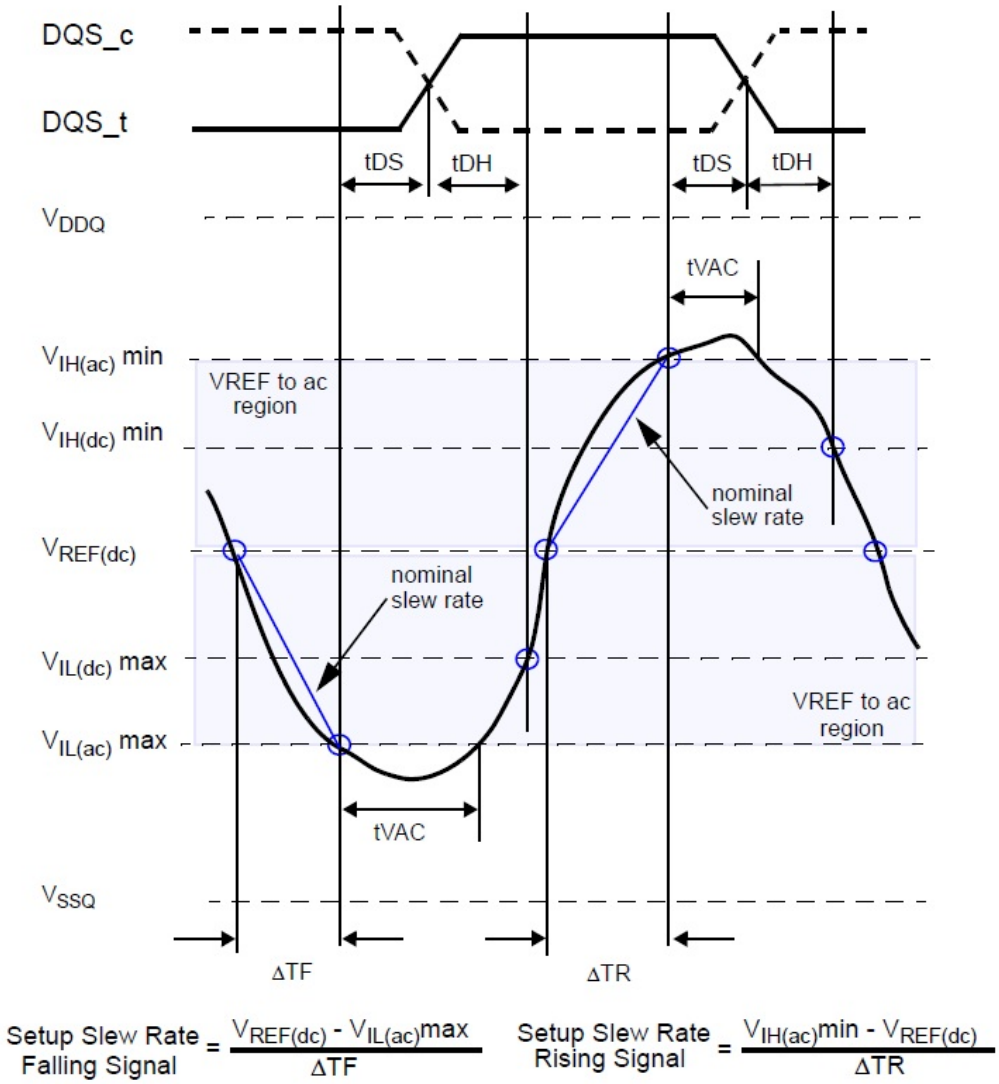


Figure 21. Slew Rate [JESD209-2D figure 124]

DQS and DQS# signals must be monotonic between VIL(dc)max and VIH(dc)min.

Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(dc)max and the first crossing of VREF(dc). Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(dc)min and the first crossing of VREF(dc).

Tests on Pre/PostAmble (using interpolation)

tWPRE, Write Preamble

Time from when DQS begins to be driven (at the beginning of the preamble) to when it crosses Vref, measured on a write cycle. tJIT(per) is prerequisite. A derating factor is applied to the limit depending on the clock jitter.

tWPST, Write Postamble

Time from when DQS crosses Vref (at the beginning of the postamble) to when DQS stops being driven (at the end of the postamble), measured on a write cycle. tJIT(duty) is prerequisite. A derating factor is applied to the limit depending on the clock jitter.

tIS(base+derated), Address and Control Input Setup Time

Input waveform timing is referenced from the input signal crossing at the VIH(ac)min level to the differential clock crosspoint at VREF for a rising signal, and from the input signal crossing at the VIL(ac)max level to the differential clock crosspoint at VREF for a falling signal applied to the device under test. See table below.

unit [ps]	LPDDR2						reference
	1066	933	800	667	533	466	
tIS(base)	0	30	70	150	240	300	$V_{IH/L(ac)}$ = VREF(dc) +/-220mV
tIH(base)	90	120	160	240	330	390	$V_{IH/L(dc)}$ = VREF(dc) +/-130mV

unit [ps]	LPDDR2				reference
	400	333	266	200	
tIS(base)	300	440	600	850	$V_{IH/L(ac)}$ = VREF(dc) +/-300mV
tIH(base)	400	540	700	950	$V_{IH/L(dc)}$ = VREF(dc) +/-200mV

NOTE 1 ac/dc referenced for 1V/ns CA and CS_n slew rate and 2V/ns differential CK_t-CK_c slew rate.

Figure 22. Reference table for tIS tIH [JESD209-2D table 104]

Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIH(ac)min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIL(ac)max.

Jedec JESD209-2D Specific page 203 with tables 105 and 106 explain the limit compensation versus the slewrate of the measured signals.

tIH(base+derated), Address and Control Input Hold Time

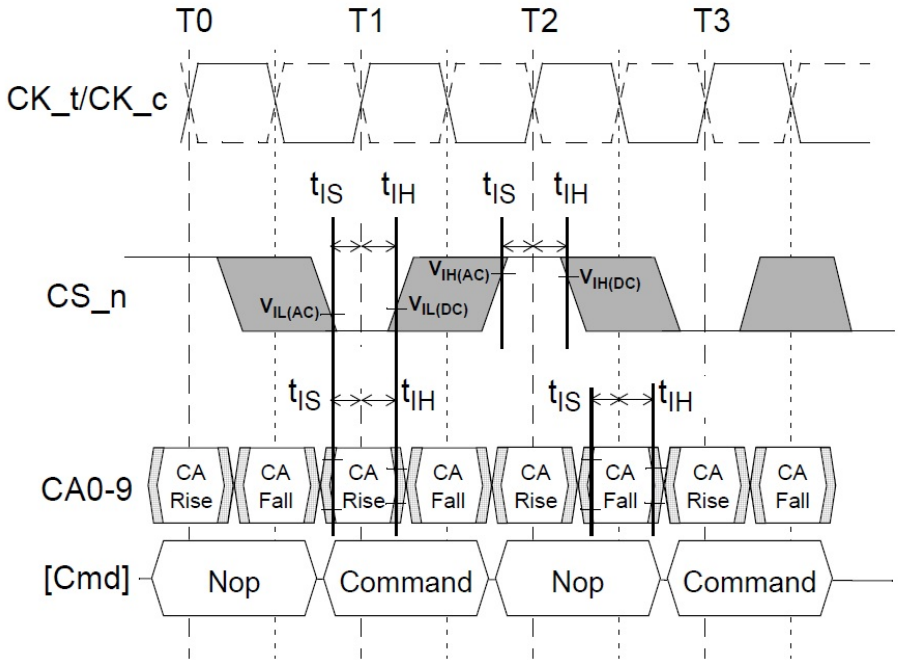


Figure 23. Command Input Setup and hold timing [JESD209-2D figure 22]

QPHY-LPDDR2 Variables

Main Settings

The following variables are used by all configurations. They can be used in conjunction with the test selection and limit set selection to create custom configurations.

Custom Speed Grade in MT/s

Custom Speed Grade of the DUT (Data Rate). Used to set the oscilloscope timebase and sampling rate. See Clock Period Per Screen Division for more explanation. Automatically updated from limit set when default value is set (0 MT/s). Value can be also any custom Speed Grade.

DQ Signal Name

Name of data (DQ) SUT. Choose between available DDR signal names. Default is DQ.

DQS Signal Name

Name of strobe (DQS) SUT. Choose between available DDR signal names. Default is DQS.

ADD/CTRL Signal Name

Select name of Address/Control line from available DDR signal names. Default is A_C.

Additional Signal Name

Name of additional DDR signal. Default is VREF.

Clock Signal Name

Select name of clock (CK) SUT. Choose between available DDR signal names. Default is CK.

DUT Power Supply VDDQ

Value of VDDQ used to compute test limits as specified by Jedec standard. Default is 1.2 V.

Script Settings

Enable Prompt Before Signal Acquisition

Enables/disables prompt to begin signal acquisition, allowing user to generate read/write bursts at the start of the acquisition or to modify the trigger conditions before signal acquisition. Set to “True” to enable. Default is False.

Save Acquired Waveforms

Saved waveforms can be used later in demonstration or optimized version of script. Choose between Yes or No. The default is No. This setting is ignored (no save) if using stored waveforms is enabled and in Demo mode.

Silent Mode Control

No more interaction with the user when silent mode is on. Choose between Yes or No. Default is No. This is useful to let the test run without interruption in the background.

Stop on Test to Review Results
When set to Yes, the script stops after each test allowing you to view the results. The setup is saved so the oscilloscope settings can be modified by the user. On resume, the setup is recalled. Any new acquisition done may cause the script to produce unexpected results.

Waveform Path
Full path to the oscilloscope folder in which to save/recall waveforms. When not in Demo Mode and when Save acquired waveforms is enabled, the waveforms are saved in this folder. When set to Demo Mode, waveforms are also available from this folder. The default location is D:\Waveforms\LPDDR2.

Demo Settings

Use Stored Waveforms
When enabled, previously stored LPDDR2 waveforms are used. Default is No for compliance test configurations, Yes for Demo configurations.

Recalled Waveform File Index (5 digits)
Five-digit number corresponding to the index of the file you want to recall. Default is 00000.

Define Format Used to Set Trace Names
Naming method for saving waveforms. LeCroy composes waveform names automatically from signal names (e.g., C1-00000.trc). A dialog prompts the user for custom waveform names. The default setting is LeCroy.

Use Stored Trace for Speed Grade
This is an optimization used specifically to measure the clock frequency only once. Choose from Yes or No values, The default selection is No.

Advanced Settings

Clock Period per Screen Division
Oscilloscope timebase and sampling rate is set to acquire the given number of clock cycle per display horizontal division at a given Custom (DUT) Speed Grad in MT/s and for a Max. Number of Samples Per Clock Period. The default is 3341 clock periods (a 10us/div timebase at 667 MT/s and 3.3MS max for 100 samples per period).

Timebase = [Clock Period Per Screen Division] / ([DUT Speed Grade in MT/s] / 2 * 1e6)

Maximum Samples = [Max. Number Of Samples Per Clock Period] * [Clock Period Per Screen Division] * 10

Number of Cycles for Clock Test
Jedec standard requires 200 cycles for the Clock compliance test. Any positive number can be entered. Default is 200.

DQS Vref Level for Write Tests
Custom value for the DQS Vref level of tests on Write bursts.

Check for Valid Pre and Postambles

If set to Yes, all the bursts with invalid preamble and/or postambles (not standard pre/postamble shape as defined by the spec) are ignored (not included in tests). If set to No, the user is warned when the preamble and/or postamble are detected as having a non-standard shape. Default is No.

Max. Number Of Samples Per Clock Period

The oscilloscope timebase and sampling rate is set to acquire the given number of points per clock period. The oscilloscope is always set to at least acquire at 20GS/s. Additionally, if an oscilloscope with greater than 6GHz bandwidth is used, the bandwidth is limited to 6GHz. See the Clock Period Per Screen Division variable for more details. Choose from 10;20;50;100;200;500 or 1000. The default value is 100.

Read/Write Burst Separation Upper/Lower Limits

Upper and Lower limits of the DQS/DQ skew range used to determine a read or write burst. This value is in fraction of a bit period. The read/write burst location is determined based on the measured skew between DQS and DQ. If the DQS and DQ edges are aligned, the burst is determined to be a read. If DQS to DQ skew is around a half bit period, the burst is determined to be a write.

Probe Setup <type> Variables

The following variables are specific to the different probe setups that may appear in different configurations.

<Signal> Signal Name

Name of DDR signal to be tested.

Probe Tip Selection

Specifies probe tip used (e.g., SI, PT, SMA/SMP, SP or HighTemp). Applies to all probes in the setup.

<Signal> Channel Gain

Allows the user to manually specify the vertical scale in V/div. Signal can be Clock, DQ, DQS, DQSn, ADD/CTRL, or DM. Default is 0 for auto-scale.

<Signal> Channel Index

Oscilloscope input channel used for the respective signal. For example, when the Clock is input to C1, Clock Channel Index is 1.

<Signal> Channel Invert

Inverts the respective signal. For example, to invert the Clock signal, set Clock Channel Invert to True. Default is False.

<Signal> Channel Offset

Specifies the offset in Volts to apply to the respective signal. Default value of 0 applies auto-scale. Only used if Gain is > 0.

<Signal> VP@Rcvr
Set an oscilloscope Math function associated with the respective signal to be VP@Rcvr. VirtualProbe@Receiver uses a simple model that allows the user to measure the voltage in the middle of the transmission line, and view the voltage as seen at the receiver (the virtual probe point).

Select Signal Under Test If Many
Signal to be tested in 4-probe setups.

QPHY-LPDDR2 Limit Sets

LPDDR2-200
This corresponds to the JEDEC JESD209-2E LPDDR2 standard specification limits for 200 MT/s.

LPDDR2-266
This corresponds to the JEDEC JESD209-2E LPDDR2 standard specification limits for 266 MT/s.

LPDDR2-333
This corresponds to the JEDEC JESD209-2E LPDDR2 standard specification limits for 333 MT/s.

LPDDR2-400
This corresponds to the JEDEC JESD209-2E LPDDR2 standard specification limits for 400 MT/s.

LPDDR2-466
This corresponds to the JEDEC JESD209-2E LPDDR2 standard specification limits for 466 MT/s.

LPDDR2-667
This corresponds to the JEDEC JESD209-2E LPDDR2 standard specification limits for 667 MT/s.

LPDDR2-800
This corresponds to the JEDEC JESD209-2E LPDDR2 standard specification limits for 800 MT/s.

LPDDR2-933
This corresponds to the JEDEC JESD209-2E LPDDR2 standard specification limits for 933 MT/s.

LPDDR2-1066
This corresponds to the JEDEC JESD209-2E LPDDR2 standard specification limits for 1066 MT/s.

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