TELEDYNE LECROY
Everywhereyoulook™

QPHY-DDR5-SYS

DDR5 System Level Compliance Software

Instruction Manual

January 2025

Relating to:

MAUI® version 11.0.x.x and later

QualiPHY® version 11.0.x.x and later

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qphy-ddr5-sys-im.pdf
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About This Manual

This manual assumes that you are familiar with using an oscilloscope, in particular the Teledyne LeCroy oscilloscope that will be used with QualiPHY and that you have purchased the QPHY-DDR5-SYS software option or the DDR5 bundle that includes it.

Some of the images in this manual may show QualiPHY products other than QPHY-DDR5-SYS, or were captured using different model oscilloscopes, as they are meant to illustrate general concepts only. Rest assured that while the user interface may look different from yours, the functionality is identical.

Introduction

QualiPHY is highly automated compliance test software meant to help you develop and validate the PHY (physical-electrical) layer of a device, in accordance with the official documents published by the applicable standards organizations and special interest groups (SIGs). You can additionally set custom variables and limits to test compliance to internal standards.

QualiPHY is composed of a "wizard" application that enables the configuration and control of separate tests for each standard through a common user interface. Features include:

- **User-Defined Test Limits** to ensure devices are well within the passing region, even if subsequently measured with different equipment.
- **Flexible Test Results Reporting** that includes XML Test Record generation to better understand device performance distribution or obtain process related information from the devices under test.

QPHY-DDR5-SYS is an automated test package performing all the real-time oscilloscope system-level tests for DDR5 designs in accordance with JEDEC Standard No. JESD79-5B. These standards are available from jedec.org.

Conventions

This manual follows these documentation conventions:

- The terms "application" and "software" without any other identifier refer to the QPHY-DDR5-SYS software option.
- The term "DUT" is an abbreviation for Device Under Test.
- The term "select" is a generic term referring to any method for activating a software control, either using a pointing device or a touch screen.
- The term "Note:" identifies important information.

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Software Installation and Setup

QualiPHY is a Windows-based application that can be configured with one or more serial data compliance components. Each compliance component is purchased as a software option.

Oscilloscope Requirements

Hardware

The QualiPHY software requires at least 13 GHz of bandwidth on a WaveMaster/SDA 8 Zi-B, WaveMaster/ SDA 8000HD or LabMaster 10 Zi-A oscilloscope for testing DDR5.

While not required, we recommend for convenience running QualiPHY on an oscilloscope equipped with an additional monitor. This allows the waveforms and measurements to be shown on the oscilloscope display, while the QualiPHY application is displayed on the attached monitor.

See the oscilloscope *Operator's Manual* for instructions on setting up dual monitor display.

Software

For the software as shown here, the oscilloscope must be installed with:

- MAUI version 10.9.x.x minimum*
- QualiPHY version 10.9.x.x minimum* with an activated QPHY-DDR5-SYS component

  Note: The versions listed above are the minimum versions required for the product as shown here. MAUI and QualiPHY software versions must match to the second point, so upgrade your version of QualilPHY if you have upgraded your oscilloscope firmware. The QualiPHY software may be installed on a remote PC, but all other software must be run on the oscilloscope.
- Optional, but highly recommended: DDR5 Debug Toolkit (for turn-on, pre-compliance, optimizing and debugging compliance failures).
- Optional, but highly recommended: VirtualProbe software (for fixing reflections, termination, probe points, de-embedding, etc.)

  Note: VirtualProbe is included with SDAIII-CompleteLinq and SDA Expert Complete.

Other Required Equipment

See the DDR5 System Testing section for other required test hardware.

Update Oscilloscope Firmware

We recommend updating your Windows OS with the latest security patches before installing our software.

Download the latest version of the MAUI firmware from:

teledynelecroy.com/support/softwaredownload/ under Oscilloscope Downloads > Software Utilities

Follow the instructions included with the download to install it.

Install QualiPHY Application

Download the latest version of the QualiPHY software from:

teledynelecroy.com/support/softwaredownload/ under Oscilloscope Downloads > Software Utilities

The application can be installed on either the test oscilloscope or on a remote host computer. For remote execution, see Set Up Remote Control.

If the oscilloscope is not connected to the Internet, copy the installer onto a USB memory stick then transfer it to the oscilloscope desktop or a folder on the D:\ drive to execute it.

Run **QualiPHYInstaller.exe** and follow the installer prompts. Choose all the components you plan to activate. If you omit any components now, you will need to update the installation to activate them later.

By default, the oscilloscope appears as local host when QualiPHY is executed on the oscilloscope. Follow the steps under Add Oscilloscope Connection to QualiPHY to check that the IP address is 127.0.0.1.

Activate QualiPHY Components in MAUI

The serial data compliance components are factory installed as part of the oscilloscope application (MAUI) and are individually activated through the use of an alphanumeric code uniquely matched to the oscilloscope's serial number. This option key code is what is delivered when purchasing a software option.

To activate a component on the oscilloscope:

1. From the menu bar, choose Utilities > Utilities Setup.
2. On the Options tab, click Add Key.
3. Use the Virtual Keyboard to Enter Option Key, then click OK.

   If activation is successful, the key code now appears in the list of Installed Option Keys.
4. Restart the application by choosing File > Exit, then double-clicking the Start DSO icon on the desktop.

Activate Other Teledyne LeCroy Software

If newly purchased, activate any other required Teledyne LeCroy software options, such as SDA Expert NRZ. The software is included with the latest firmware, you need only install your option key using the procedure above to activate it.

Set Up Remote Control (optional)

Usually, the oscilloscope is the host computer for the QualiPHY software, and all models that meet the acquisition requirements will also meet the host system requirements. However, the QualiPHY software can be executed from a remote host computer.

To run QualiPHY remotely:

- The oscilloscope must be connected to a LAN and assigned an IP address (fixed or dynamic).
- The host computer must be on the same LAN as the oscilloscope.

Remote Host Computer Requirements

If you wish to run the QualiPHY software from a remote computer, these minimum requirements apply:

- Windows 10 Professional operating system (Windows 11 is not currently supported)
- 1 GHz or faster processor
- 1 GB (32-bit) or 2 GB (64-bit) of RAM
- Ethernet (LAN) network capability
- Hard Drive:
  - At least 100 MB free to install the wizard application
  - Up to 2 GB per standard installed to store the log database (each database grows from a few MB to a maximum of 2 GB)

Configure Oscilloscope for Remote Control

1. From the oscilloscope menu bar, choose Utilities → Utilities Setup...
2. Open the Remote tab and set Remote Control to TCP/IP.
3. Verify that the oscilloscope shows an IP address.

Add Oscilloscope Connection to QualiPHY

1. On the host PC, download and run QualiPHYInstaller.exe.
2. Start QualiPHY and click the General Setup button.
3. On the Connection tab, click Scope Selector.
4. Click Add and choose the connection type. Enter the oscilloscope IP address from Step 3 above. Click OK.
5. When the oscilloscope is properly detected, it appears on the Scope Selector dialog. Select the connection and click OK. QualiPHY is now ready to control the oscilloscope.

Select Oscilloscope Connection

Multiple oscilloscopes may be accessible to a single remote host. In that case, go to the QualiPHY General Setup Connection tab and use the Scope Selector at the start of each session to choose the correct connection.

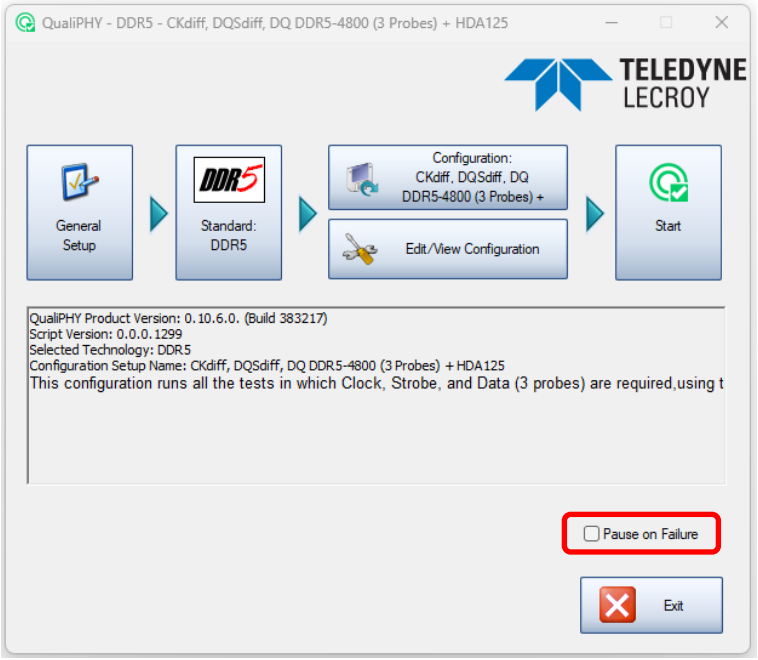
QualiPHY tests the oscilloscope connection when starting a test. The software warns you if there is a connection problem.

Set Up the QualiPHY Application

The following general settings will persist with each test session you run in QualiPHY. We recommend these be made as part of initial installation. To begin, access the QualiPHY wizard by either:

- Choosing **Analysis > QualiPHY** from the oscilloscope menu bar
- Double-clicking the **QualiPHY desktop icon**  on a remote computer or oscilloscope desktop.

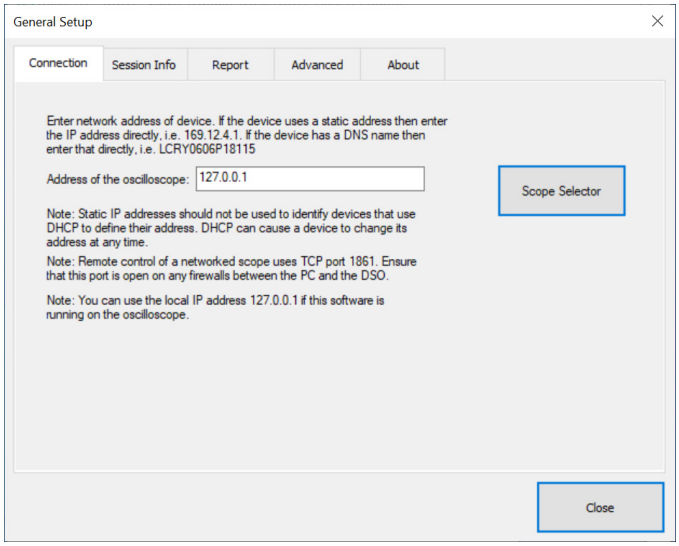
When **Pause on Failure** is checked, QualiPHY will pause execution whenever a test fails and prompt you to make corrections before retrying a measurement. You may open DDR Debug Toolkit to analyze the failure, even if you have not purchased the Debug Toolkit license.



On the Wizard, click the **General Setup** button to continue.

Connection Tab

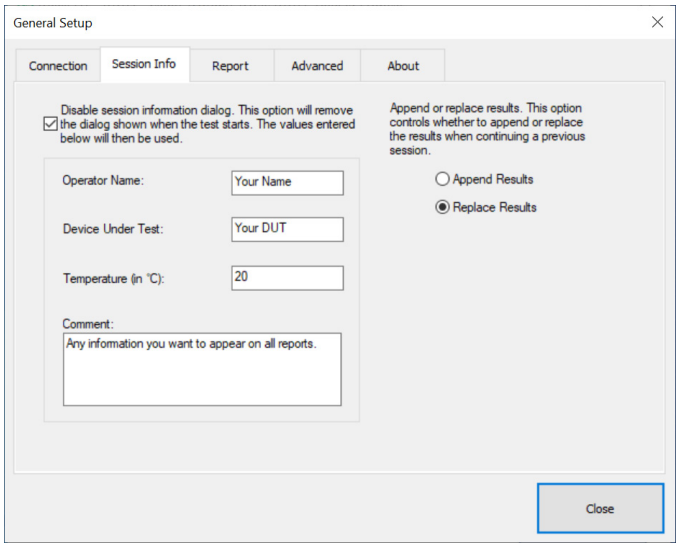
The Connection tab shows the **Address of the oscilloscope** is local host 127.0.0.1 when QualiPHY is run from the oscilloscope. If you are running QualiPHY from a remote computer, this will show the network IP address of the oscilloscope to which QualiPHY is currently connected.



The **Scope Selector** button allows you to choose the oscilloscope used for testing when several are connected to the QualiPHY application on a remote host. See Set Up Remote Control for details.

Session Info tab

The Session Info tab contains information that appears on reports, such as: **Operator Name**, **Device Under Test** (DUT) name, **Temperature (in °C)** of the test location, and any additional **Comments**.

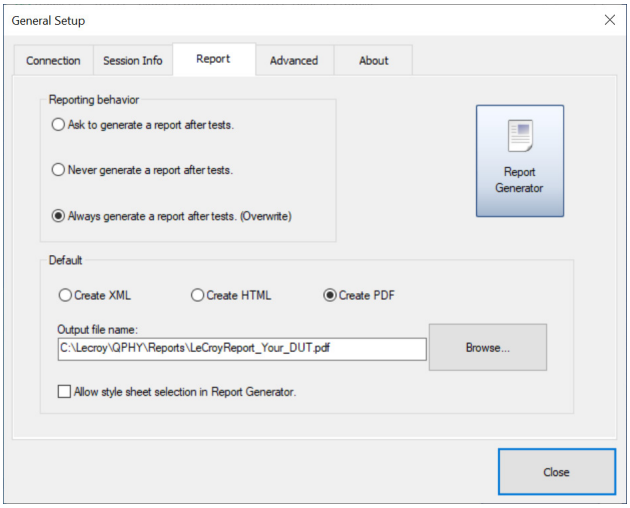


If you check **Disable session information dialog**, these global settings will be used on all reports. Otherwise, you will be presented with a dialog at the start of each session that overrides these settings.

There is also a selection to **Append Results** or **Replace Results** (overwrite) when continuing a previous test session.

Report tab

The Report tab contains settings related to report generation.



Choose a **Reporting behavior** of:

- "Ask to generate a report after tests"—you'll be prompted to create a new file for each set of test results.
- "Never generate a report after tests"—you'll need to manually execute the Report Generator.
- "Always generate a report after tests" will autogenerate a report of the latest test results.

Choose a **Default** report output file format of XML, HTML, or PDF.

Optionally, check **Allow style sheet selection in Report Generator** to enable the use of a custom .xslt when generating XML and HTML reports. The path to the .xslt is entered on the Report Generator dialog.

The **Report Generator** button launches the Report Generator dialog, which contains the same settings as the Report tab, only applied to individual reports. This dialog appears automatically at the conclusion of each test group if you have selected "Ask to generate a report after tests."

DDR5 System Testing

If you are new to QualiPHY, review Using QualiPHY to understand the conventions of the user interface.

Required Hardware

In addition to the oscilloscope, you will need the following to run the DDR5 tests:

- 3 to 4 DHXX-PA Series probes and DH-SI solder tips. This is to measure the DQ (Data), CK (Clock), DQS (Strobe) and possibly the CA (Command Address).
- Interposers make a world of difference in a high-quality setup. They are soldered between the PCB and the DRAM chip to provide easy probing points. Reach out to Nexus (world-wide) or EyeKnowHow (Europe).
- A HDA125 Logic Analyzer is a modular and upgradable MSO that probes the Command Address lanes to trigger and decode. It vastly improves the Read / Write packet separation and is highly recommended.

Preparing Oscilloscope

Before beginning any test or data acquisition, allow the oscilloscope and probes to warm up for at least 30 minutes after powering on.

Oscilloscope calibration is automatically performed by the oscilloscope application; no manual calibration is required. The calibration procedure will be run again if the temperature of the oscilloscope changes by more than a few degrees.

Connecting Probes

Determining Signals to Access

The required signals to probe depend up on which tests are being run in QPHY-DDR5-SYS. The configurations are tailored to different probe setups to allow you to easily see which signals are required for a particular test.

Best Places to Probe

The DDR5 specification is defined by the JEDEC standards to be tested at the balls of the DRAM (BGA). The probes should be placed as close to the DRAM as possible in order to follow the JEDEC defined specification. This is important to minimize signal quality issues, such as reflections that can occur on the signals.

For the best signal fidelity capture, it's recommended that an interposer be soldered in between the DRAM and the PCB. Typically, the DRAM sits on the interposer, which sits on a riser board, which sits on the PCB. By using an interposer, the solder-down probe leads can easily be accessed with little impact to the signal.

Two companies that offer interposers and/or installation in circuit are Nexus Technologies (world wide) and EyeKnowHow (Europe).

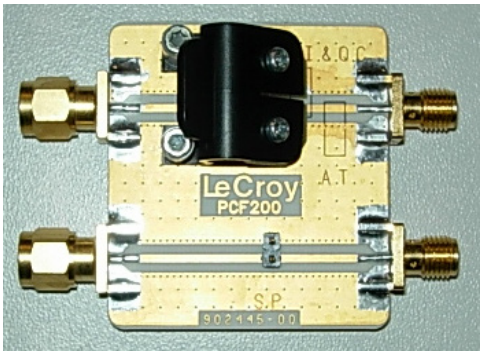
Another commonly used method is to place vias on the PCB to access the Data, Strobe, Clock or command address signals. These typically are too small, so during layout it's recommended to run traces to make them easier to solder to and place them at similar distances from the BGA. The closer you are to the BGA the better, to help ensure fewer reflections due to trace length. If using this method, apply VirtualProbe software to de-embed the trace lengths with simulated S-parameter files.

Deskewing Probes

For DDR measurements, it is crucial properly deskew probes before running tests to ensure proper signal timing. Ideally, the same settings should be used when deskewing as when acquiring signals for analysis. This will ensure that the channels are deskewed using the same setup as when running compliance tests. Deskew values are saved and stored by QualiPHY at the beginning of each run.

For ease of connectivity, we recommend using the SP tip to deskew, but as long as the same tip is used to deskew each probe, it does not matter which style of tip is used.

Required Equipment



- PCF200 deskew fixture. The fixture has two signal paths:
    - The upper path (with the black clip) is for Solder-In (SI), Quick-Link Solder-In (QL-SI), Quick-Connect (QC) and Adjustable Tip (AT) probe tips.
    - The lower path is for Square-Pin (SP) probe tips.
- 50 Ω terminator

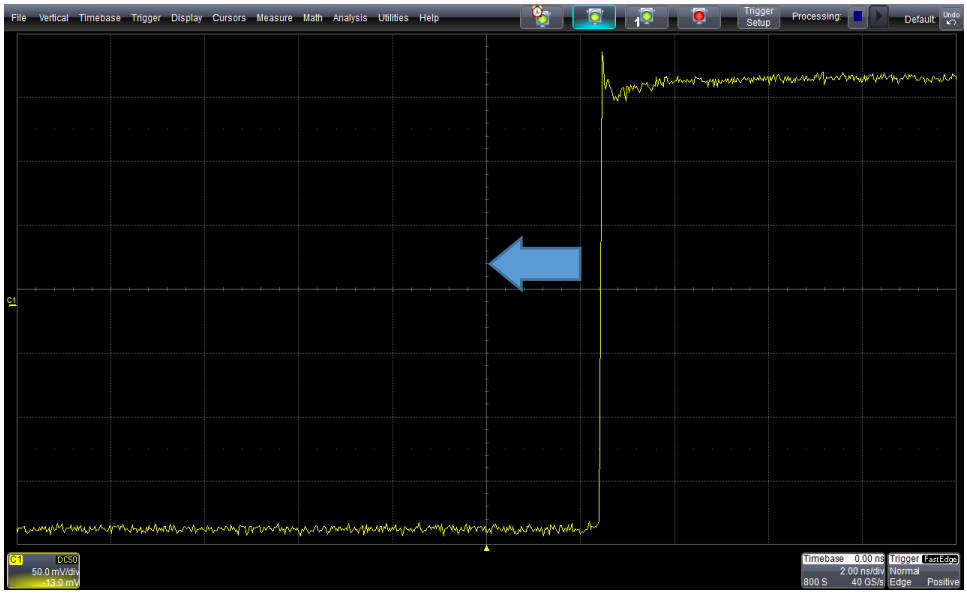
Note: Alternatively, use an LPA-K-A adapter and SMA cable.

Deskew Method

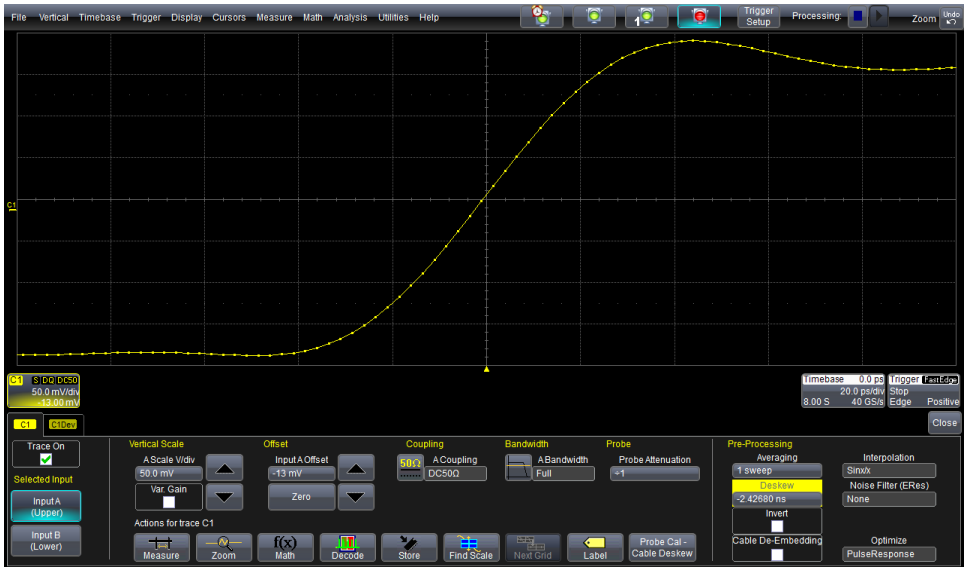
Before beginning the procedure, be sure to warm the oscilloscope for at least 30 minutes.

1. Connect the PCF200 to the oscilloscope's fast edge output.
2. Connect probes electrically in a single-ended arrangement using their designated area on the fixture:
    - Connect the positive side of the probe to the signal trace (in between the two white strips). The positive polarity is indicated on the tip of the probe by a plus sign.
    - Connect the negative side to the ground plane (outside of the white strips).
    - To minimize reflections, apply a 50 Ω terminator to the end of the signal path in use. If a 50 Ω terminator is not available, an SMA cable can be used to terminate the PCF200 to one of the oscilloscope's outputs.
3. Set the oscilloscope Trigger Source to Fast Edge, Trigger Type to Edge.
4. Set a Timebase of approximately 10 ns/div and Timebase Delay of 0.

    Once everything is properly set up, the oscilloscope display should look similar to the figure below. If there is no propagation delay due to the probe, and no internal oscilloscope channel propagation delay, the 50% trigger level will be at the center line of the oscilloscope grid.



5. From the channel setup dialog (C*n*):
    - Enable **Sinx/x** interpolation and set the **Averaging** to **50** sweeps.
    - Touch the **Deskew** field once to highlight it, then adjust the deskew value to move the rising edge of the trace to the center of the display.
6. Now, decrease the **Timebase** to around **20 ps/div** and once again adjust the **Deskew** value so that the 50% rising edge point is centered in time.



Repeat this deskew procedure for each probe using the same probe tip.

Note: Before moving on to the next probe, reset Averaging to 1 sweep and turn off Sinx/x interpolation.

When QualiPHY is started, the deskew values from each channel dialog are saved and stored by QPHY at the beginning of each run. However, at the end of testing these values will be erased. By saving a panel setup (.lss file), it is possible to refer to the deskew values after testing has completed.

Read (R) and Write (W) Burst Requirements

Read/Write Burst Separation

One of the most critical aspects of memory testing is separating the bi-directional Data (DQ) and Strobe (DQS) lines, which each have data moving in two directions ("Write" packets from the PHY controller and "Read" packets from the DRAM). If you're testing DDR5, there are three different methods for burst separation. Some are more reliable based on the allowable variations of the JEDEC standards.

Phase Detection

In DDR5, we can separate Read and Write bursts using an algorithm that best approximates the packet type based on skew relationship between the Data (DQ) and Strobe (DQS) signals.

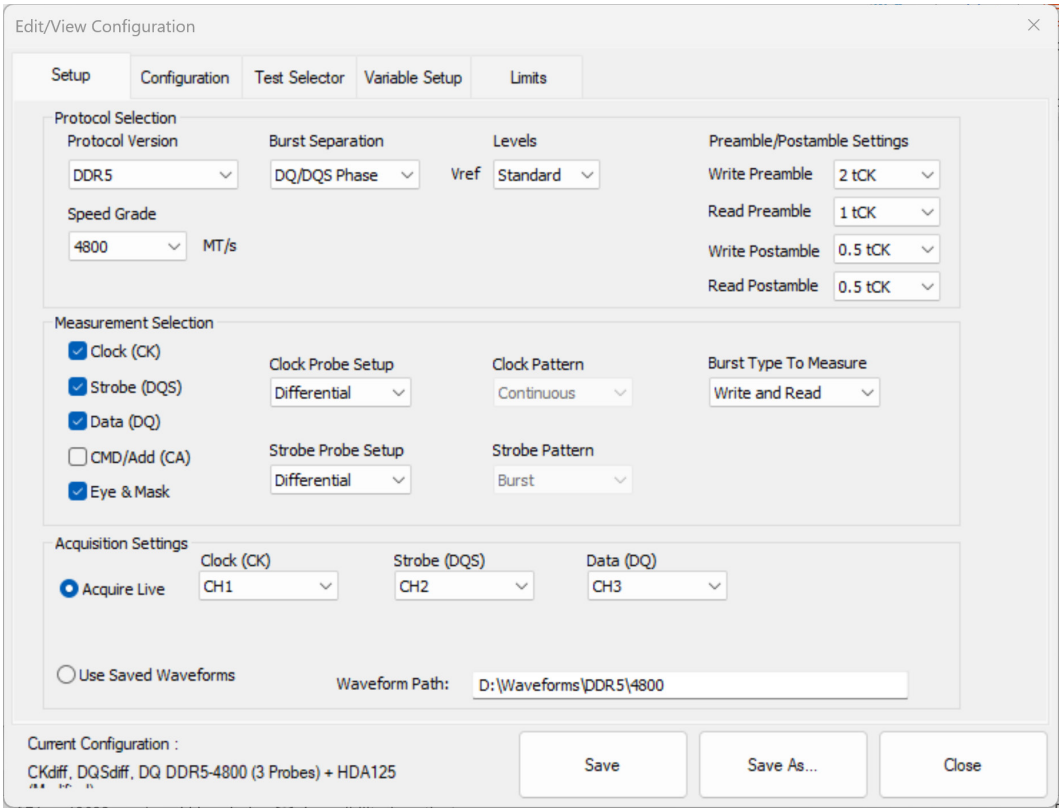


Figure 1. Setup for Phase Detection burst separation method.

Command Address Detection (with HDA125)

For DDR5, the most reliable solution for R/W burst separation is using the external MSO device, HDA125 High-speed Digital Analyzer. By probing the Command Address (CA) lines, the software decodes the JEDEC's Command Truth Table to exactly know when Read and Write information occurs. The QPHY-DDR5-SYS software uses this for packet separation in order to overcome signal quality issues that might cause R/W burst algorithm challenges.

Choose the HDA125 Burst Separation method. Click the HDA125 button to set up your digital inputs. Be sure to update the CAS Latency settings.

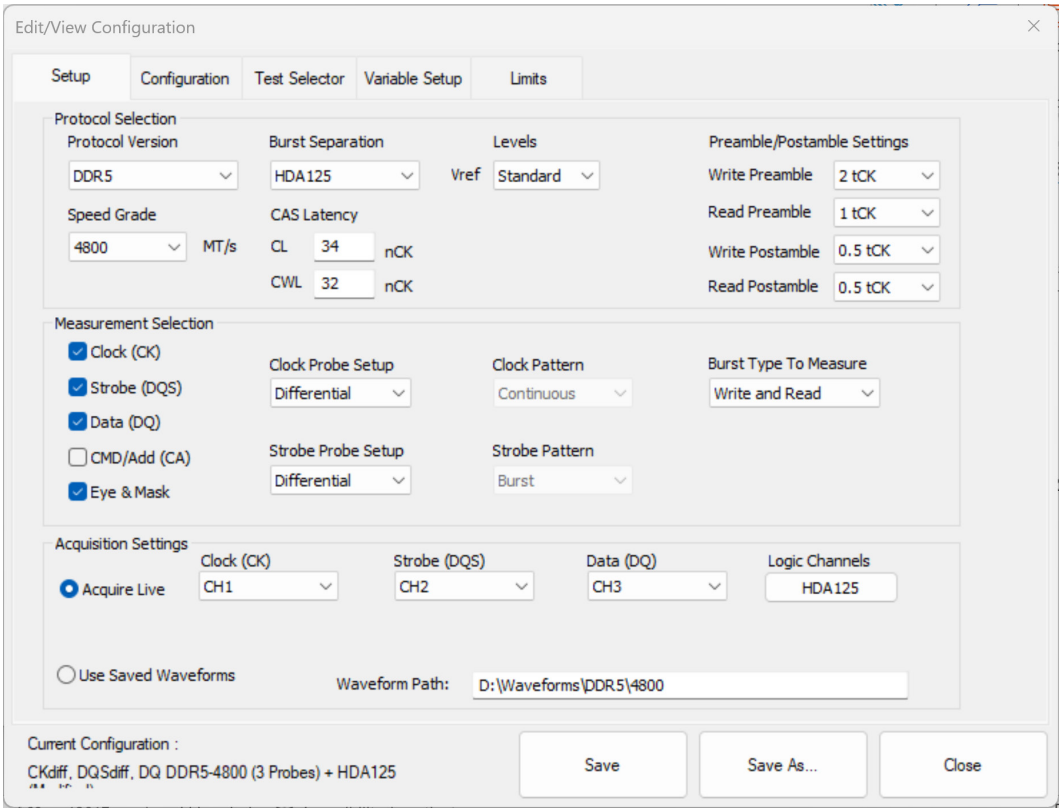


Figure 2. Setup for Command Address Detection burst separation method.

CA4 + Latency

The CA4 method detects the start of the burst, then subtracts the latency periods to look at the state of the CA4 line in both cases. If using the CA4 line for separation, enter the number of clock cycles in the CAS Read Latency (CL) and CAS Write Latency (CWL).

For this method, use a single-ended probe with ≥4 GHz bandwidth to probe the CA4 line. Enter this fourth analog input channel in CMD/Address (CA). The DH Series probes can be used as single-ended probes in this case to input the CA4 line.

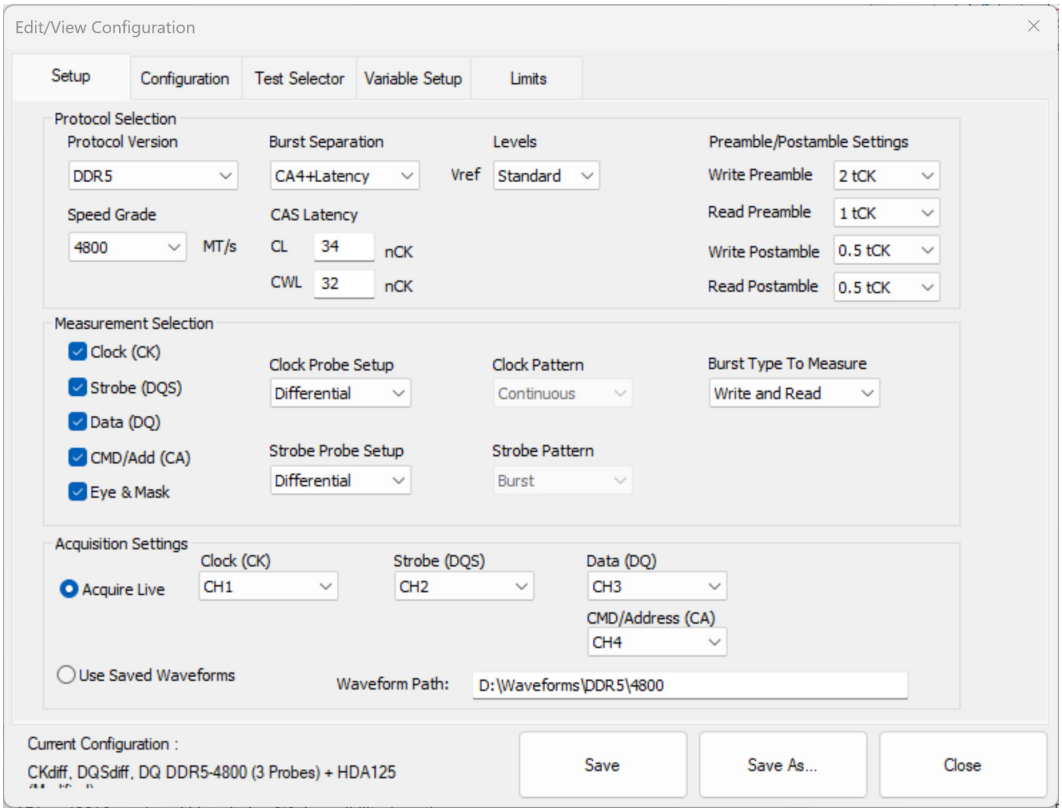


Figure 3. Setup for CA4 + Latency Detection burst separation method.

Read/Write Burst Generation

It is recommended to capture a minimum of 10 Read and 10 Write bursts during each acquisition, but for greater statistical significance, it is encouraged to capture more.

DDR5 Burst Generation

Programs that can communicate with the DRAM and controller are widely available. For PCs, one popular option is *Memtest86+*, which is available for download from memtest.org as well is integrated in some PC BIOS menus.

When using Memtest, it is recommended to randomly generate the amount of data. We've found test mode 7, which will randomly generate both Read and Write bursts, to be successful. Other custom programs like *Windows Memory Diagnostic* can be used to stimulate the transfer of data to DIMM.

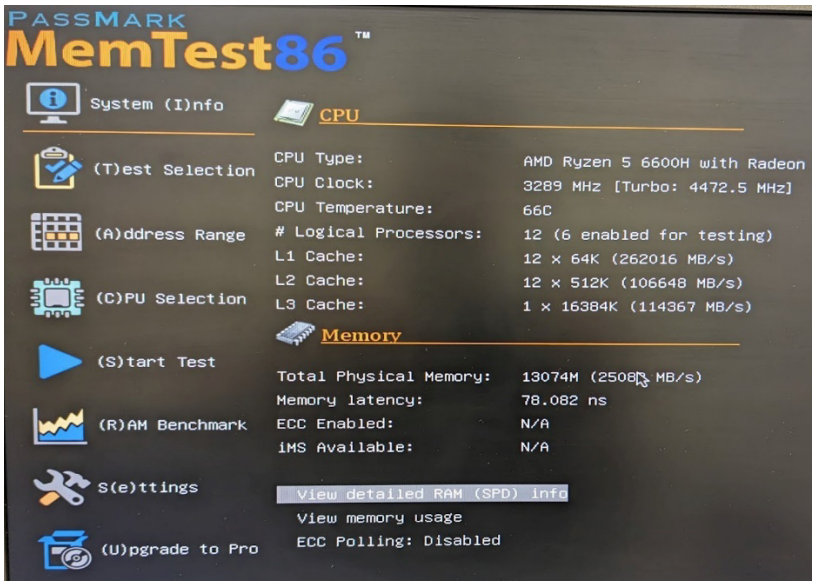


Figure 4. Memtest86+ software.

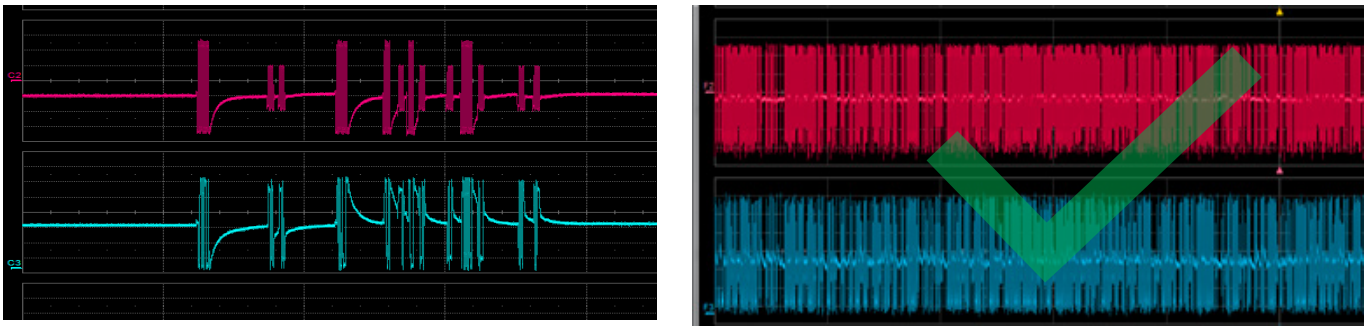


Figure 5. Making sure Memtest is generating enough data traffic.

Initial Signal Checking

Before running QualiPHY to test DDR5, check the signals to verify that they make sense. This section covers some of the basic things that should be verified by the operator before running QPHY-DDR5-SYS.

Expected Channels

By default, QPHY-DDR5-SYS expects to see the Clock (CK) on CH1, Strobe (DQS) on CH2 and Data (DQ) on CH3. This is what is shown in the connection diagrams. The Input Channel variables can always be used to modify any of these channel assignments.

Signal Amplitude Clipping

For best results, it is recommended that the signals take up 80% to 95% of the vertical graticule for the best measurement accuracy. Avoid allowing the signal to go outside the oscilloscope vertical screen, as this clips and removes the usable data.

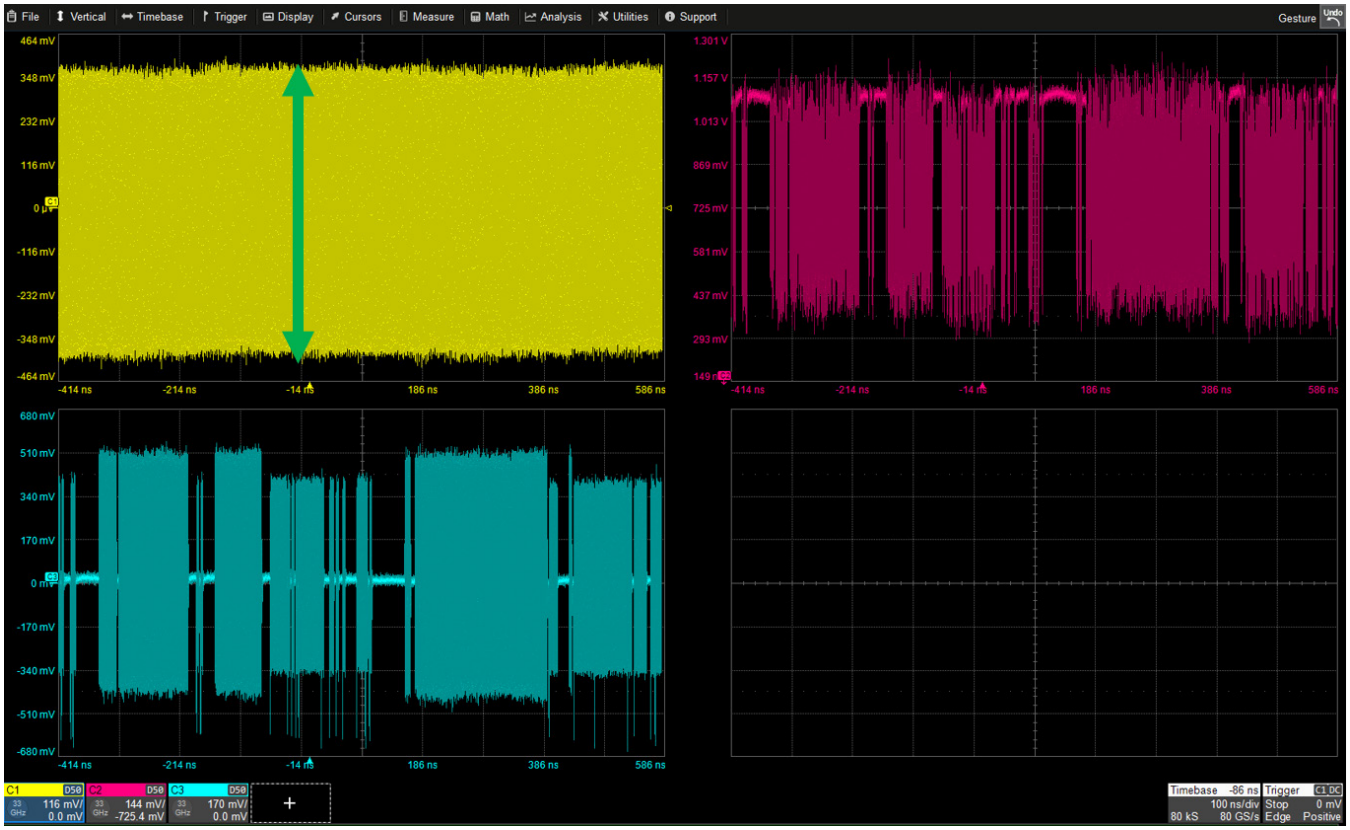


Figure 6. Checking that the signals take up enough vertical space, but don't' clip.

Clock Frequency

By applying the Frequency measurement parameter to the CK signal, you can verify that the DDR5 system is running at the expected speed (Data Rate = Clock Frequency * 2).

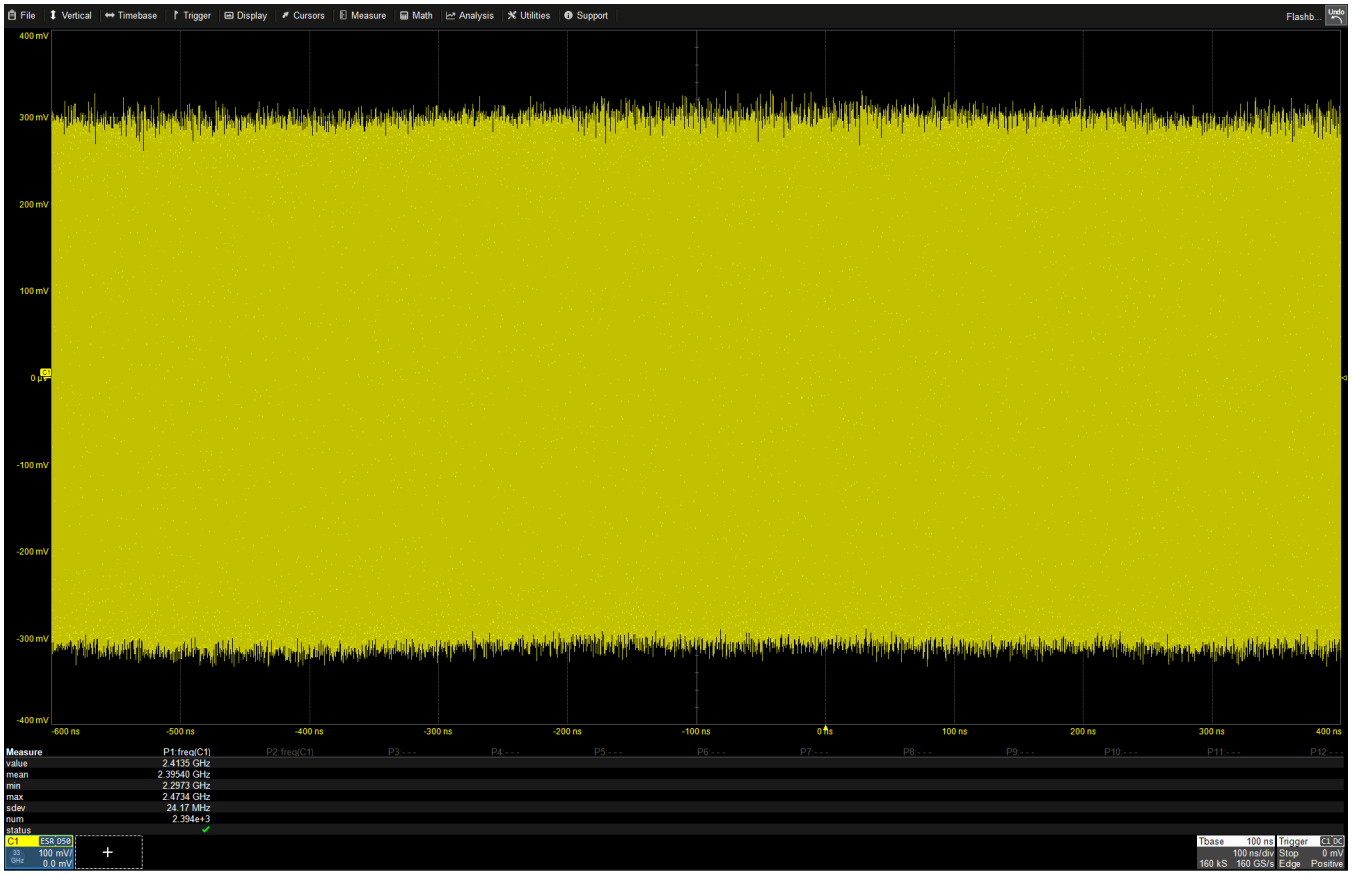


Figure 7. Measuring the Clock Frequency.

Presence of Read/Write Burst

In DDR5, checks can evaluate the quality of the burst packets. One way to validate both packets are present is to use the Decode capability of the DDR5 Debug Toolkit, as seen in Figure 4. Additionally, the signal amplitude can be used to determine the presence of Read and Write bursts as seen in Figure 5. If probing at the memory BGA, you can typically expect Read bursts will have a larger amplitude than Write bursts.

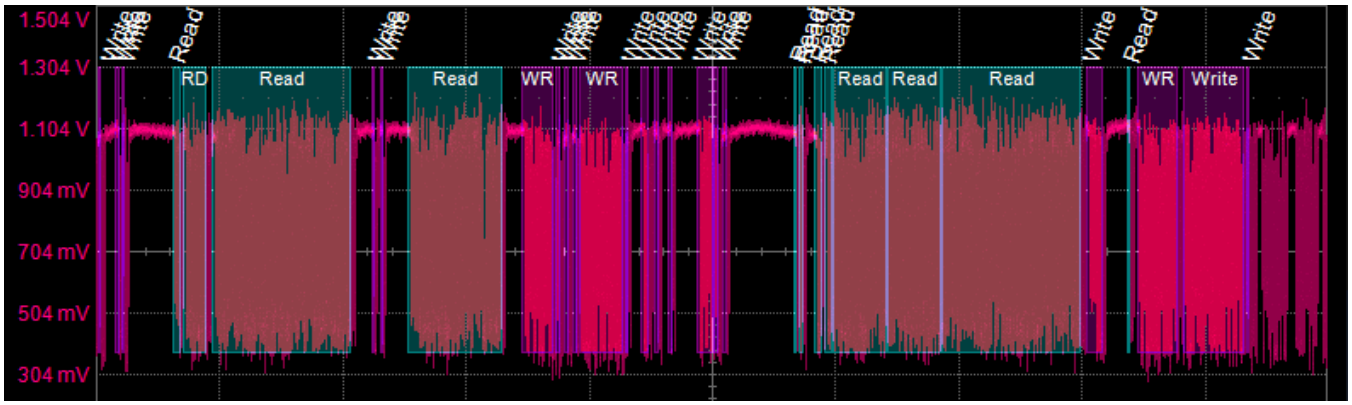


Figure 8. DDR5 Packet Decoding to Identify Read and Write Packets

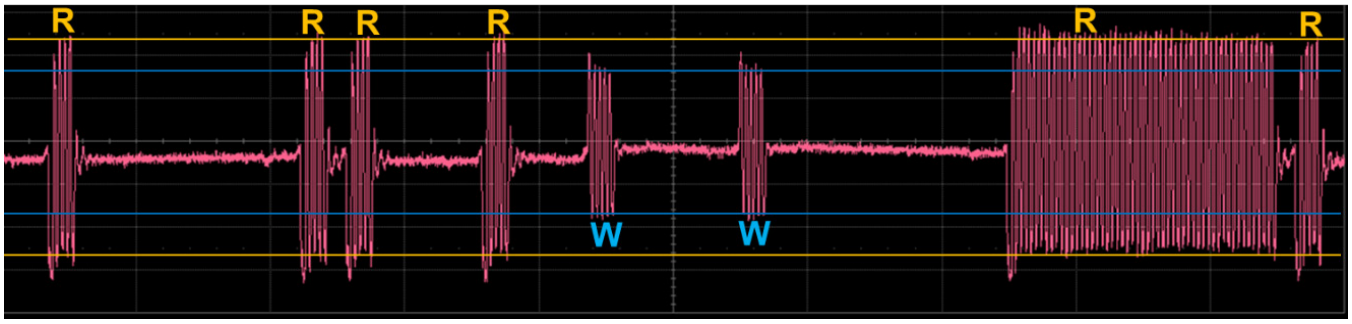
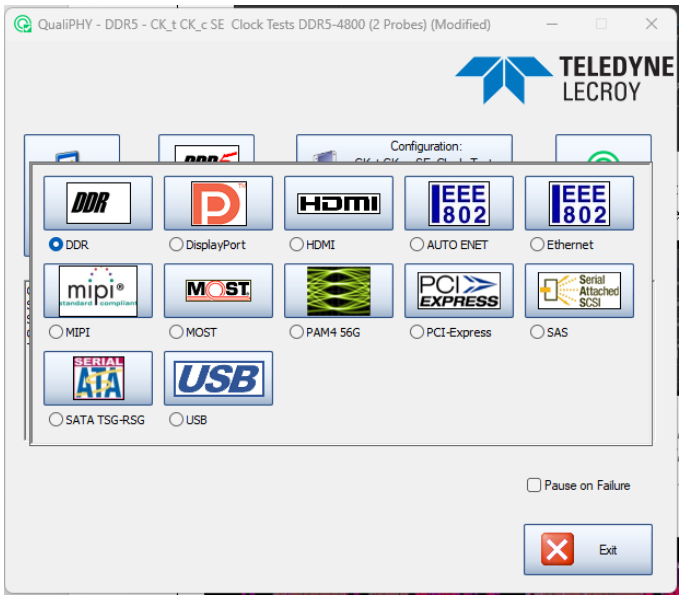


Figure 9. Amplitude can help validate if different burst packets are present.

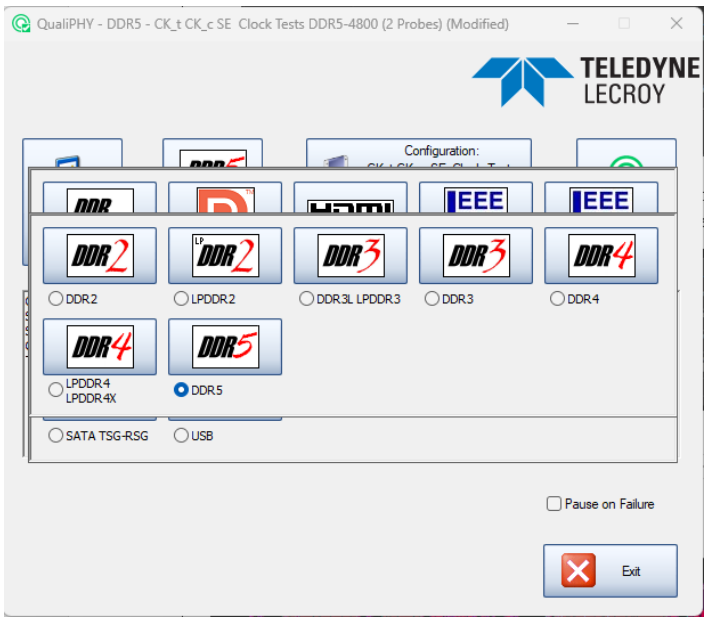
Test Initiation

Follow these steps to begin a new DDR test session in QualiPHY:

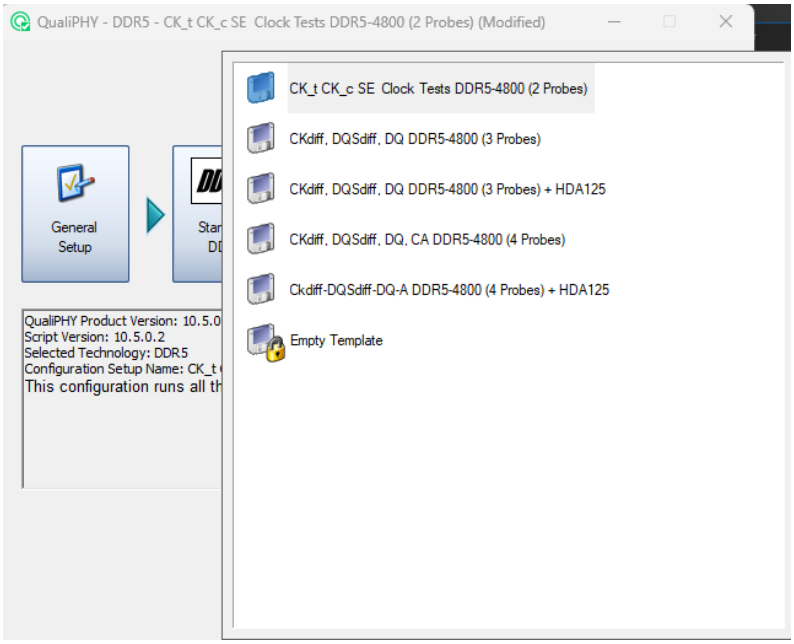
1. Access QualiPHY by either:
   - Choosing **Analysis > QualiPHY** from the oscilloscope menu bar
   - Double-clicking the **QualiPHY desktop icon**  on a remote computer or oscilloscope desktop.
2. Open the QualiPHY wizard, select the **Standard** button and choose **DDR**:



3. Select the memory type you wish to test (e.g., DDR5).



4. On the wizard, click the **Configuration** button and select the test configuration you wish to run. The standard configurations are preset to run tests according to JEDEC test standards. Different configurations are designed to set key variables as required for different probing setups or testing different types of DUTs, etc.



5. Click **Edit/View Configuration** and modify any variables required on the Setup tab.

   Tip: You can work back and forth between the Setup and Variable Setup tabs until all selections are made.

   Note: Standard configurations are locked and cannot be changed. If you need to change any test selections or variables, you will be prompted to Save As a new configuration. See Customizing QualiPHY for more information about creating custom configurations.

6. On the wizard, click the **Configuration** button and select the new, modified configuration.
7. click the **Start** button when ready to begin testing.

8. As connection diagrams appear, follow the instructions to set up the test equipment.

DDR5 Test Configurations

Standard configurations have been created to provide a starting point for DDR5 testing. These configurations include different probing setups, measurement selections, and variable and threshold settings. Click the **Configuration** button on the wizard dialog to view the list of configurations from which you may choose.

To begin, load a test configuration that is closest to what you'll need, edit it for your desired setup, then save a copy for future use. See DDR5 Test Descriptions and DDR5 Variables and Limits for more information about each.

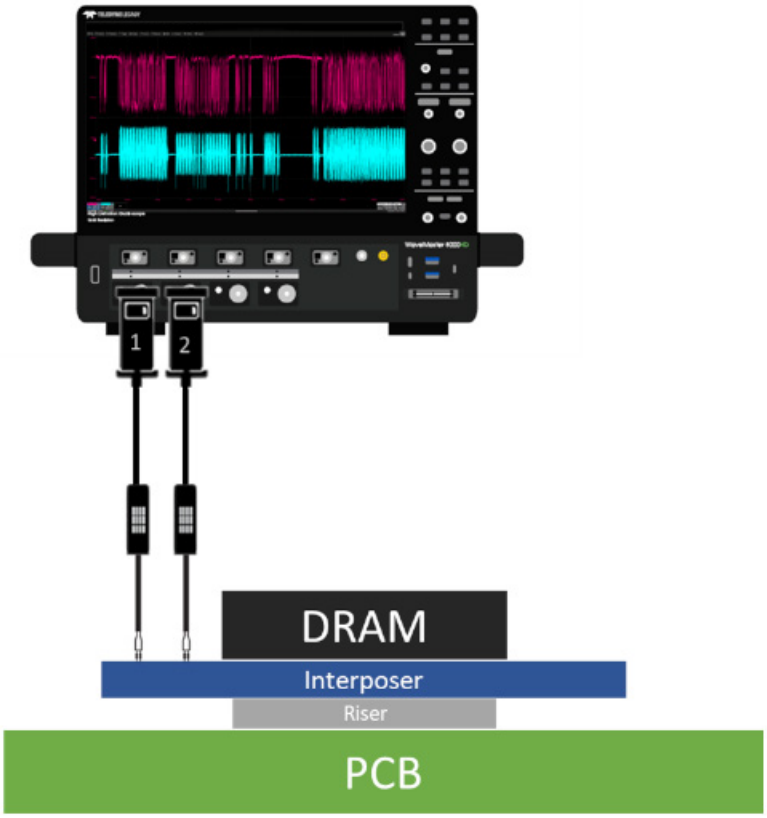
Note: The configurations below are customized for different DDR and probing setups. For example, the configuration named CK_t CK_c SE Clock Tests DDR5-4800 (2 Probes) will run Clock tests using two analog probes at the 4800 MT/s speed grade. The descriptions here show the default channel and line assignments for each input, however these defaults can be changed if necessary to match your actual probing configuration on the Edit/View Configuration Setup tab.

Important! Custom configurations will be erased when making a firmware upgrade.

Note: For the most part, the same tests within each configuration are conducted in the same manner. Exceptions will be noted in the manual.

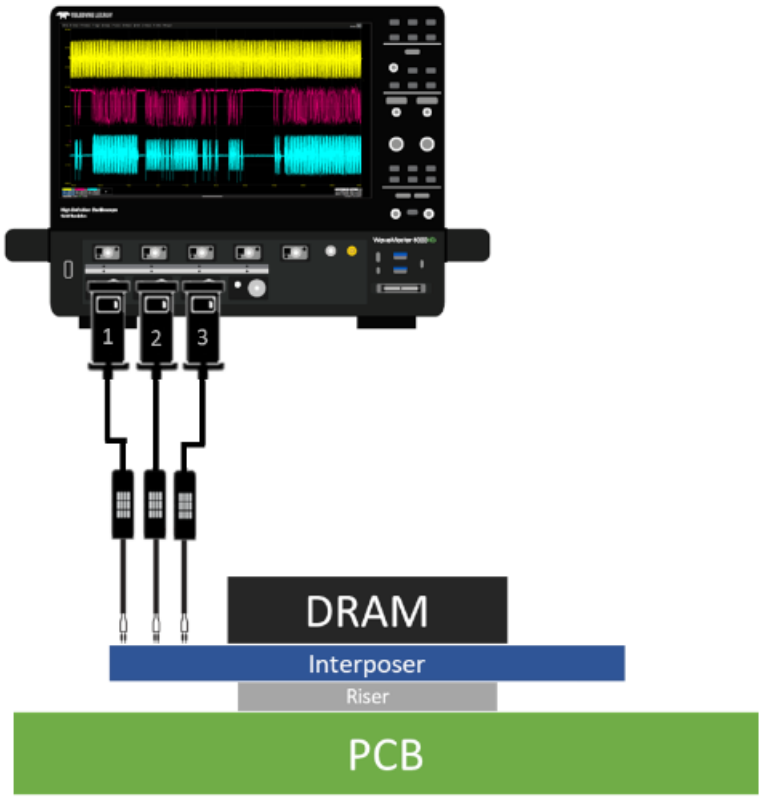
CK_t CK_c SE Clock Tests DDR5-4800 (2 Probes)

This configuration runs all the tests in which two, single-ended Clock inputs (2 probes) are required. A probe is connected to each single-ended Clock line, the CK_t (True) to GND on CH1 and the CK_c (Complement) to GND on CH2. The speed grade, measurements and JEDEC limits are set up for DDR5 4800 MT/s testing. No HDA125 is used in this configuration.



Ckdiff, DQSdiff, DQ DDR5-4800 (3 Probes)

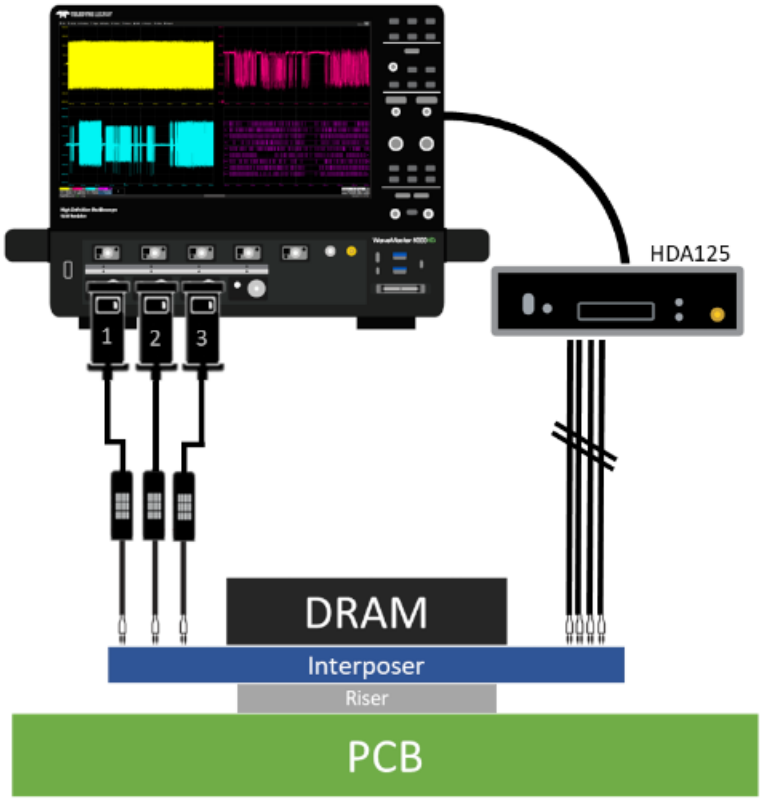
This configuration runs all the DDR5 system level tests in which Clock (CK), Strobe (DQS) and Data (DQ) inputs (3 probes) are required. A probe is connected to the differential Clock (CK_t & CK_c) on CH1, the differential Strobe (DQS_t & DQS_c) on CH2 and single-ended Data (DQ & GND) on CH3. The speed grade, measurements and JEDEC limits are set up for DDR5 4800 MT/s testing. No HDA125 is used in this configuration.



Ckdiff, DQSdiff, DQ DDR5-4800 (3 Probes) + HDA125

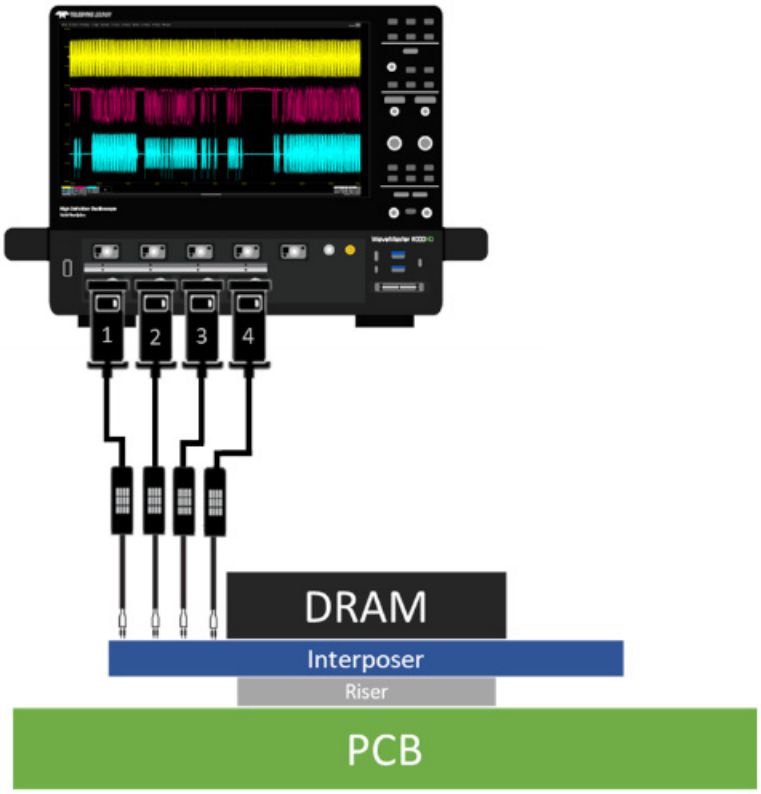
This configuration runs all the DDR5 system level tests in which Clock (CK), Strobe (DQS), and Data (DQ) inputs (3 probes) are required. A probe is connected to the differential Clock (CK_t & CK_c) on CH1, the differential Strobe (DQS_t & DQS_c) on CH2, and single-ended Data (DQ & GND) on CH3. The speed grade, measurements and JEDEC limits are set up for DDR5 4800 MT/s testing.

This configuration is additionally set up to use the HDA125 to probe the Command Bus, which improves accuracy in performing Read and Write packet separation, at these default settings: CS Line D9, CA0 Line D10, CA1 Line D11, CA2 Line D12, CA3 Line D13, CA4 Line D14, CA9 Line D15, CA10 Line D16, CA12 Line D17; HDA Read Latency 34; HDA Write Latency 32, Default (logic) threshold -0.700 V.



Ckdiff, DQSdiff, DQ, CA DDR5-4800 (4 Probes)

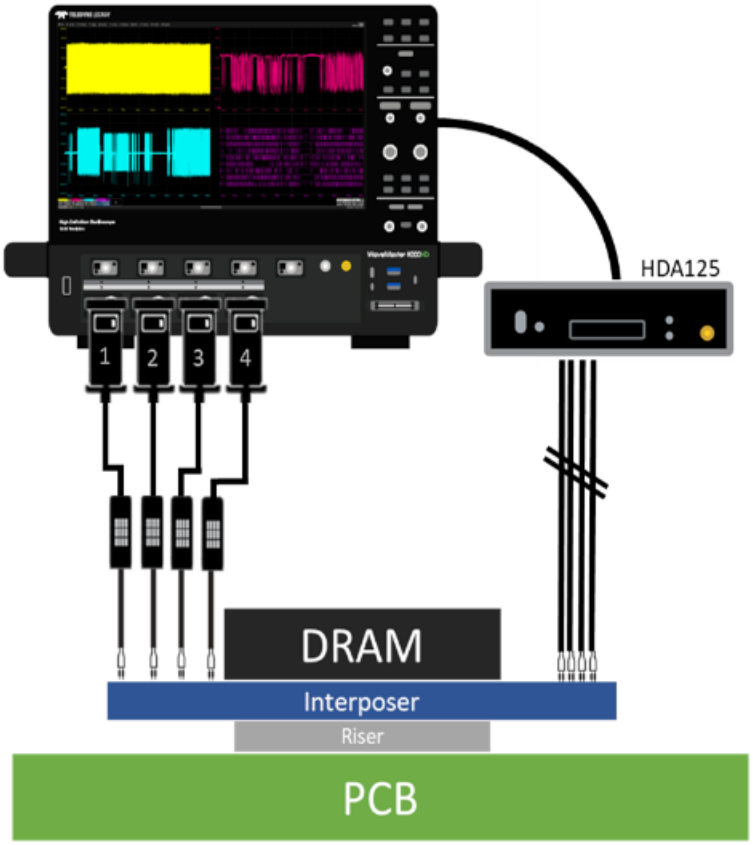
This configuration runs all the DDR5 system level tests in which Clock (CK), Strobe (DQS), Data (DQ) and Command Address (CA) inputs (4 probes) are required. A probe is connected to the differential Clock (CK_t & CK_c) on CH1, the differential Strobe (DQS_t & DQS_c) on CH2, single-ended Data (DQ & GND) on CH3, and single-ended Command Address (CAx & GND) on CH4. The speed grade, measurements and JEDEC limits are set up for DDR5 4800 MT/s testing. No HDA125 is used in this configuration.



Ckdiff, DQSdiff, DQ, CA DDR5-4800 (4 Probes) + HDA125

This configuration runs all the DDR5 system level tests in which Clock (CK), Strobe (DQS), Data (DQ) and Command Address (CA) inputs (4 probes) are required. A probe is connected to the differential Clock (CK_t & CK_c) on CH1, the differential Strobe (DQS_t & DQS_c) on CH2, single-ended Data (DQ & GND) on CH3, and single-ended Command Address (CAx & GND) on CH4. The speed grade, measurements and JEDEC limits are set up for DDR5 4800 MT/s testing.

This configuration is additionally set up to use the HDA125 to probe the Command Bus, which improves accuracy in performing Read and Write packet separation, at these default settings: CS Line D9, CA0 Line D10, CA1 Line D11, CA2 Line D12, CA3 Line D13, CA4 Line D14, CA9 Line D15, CA10 Line D16, CA12 Line D17; HDA Read Latency 34; HDA Write Latency 32, Default (logic) threshold -0.700 V.



Empty Template

All tests are left deselected to allow creation of a custom configuration. All variables are set to their defaults.

Setup Tab Configuration

After making the initial configuration selection based on your probing, select **Edit/View Configuration** on the wizard dialog and use the Setup tab to refine the test settings.

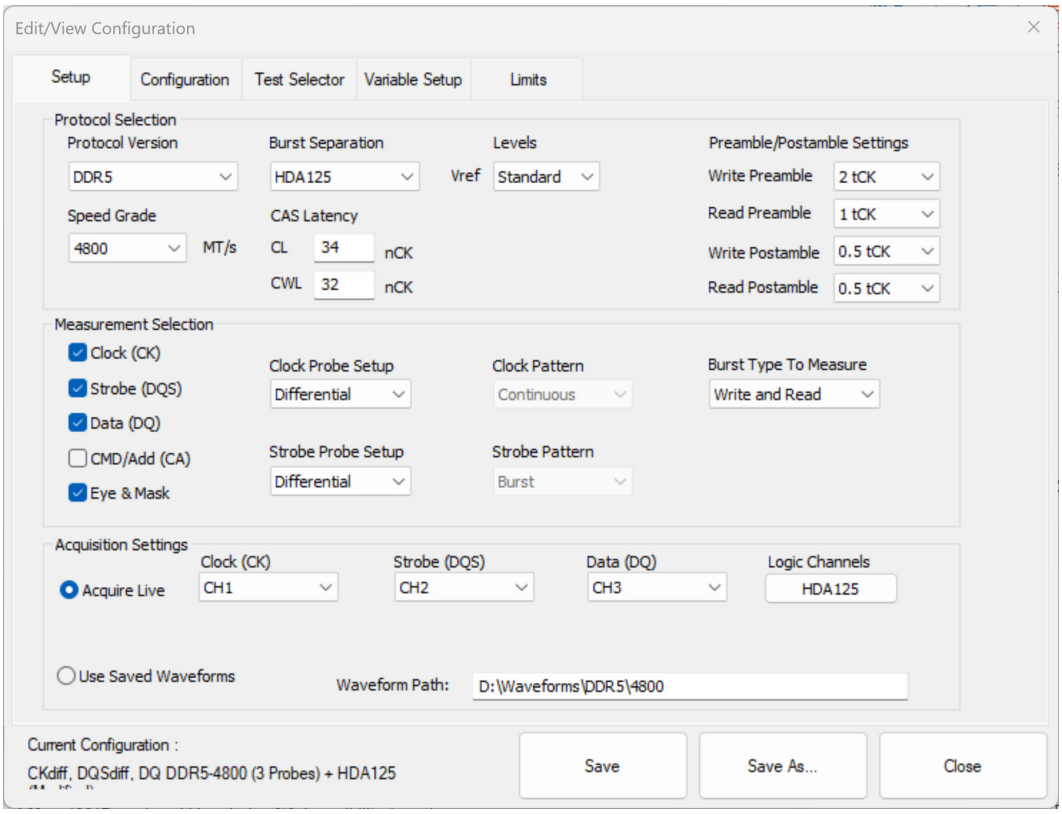


Figure 10.The DDR5 Setup tab contains all important variable selections.

Protocol Version: Select the version of the DDR standard to test for compliance. All the configurations will preset this to DDR5, but you can choose an older version of the standard to test for backward compatibility.

Speed Grade: Choose the operating memory speed.

Note: Be sure the Limit Set that matches the Speed Grade is selected on the Limits tab (e.g., Speed Grade 4800 MT/s matches Limit Set DDR5-4800.)

Burst Separation: Choose to identify Read and Write burst using DQ/DQS Phase detection, the command bus probed with the HDA125, or CA4 + Latency. See p.12 for a description of each.

Note: If using HDA125, click the Logic Channels HDA125 button to enter your line inputs (see below).

CAS Latency: Enter the number of nCKs latency for the CL (Read) and CWL (Write). This is especially important when using the HDA125 or the CA4+Latency burst separation method.

Levels: Choose the Vref logic Level type. Custom allows you to enter a value in V. Standard defaults to the values specified by the standard. Auto makes a best estimate of values based on an internal algorithm.

Preamble/Postamble Setup: Enter the number of tCKs in the Write/Read Preamble and the Write/Read Postamble.

Measurement Selection: Select all the types of tests to run. This will automatically make the required selections on the Test Selector tab.

Clock Probe Setup and **Strobe Probe Setup**: Choose your probing configuration.

Clock Pattern and **Strobe Pattern**: Choose either Continuous or Burst(ed).

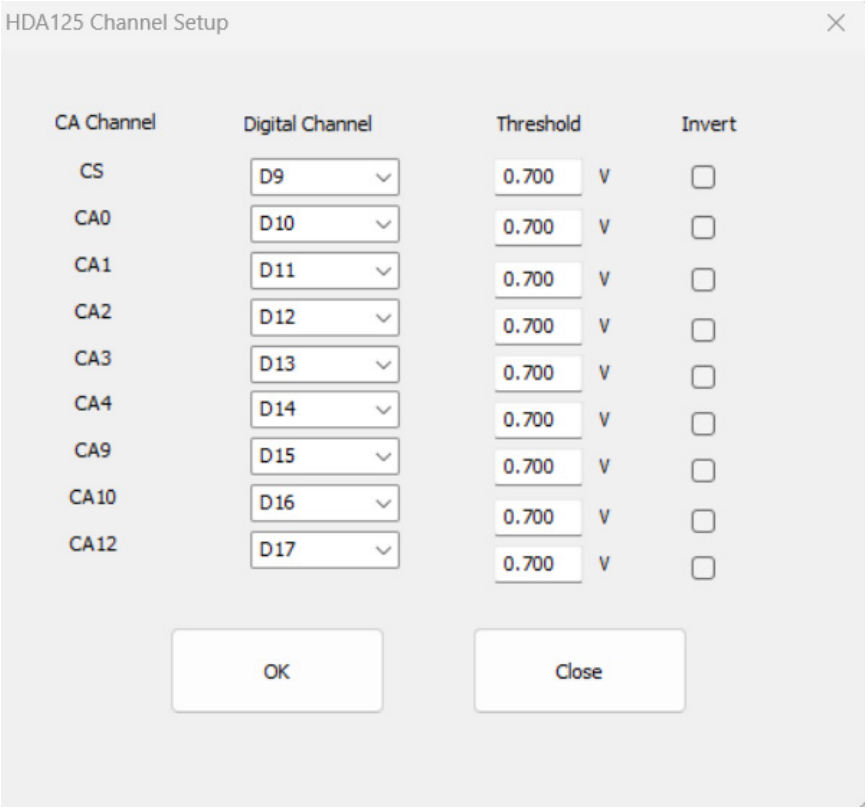
Burst Type To Measure: Choose Write only, Read only, or Write and Read.

Acquire Live and Use Saved Waveforms: Select whether to run tests on newly acquired signals or on saved waveform files.

Clock (CK), Strobe (DQS) and Data (DQ): Select the input channel used for each when acquiring live signals. If you are using single-ended probing, a second field will appear for entering the clock and strobe inputs' True (*_t) and Complement (*_c) channels.

CMD/Address (CA4): If using the CA4 + Latency burst separation method, enter the CA4 line input channel.

Logic Channels: If using HDA125 burst separation method, click the HDA125 button and enter the Digital Channel (lines D0-D17) used to input each command bus signal. Enter the logic voltage Threshold for each. If you have connected any line with reversed polarity, you can use the checkbox to Invert the signal. Click OK to save these values, then Close.



Waveform Path: enter the full path to the waveform files when using saved waveforms.

When you have entered all Setup variables, click Save As if you're editing one of our standard configurations and give the new configuration a name. If you're editing a custom configuration, you can either Save these changes to it, or also Save As a new configuration.

Before testing, click the Configuration button on the wizard and select the modified configuration from the list.

DDR5 Test Descriptions

These are the DDR5 compliance tests. The required tests for each type of measurement selected on the Setup tab are preselected, and you should rarely have to adjust these selections unless you are creating custom configurations for internal testing.

Unless stated, tests are conducted in the same manner for all JEDEC memory standards.

Probe Auto Zero

Select this to perform a probe Auto Zero sequence at the beginning of the test sequence. This step should always be performed when changing probes or for the first run after power up.

Note: If the Deskew test is also selected, the Auto Zero will be performed during the deskew procedure.

Deskew

Select this to perform a probe-to-probe deskew. A deskew should always be performed when changing the probe configuration. Deskew settings are saved and re-used by default. Another important reason to perform deskew is to correctly synchronize your analog channels to the digital HDA125 channels (if using). Being off a couple Clock cycles can cause serial R/W separation issue once you've entered your CL/CWL Latencies.

Clock Tests

In DDR5, the Clock tests are split into Single-Ended and Differential configurations. To properly perform Clock tests, know which measurements you want to perform and make sure your probe connections are set up correctly. For instance, VIX_CK_Ratio needs both the CK_t (True) and CK_c (Complement) signals and a Clock Probe Setup of Single-Ended.

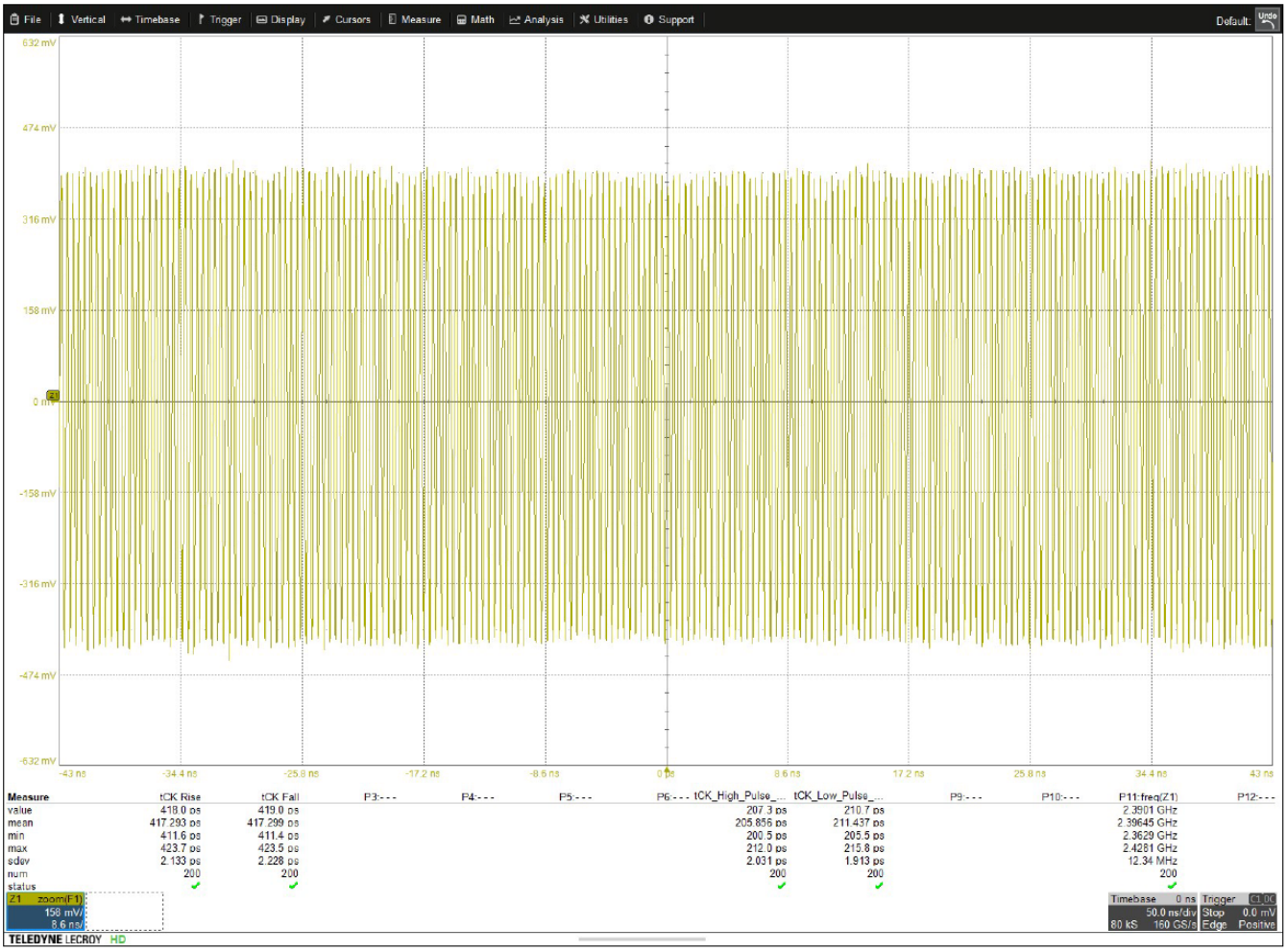
To add these tests, choose Clock (CK) from the Setup tab Measurements Selection, pick the probe setup used, then go to the Acquisition Settings variables to confirm the channel inputs. This will automatically select the appropriate Clock measurements from the Test Selector tab.

tCK

JEDEC defines a set of input Clock jitter specifications. The tCK is called the “DRAM Reference Clock Frequency” and is required to be measured within +/- 0.0001 MHz of the fundamental frequency f0. This is defined as f0 = (Data Rate)/2.

For example, if f0 = 3200/2 = 1,600 MHz, the JEDEC requires the Clock to frequency to be between 1,599.8 MHz and 1,601.6 MHz.

At the completion of the tCK test, the oscilloscope saves a screenshot of the waveforms and the frequency measurements being performed for the report, similar to that below:



Clock Tests

Figure 11. Clock signal being measured for tCK.

As can be seen in the above picture, the Clock signal is present on Channel 1 and the measurement system is validating the average frequency of the Clock signal to make sure there isn’t too much variation in its frequency. Then it compares that to the JEDEC standard’s tCK limits defined for the appropriate speed.

tCK_Duty_UI_Error

JEDEC defines a set of input Clock jitter specifications. The tCK_Duty_UI_Error is called the “Duty Cycle Error”. It’s the absolute difference between average value of all UI with that of average odd or even UIs. This is measured to the max/min limits set in the DDR5 JEDEC standard.

At the completion of the tCK_Duty_UI_Error test, the oscilloscope saves a Pass/Fail result of the measurement, saves the test criteria and current value, along with a time-stamp of when the test was performed.

✔ Pass	Measurement:	***tCK_Duty_UI_Error***		
	Current Value:	13 mUI	Test Criteria:	x <= 50 mUI
	Timestamp:	11/03/2023 12:47:37	Limit Name:	tCKDutyUiErrorLimit
	Description:	Test is to measure the duty cycle error.		

VIX_CK_Ratio

The Clock Differential Input Crossing Voltage Ratio (VIX_CK_Ratio) is designed to confirm the single-ended CK_t (True) and CK_c (Complement) crossing point locations are within 50% of the RMS voltage range when referenced to the mid reference level VIX_CK = (CK_t + CK_c)/2. The VIX_CK is the mean over 8 unit intervals.

This measurement requires that the setup includes two probes, one for the Clock True and another for the Clock Complement. Make sure each probe is connected between the signal to the device ground.

Run the QualiPHY test and at completion, the oscilloscope will save a screenshot with annotations of where the measurement is being performed as seen in Figure 10 below.

✔ Pass	Measurement:	***VIX_CK_Ratio***		
	Current Value:	4.972 %	Test Criteria:	x <= 50.000 %
	Timestamp:	11/09/2023 14:43:33	Limit Name:	VIX_CK_Ratio_Limit
	Description:	Test is to verify the differential input crosspoint voltage ratio, VIX_CK_Ratio parameter.		

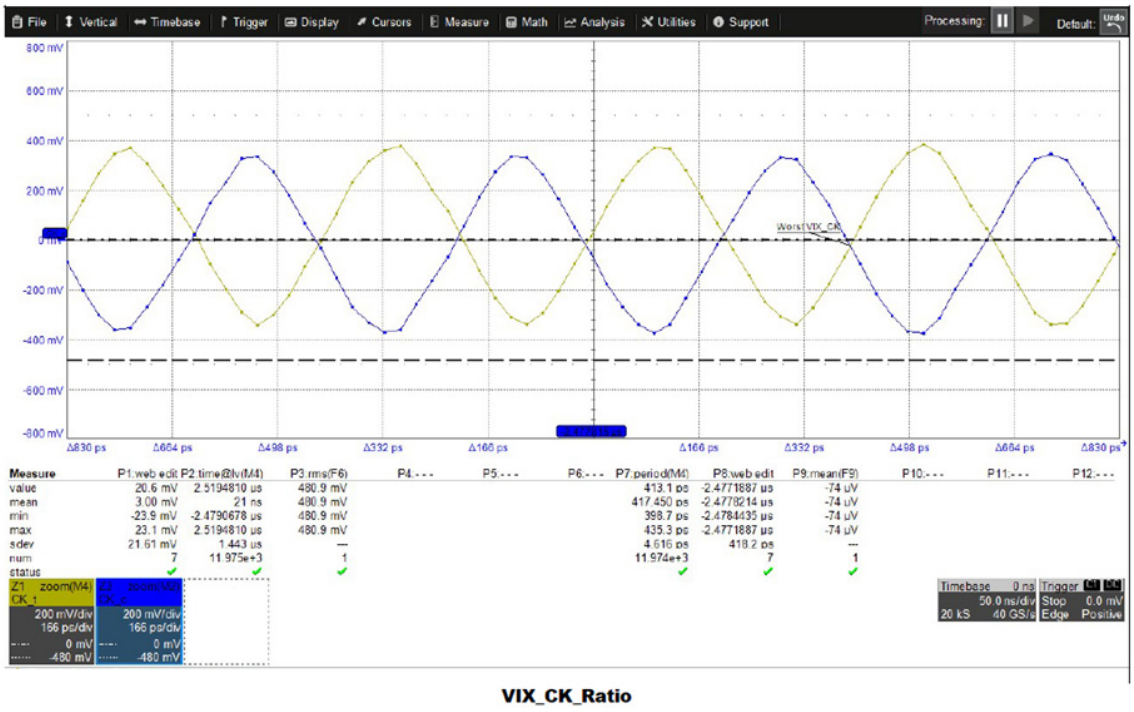


Figure 12. Annotated screenshot of the VIX_CK_Ratio measurement.

AC Over/Undershoot Peak and Area

This test measures the overshoot/undershoot pk and area measurements on single-ended CK_t and CK_c signals. The measurements performed are:

VCOSP: Maximum peak amplitude above VCOS

VCUS: Maximum peak amplitude allowed for undershoot

ACOS1: Maximum overshoot area per 1 UI between VDD and VDOS

ACOS2: Maximum overshoot area per 1 UI above VCOS

ACUS: Maximum undershoot area per 1 UI below VSS

Jitter Tests

1, 2, 3 UI Rj, Dj, Tj (no BUj)

This test measures Random jitter (Rj), Deterministic jitter (Dj) and Total jitter (Tj) using the dual-Dirac jitter model, where 1, 2 and 3 UI measurements constitute the data set for the measurement. Rj, Dj and Tj are determined at a BER configured by the user.

*n*UI Rj, Dj, Tj (no BUj)

This test measures Random jitter (Rj), Deterministic jitter (Dj) and Total jitter (Tj) using the dual-Dirac jitter model, where *n*UI measurements constitute the data set for the measurement. Rj, Dj and Tj are determined at a BER and number of UIs (*n*UI) configured by the user.

Eye Diagram Tests

CA/CS: VIHL_AC

Analysis on the Command Address (CA) or Chip Select (CS) lines is important for signal quality inspection. Testing one or more signal lines is preferred, but the shortest and longest trace lengths will typically give you a good approximation to find how bad the worst case appears.

VIHL_AC is a measurement that tests the peak-to-peak amplitude of the CA or CS signal for each pulse during a vertical alignment with a mask diagram. The amplitudes during this time are compared to the limits set by the JEDEC based on the corresponding speed level.

Additionally, anytime a CA/CS line are measured ≥5200 MT/s, the JEDEC requires that users define the CA Package Delay (Tpkg_Delay_CA) as being Option 1 (35ps), Option 2 (32ps) or Option 3 (29ps); and capacitance CI_Max range (0.50pF or 0.55pF). As these package settings alter the allowable minimum allowed amplitudes at higher speeds.

CA Eye Mask Test: TcIVW/VcIVW

VcIVW and TcIVW define the voltage and timing margin for the CA input receiver mask. The receiver mask (Rx Mask) defines the area that the signal must not encroach for the DRAM input receiver to successfully capture a valid input signal.

Electrical Tests on Write Bursts (Inputs)

Differential Amplitude and Levels: VIHdiff, VILdiff

VIHdiff (AC)_CK and VIHdiff (DC)_CK

These tests measure the min and max voltage of the high-level AC and DC levels of a differential clock signal. This is referred as the Voltage Input High (VIHdiff) and is reference measured from the 0 V position. The minimum and maximum across all AC and DC locations of the clocks occur during the Input (Write) timings of packets.

Probing for this signal is with a differential probe across the CK_t (True) and CK_c (Complement) at the ball of the DRAM (at the BGA).

This is an informational only test that is not required by the JEDEC but has been historically measured in DDR standards to help users understand the ranges often used for slew rates and other measurements. Therefor there is no pass/fail reported or test criterial limits.

VILdiff (AC)_CK and VILdiff (DC)_CK

These tests measure the min and max voltage of the low-level AC and DC levels of a differential clock signal. This is referred as the Voltage Input High (VIHdiff) and is reference measured from the 0 V position. The minimum and maximum across all AC and DC locations of the clocks occur during the Input (Write) timings of packets.

Probing for this signal is with a differential probe across the CK_t (True) and CK_c (Complement) at the ball of the DRAM (at the BGA).

This is an informational only test that is not required by the JEDEC but has been historically measured in DDR standards to help users understand the ranges often used for slew rates and other measurements. Therefore, there is no pass/fail reported or test criterial limits.

Input Slewrate

The purpose of these tests is to characterize the slewrate on all the Write (input) signals. The tests are performed on both rising and falling edges. By default, the slewrate is measured only on Clock (CK) signals.

SRIdiff_DQS

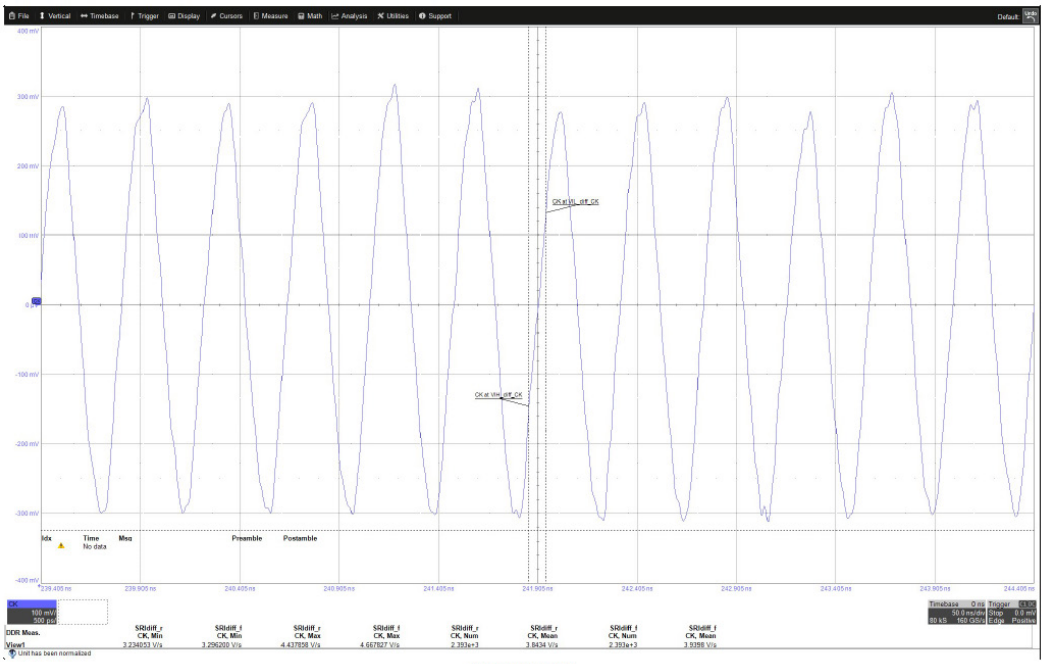
This test measures the rising and falling slew rate of the differential input (write) strobe signals (DQS_t & DQS_c), reporting the maximum and minimum value and validating if any rising or falling sew rates fall outside the limits set by JEDEC. The thresholds are measured as the 25% to 75% for the corresponding VIH and VIL levels.

SRIdiff_CK

This test measures the rising and falling slew rate of the differentially acquired input clock signal. It requires a probe to be connected to the (CK_t & CK_c) signals. It then measures the max and min values of all signals and validates if any slew rate limits fall outside the JEDEC requirements. The thresholds are measured as the 25% to 75% (<6800 MT/s) and 30% to 70% (>6400 MT/s) for the corresponding VIH and VIL threshold levels.

The QualiPHY report will show annotations of where the slewrate is measured between the VILdiff and VIHdiff locations. The result will show a graph for the minimum vs. maximum value locations. Results are in volts per nanoseconds (V/ns).

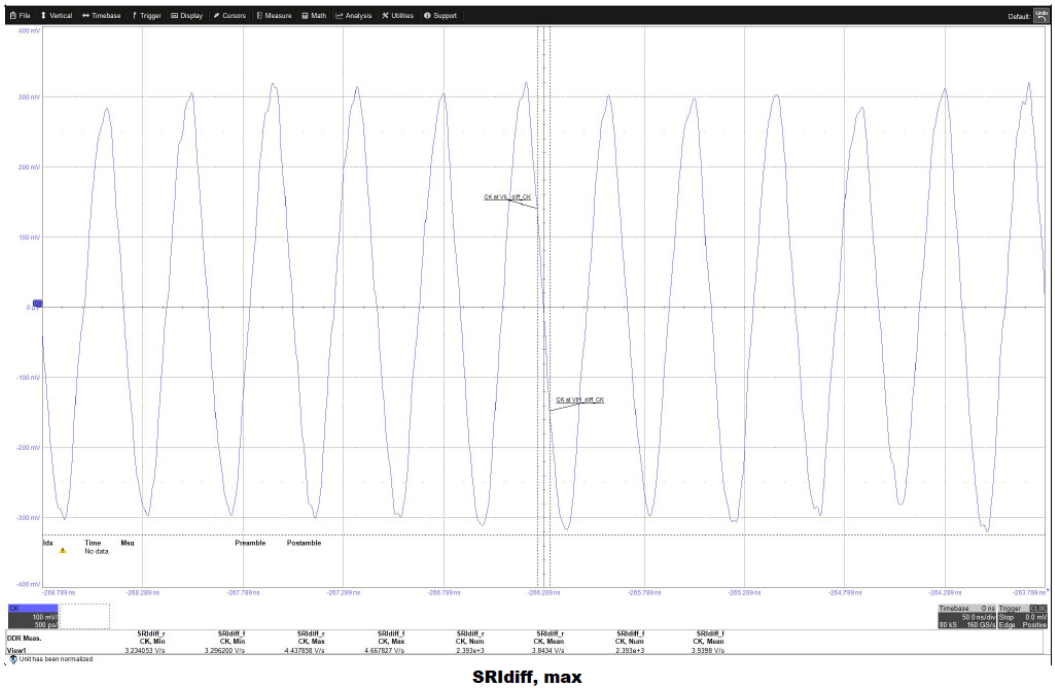
✔ Pass	Measurement:	***SRIdiff, min***		
	Current Value:	3.234 V/ns	Test Criteria:	x >= 2.000 V/ns
	Timestamp:	11/16/2023 16:16:26	Limit Name:	SRIdiff_CK_min
	Description:	Differential Input Slew Rate, min (CK)		



SRIdiff, min

Figure 13. SRIdiff, min test makes sure the minimum slew rate is >2 V/ns on the clock signal.

Pass	Measurement: ***SRIdiff, max***		
	Current Value: 4.668 V/ns	Test Criteria:	x <= 14.000 V/ns
	Timestamp: 11/16/2023 16:16:28	Limit Name:	SRIdiff_CK_max
	Description: Differential Input Slew Rate, max (CK)		



SRIdiff, max

Figure 14. SRIdiff, max test makes sure the maximum slew rate is <14 V/ns on the clock signal.

SRIN_clVW

The JEDEC defines “Input Slew Rate over VcIVW” for CA signals when measuring around the Rx Mask. The Rx Mask is defined by the mask height (VcIVW) and width (TcIVW_total) limits in the JEDEC specification. The mask is centered around Vcent_CA (pin mid) and this reference point is used for the min/max slew rate measurements.

Note: If errors arise, go into DDR Debug and validate the VrefCA threshold is correct for the signal.

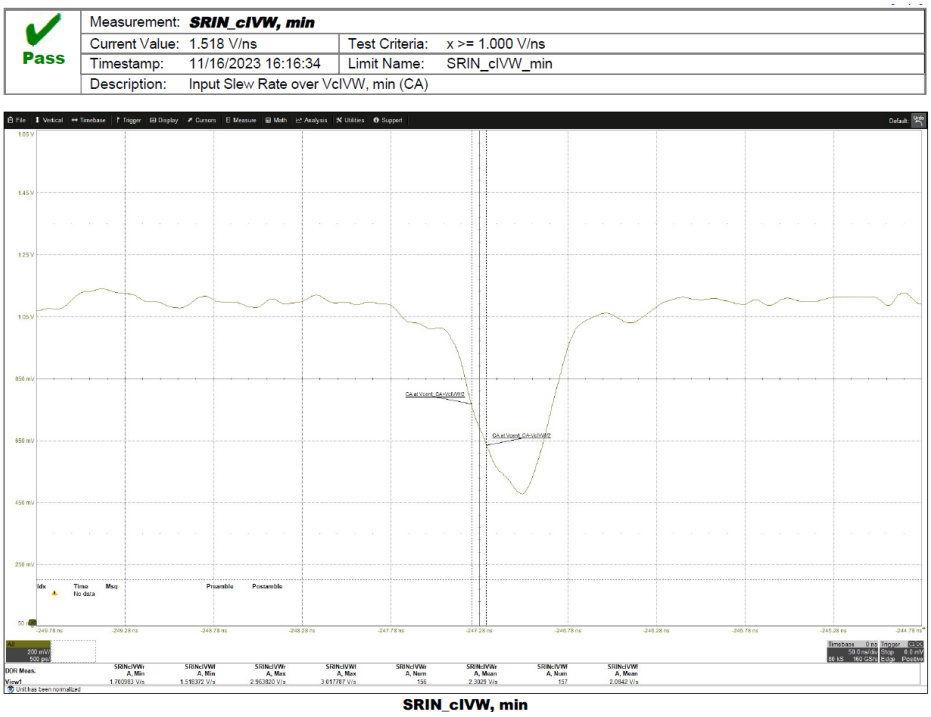


Figure 15. SRIN_clVW, min test checks that the minimum CA slew is greater than 1 V/ns.

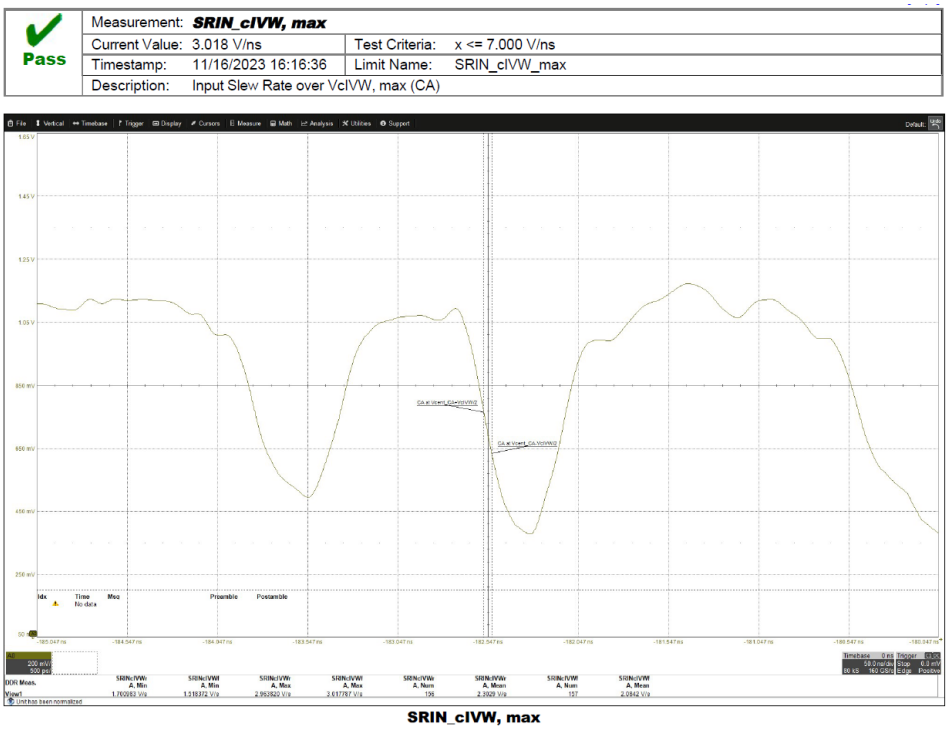


Figure 16. SRIN_clVW, max test checks that the maximum CA slew is less than 7 V/ns.

DQS Single-ended Tests

VIX_DQS_Ratio

The Differential Strobe Input Crossing Voltage Ratio (VIX_DQS_Ratio) is designed to confirm the single ended DQS_t (True) and DQS _c (Compliment) crossing point locations are within 50% of the RMS voltage range when referenced to the mid reference level VIX_ DQS = (DQS _t + DQS _c)/2. The VIX_ DQS is the mean over 8 unit intervals.

Electrical Tests on Read Bursts (Outputs)

VOH(AC)_DQ and VOH(DC)_DQ

These tests measure the min and max voltage of the high-level AC and DC thresholds of a data (DQ) signal. This is referred as the Voltage Output High (VOH). The minimum and maximum across all AC and DC locations are measured across all detected output (Read) packets.

This is an informational only test that is not required by the JEDEC but has been historically measured in DDR standards and serves to help users understand the range of this threshold that is often used for slew rates and other measurements. Therefor there is no pass/fail reported or test criterial limits.

VOL(AC)_DQ and VOL(DC)_DQ

These tests measure the min and max voltage of the low-level AC and DC thresholds of a data (DQ) signal. This is referred as the Voltage Output Low (VOL). The minimum and maximum across all AC and DC locations are measured across all detected output (Read) packets.

This is an informational only test that is not required by the JEDEC but has been historically measured in DDR standards and serves to be helpful for users to understand the range of this threshold that is often used for slew rates and other measurements. Therefor there is no pass/fail reported or test criterial limits.

VOHdiff(AC)_DQS and VOLdiff(AC)_DQS

These tests measure the min and max voltage of the high-level and low-level AC thresholds of the strobe (DQS) signal. This is referred as the Voltage Output High Differential (VOHdiff) and Voltage Output Low Differential (VOLdiff). The minimum and maximum across all AC locations are measured across all detected output (Read) packets of the strobe.

Probing for these signals is done using a differential probe across the DQS_t (True) and DQS_c (Complement) at the ball of the DRAM.

This is an informational only test that is not required by the JEDEC but has been historically measured in DDR standards and serves to help users understand the range of this threshold that is often used for slew rates and other measurements. Therefore, there is no pass/fail reported or test criterial limits.

Output Slewrate

The purpose of these tests is to characterize the slewrate on DQ and DQS of all the Read bursts (output) in the acquisition. This test is performed on the Slewrate (SR) of the Query Output (Q) for both Single-ended (se) and Differential (diff) setups (i.e., SRQse and SRQdiff). The rising and falling edges are measured against the minimum and maximum values allowed by the JEDEC standard for its corresponding speed.

Note: Only slewrate measured on the edge of a DQ is shown in the images below. The measurement methodology is exactly the same for both the rising and falling edge.

SRQse

The “single-ended output slew rate” SRQse is defined as the rising and falling edges measured between VOH and VOL across the Strobes DQS_t (True) and DQS_c (Complement) signals, each with its own probe.

The slew rate VOH and VOL thresholds are measured at the 25% to 75% for speeds <6800 MT/s. For >6400 MT/s speeds, this is set to 30% and 70% threshold ranges.

At the completion of the SRQse test, the oscilloscope will display a min and max edge in the following state:

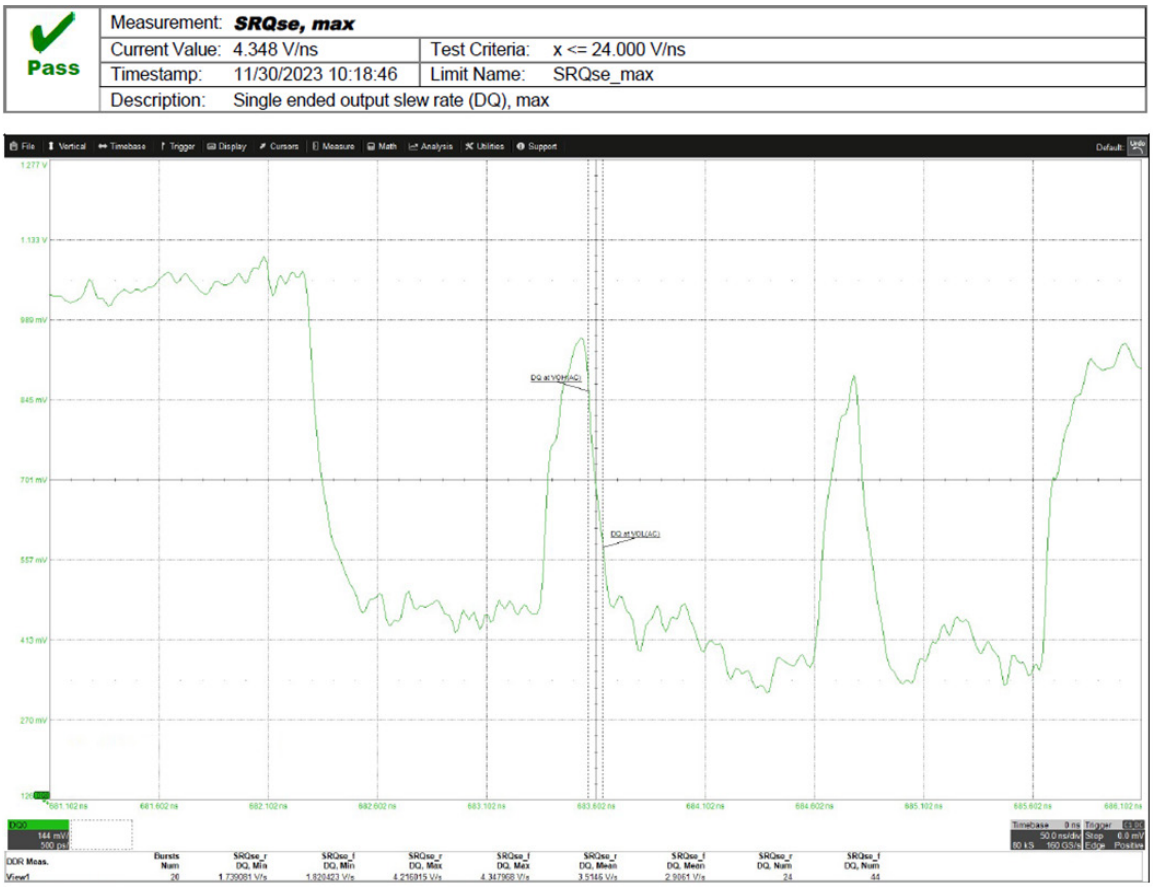


Figure 17. Measurement display after the SRQse test.

Shown in the report:

- A title, description of the current measurement
- A pass or fail result with the current value and expected test criteria outlined by JEDEC
- The acquired DQ signal positioned at the location of the max SRQse falling or rising measurement
- Annotations showing where the current VOH(AC) and VOL(AC) thresholds are located

In the DDR Measure table:

- Burst Num shows the number of Read bursts that were detected.
- SRQse_r min, SRQse_f min, SRQse_r max, SRQse_r min are measuring the slewrate of DQ on the rising and falling edges. This test is passed if the max measured value is less than 24 V/ns.

SRQdiff

The “differential output slew rate” SRQdiff is defined as the rising and falling edges measured between VOH(AC) and VOL(AC) across the Strobes DQS_t (True) and DQS_c (Complement) signals, using one differential probe across both signals.

This test is performed identically to the SRQse process listed above, except it’s occurring on a differential signal.

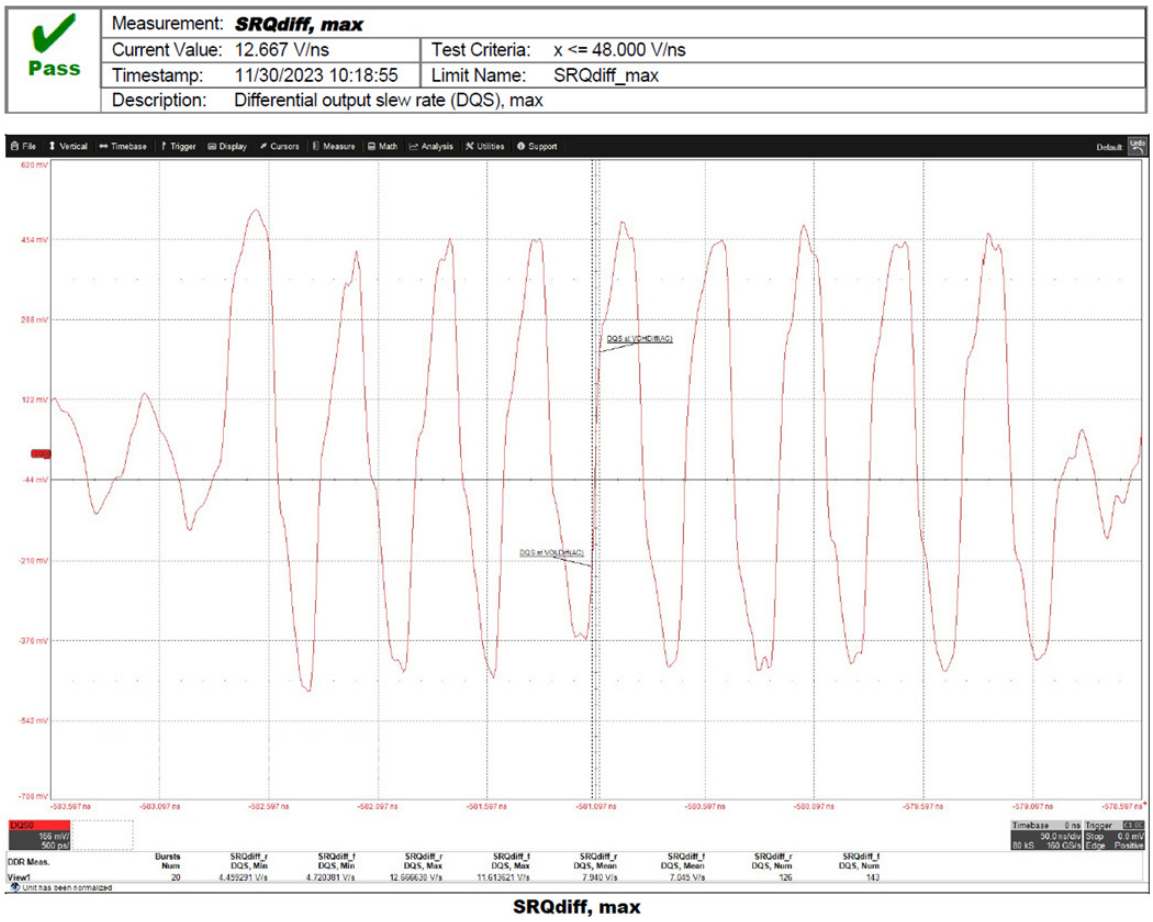
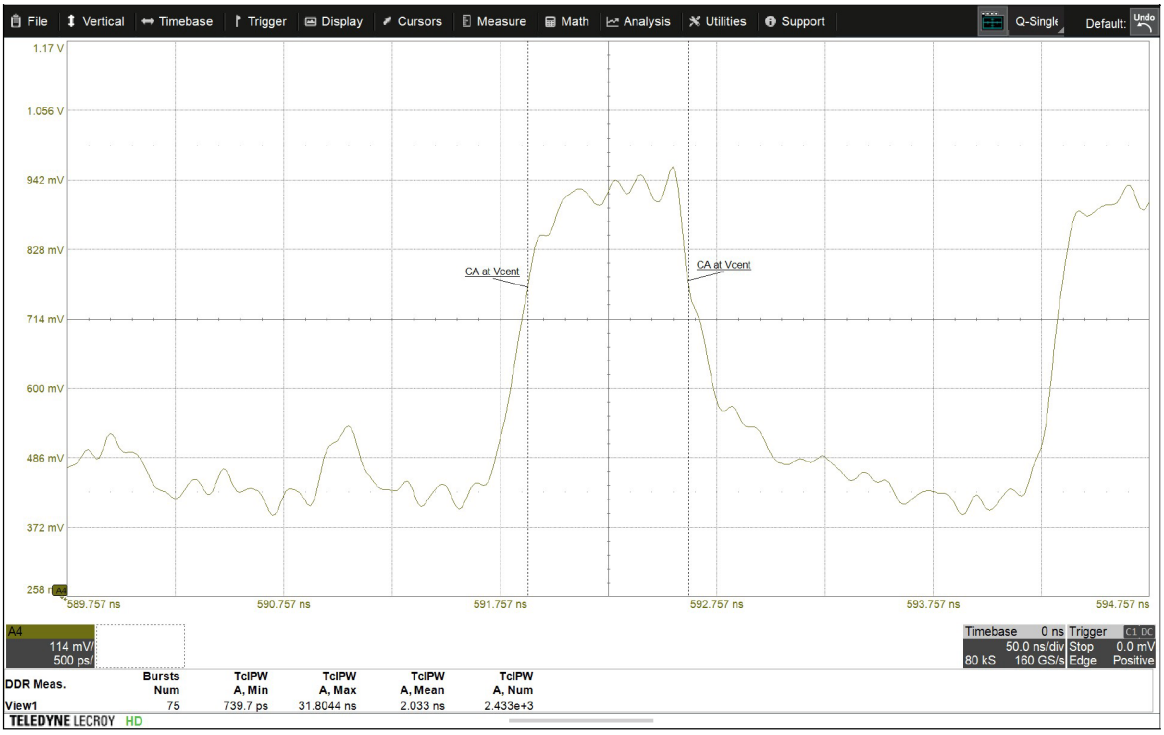


Figure 18. Measurement display after the SRQdiff test.

Timing Tests
Tests on CA
TcIPW
This test measures the CA input pulse width in reference to the Vcent_CA and checks for the minimum pulse width.

Pass	Measurement:	***TcIPW min, CA***	
	Current Value:	3.536 UI	Test Criteria: x >= 580 mUI
	Timestamp:	07/18/2024 13:43:06	Limit Name: TcIPW_min
	Description:	Minimum input pulse width of CA signal (on positive and negative pulse)	



TcIPW min, CA

Tests on Write Bursts
Timing Tests on Bits (not using interpolation)
tDQSS
tDQSS defines the system related drift between DQS to CK.

The min/max limits are set by +/-0.25*tWPRE_EN_ntCK(min), where tWPRE_en is defined by the tCK clock pattern of the pre-amble window, outlined in the JEDEC specification.

At the completion of the tDQSS test, the report will save both a min and max values.

tDQS2DQ
The purpose of this measurement is to measure the offset between the DQ and the DQS signals during the write bursts.

The value is measured between the start of the DQS signal (after the preamble) and first valid bit of DQ.

Note: To obtain a valid measurement result, this test requires a transitioning bit at the first valid bit in the DQ bus. Otherwise, this test uses the first transition bit found, which may yield undesirable results.

Timing Tests on Pre/Postamble (using interpolation)

tDSS
The purpose of this test is to characterize the setup time for a falling DQS edge to the rising clock (CK) edge on Write bursts. The minimum value is measured.

tDSH
The purpose of this test is to characterize the hold time for a falling DQS edge to the rising clock (CK) edge on Write bursts. The minimum value is measured.

twPST
The purpose of this test is to characterize the Postamble time during all Write bursts detected in the acquisition. tWPST measures the timing between when the postamble starts and where the postamble ends. The test uses an interpolation algorithm to improve accuracy in determining the point where the signal begins and signal shape.

tWPRE
The purpose of this test is to characterize the Preamble time during all Write bursts detected in the acquisition. tWPRE measures the timing between when preamble starts and the preamble ends. The test uses an interpolation algorithm to improve accuracy in determining the point where the signal begins and signal shape.

Timing Tests on Read Bursts

Timing Tests on Bits (not using interpolation)

tDQSCK

The purpose of this test is to characterize the allowed range for a rising Data Strobe edge relative to CK on Read bursts. It is measured using a single-ended (DQS_t, DQS_c or DQSdiff signal) rising edge Strobe (DQS) Read packet and is time referenced to the corresponding single-ended rising Clock (CK_t, CK_c or CKdiff signal). The min/max values tCK cycle range is measured to the JEDEC specification.

At the completion of the tDQSCK test, the report will save both a min and max in the following state:

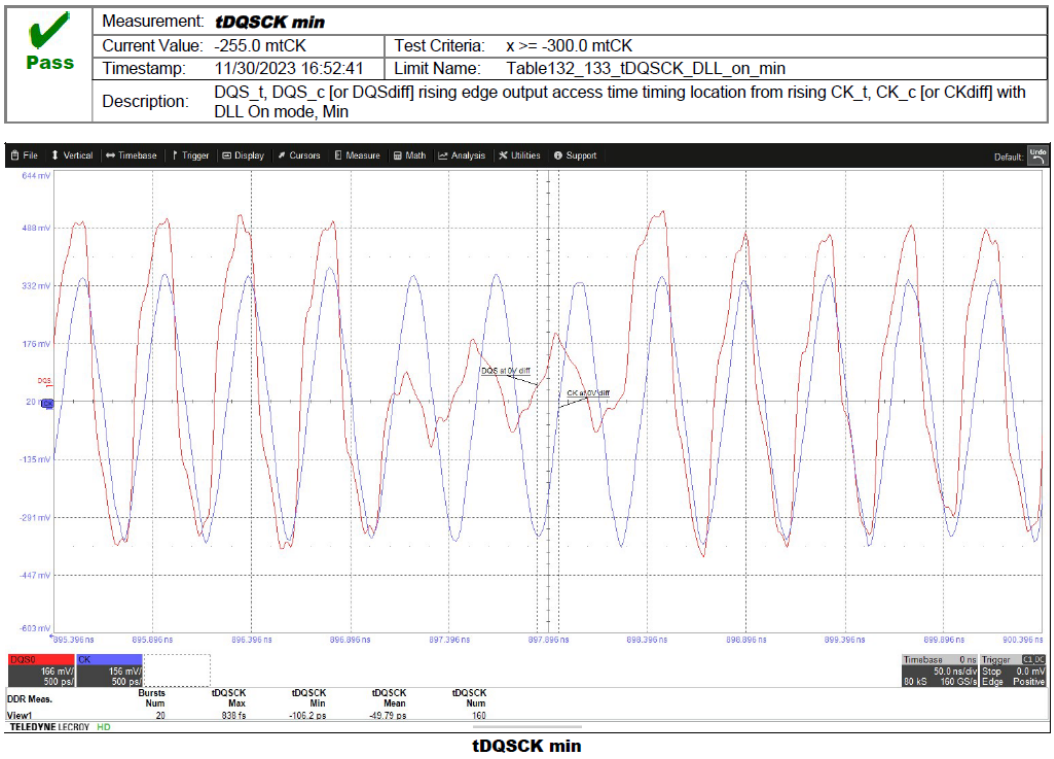


Figure 19. Measurement display after the tDQSCK min test.

Shown in the report:

- A title, description of the current measurement
- A pass or fail result with the current value and expected test criteria outlined by JEDEC
- The acquired DQS and CK signals positioned at the location of the minimum location of a tDQSCK measurement
- Annotations showing where the current 0 V differential thresholds crossing are for the skew between the DQS and CK

In the DDR Measure table:

- Burst Num shows the number of Read bursts that were detected.
- tDQSCK max, tDQSCK min are measuring the time between the DQ and CK rising edges. This test is passed if the minimum time is greater than or equal to -300mtCK.

Timing Tests on Pre/Postamble (using interpolation)

tLZ(DQS) and tHZ(DQS)
The purpose of these tests is to characterize the Low Impedance time (tLZ) and High Impedance time (tHZ). The tests measure the time between when the device quits driving the respective line and CK at Vref. The tests use an interpolation algorithm to improve the positioning of where the signal begins.

Both a minimum and a maximum value are reported.

tLZ(DQS)

The purpose of this test is to verify the time when DQS starts driving (*from High-impedance state to High/Low state) to the nearest rising clock signal crossing.

tLZ tests both a minimum and a maximum value. The test uses an interpolation algorithm to improve the positioning of where the signal begins.

tHZ(DQS)

The purpose of this test is to verify the time when DQS is no longer driving (from High state OR Low state to the High-impedance state) to the reference clock signal crossing.

tHZ tests, both the minimum and maximum value. The test uses an interpolation algorithm to improve the positioning of where the signal begins.

tRPRE and tRPST
The purpose of these tests is to measure the Preamble (tRPRE) and Postamble (tRPST) times for all Read bursts detected in the acquisition. Both tests use an interpolation algorithm to improve accuracy in determining the point where the signal begins and signal shape (as defined by the JEDEC). The minimum times across multiple bursts are captured and displayed as an informative (no JEDEC limits) measurement.

- tRPRE measures the time from the preamble start to end.
- tRPST measures the time from the postamble start to end.

At the completion of the tRPRE and tRPST tests, the report shows the following screenshots, with annotated measurement locations:

Measurement:	***tRPRE min***		
Current Value:	1.048 tCK	Test Criteria:	Informational Only
Timestamp:	11/30/2023 16:52:47	Limit Name:	InfoOnlytCK
Description:	DQS_t, DQS_c differential READ Preamble		

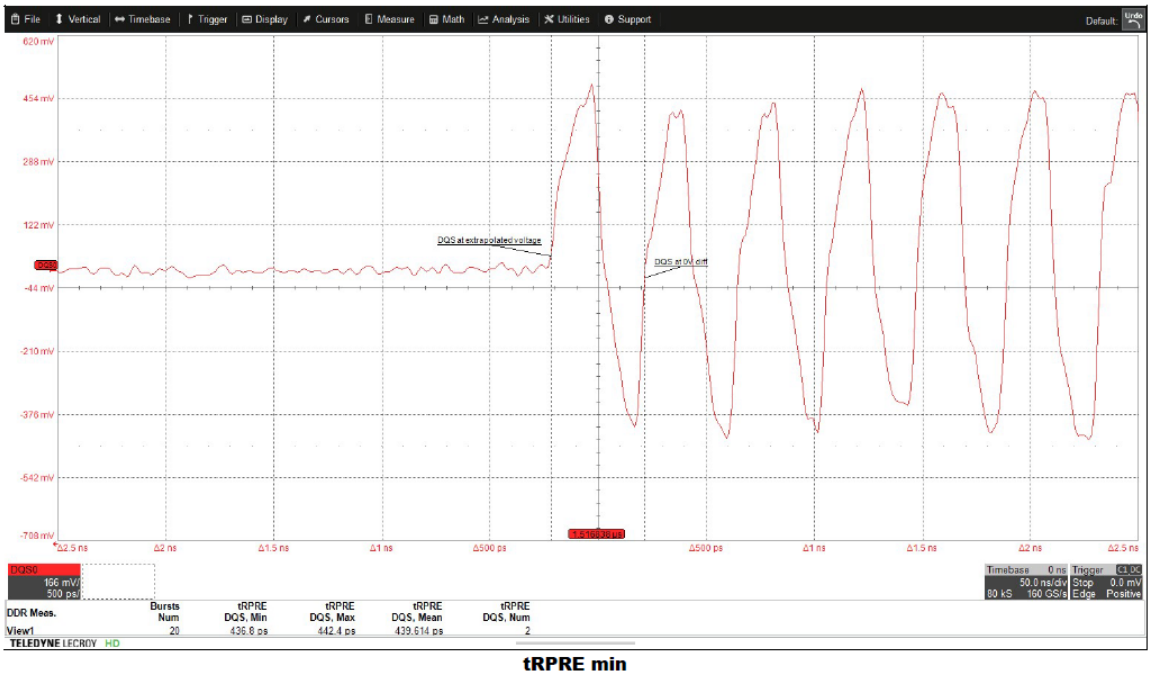


Figure 20. Measurement display after the tRPRE min test.

Measurement:	***tRPST min***		
Current Value:	426 mtCK	Test Criteria:	Informational Only
Timestamp:	11/30/2023 16:52:52	Limit Name:	InfoOnlytCK
Description:	DQS_t, DQS_c differential READ Postamble		

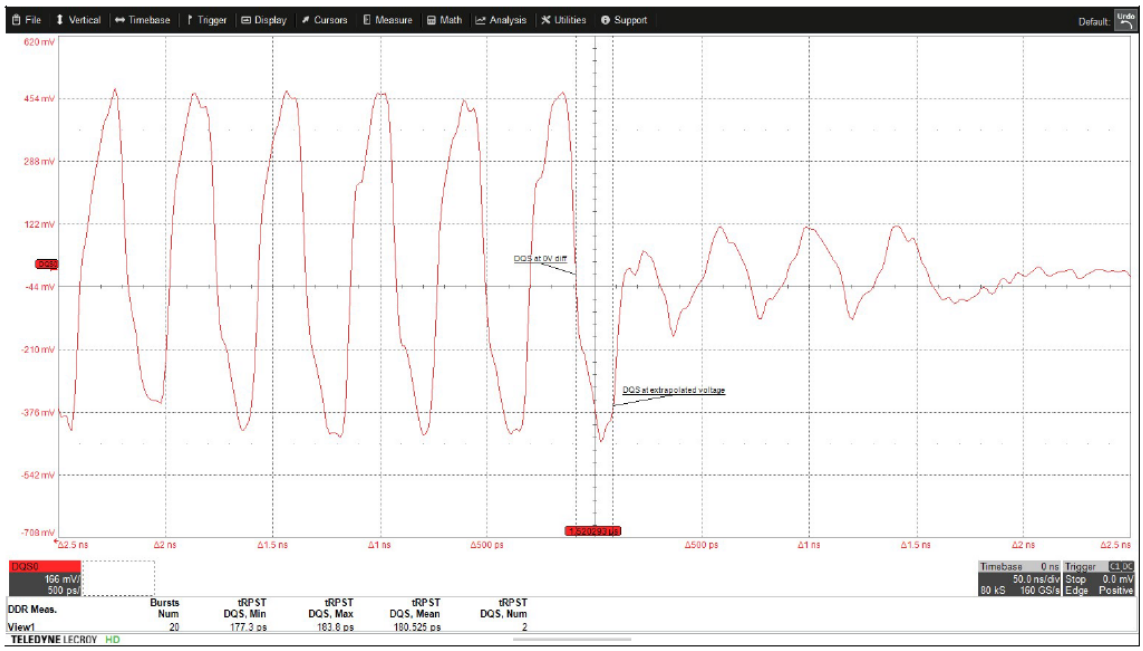


Figure 21. Measurement display after the tRPST min test.

DDR5 Test Variables

Main Settings

Speed Grade
Sets which DDR5 speed grade to use for testing. Default is DDR5-4800. If Custom is selected, in Custom Speed Grade enter the maximum speed that the signal can go up to.

Script Execution Variables

Read/Write Burst Separation Method
Specifies whether to use the phase difference between DQ and DQS analog signals or HDA125 digital signals to identify and separate Read and Write bursts. Default is DQ/DQS.

Use previously saved deskew values?
When set to Yes, QualiPHY will use deskew values previously saved during the manual channel deskew procedure. When No, you will be prompted to repeat the deskew procedure as part of the test. Default is No.

Pause after tests to review results?
When set to Yes, the script stops after each test allowing you to view the results. The setup is saved so the oscilloscope settings can be modified to allow for further debug results. Upon completion of debugging, testing can be seamlessly resumed with one click of a button. Default is No.

Prompt before signal acquisition?
Enables/disables a prompt at the beginning of the signal acquisition sequence. This will allow generation of Read/Write bursts at the start of the acquisition or modify the trigger conditions before signal acquisition. The default value for this variable is No.

Disable connection diagrams?
Disables/enables the display of connection diagrams when probe/cable setups require a change. When No, tests are stopped while the diagrams are displayed; when Yes, diagrams are disabled. Default is No.

Signal Settings
These variables give you control over the signals included in the tests.

CAPackageDelayOption
Select the package delay option to use for the CA line.

CI Max
CI max variable is added to handle different reference voltage level for different value.

Clock Probe Selection Setup
Select the clock signal probing method, Single-Ended or Differential.

Strobe Probe Setup
Select the clock strobe signal probing method, Single-Ended or Differential.

Signal to Test <signal>
For each signal, select “Yes” to include it in the set of signals to test.

Signal to Test Eye and Mask
Select/Unselect the Eye & Mask signal to test.

Analog Signal Channel Assignments

<Signal> Input Channel
For each analog signal (CK_c, CK_t, CK(differential), etc.), select the oscilloscope channel to which it is connected.

HDA125 Digital Signal Assignments
These variables assign different signals and properties to the digital lines.

<Digital Signal> Line
For each digital signal (CS, CA0, CA1, CA2, CA3, etc.), select the HDA125 line over which it is input, or select Not Connected if it is not in use.

HDA Read Latency
Refer to the CAS Read Latency section below.

HDA Write Latency
Refer to the CAS Write Latency section below.

Default Threshold (volts)
Default logic threshold for all lines.

<Digital Signal> Threshold (volts)
For digital signals that are not using the default threshold level, enter individual thresholds in the respective field.

Analog Signal Names

CMD/ADDR
Select the name to use for the Command Address signal to distinguish between different pinouts. The suffix will be included in saved waveform files and in the report. Default is A0.

CK
Select the name to use for the Clock signal to distinguish between different pairs. The suffix will be included in saved waveform files and in the report. Default is CK.

DQ
Select the name to use for the Data signal to distinguish between different signals. The suffix will be included in saved waveform files and in the report. Default is DQ0.

DQS
Select the name to use for the Strobe signal to distinguish between different signals. The suffix will be included in saved waveform files and in the report. Default is DQS0.

Analog Probe Settings
Probe Tip, <Channel *N*>
Specify the tip installed on the probe connected to the respective channel number, C1-C4. Default is SI.

Analog Probe Location Corrections
<Channel> Probe Location Correction (ps)
Time in picoseconds to shift the waveform on the respective channel, C1-C4, *in addition to* the deskew value.

Analog Signal Channel Inversion

Invert <signal> Signal

Select “Yes” to invert the waveform on the respective input channel, Channel 1-Channel 4. Default is No.

Digital Signal Channel Inversion

Invert <signal> Signal

Select “Yes” to invert the respective digital signal (CS, WE, RAS, etc.). Default is No.

Probe and Pattern Setup

Clock and **Strobe Pattern Selection Setup**

Choose whether the signal is operating in Continuous or Bursted mode.

Read Preamble and **Write Preamble**

Enter the number of tCKs in the preamble.

Read Postamble and **Write Postamble**

Enter the number of tCKs in the postamble.

Save/Recall Waveforms

Use stored waveforms?

Select “Yes” to use previously stored waveform in the Waveform Path folder will be used.

Waveform Path

Full path to the folder in which to save waveform files, or from which to recall files when Use stored waveforms? is “Yes”. When running normally, Waveform Path is the root path, with subfolders defined by the DUT name entered on the Operator dialog and the incrementing Run number. When running on stored waveforms, waveform files are recalled from this folder.

Recalled Waveform File Index

5-digit index number of the waveform file to recall when running the script on previously stored waveforms.

Virtual Probe Setup

This group of variables enables you to apply virtual probing to the acquired signals and conduct the DDR measurements on the compensated waveforms.

Virtual Probe Control

Select the type of bursts (Read, Write or Both) to which to apply virtual probe compensation. Select Off to turn off VP compensation.

Virtual Probe Tool Selection

Select the Virtual Probe tool to use.

VP@Receiver math functions simulate the waveform at termination. Use this tool if you are seeing reflections that are too large to get good measurements. When creating the math functions, use F9-F12 for sources C1-C4, in order. Place the saved setup files in the VirtualProbe Path folder.

VirtualProbe utilizes the Virtual Probe toolkit. Use this tool if you have good models of the circuit in .s2p (single-ended) or .s4p (differential) touchstone files. When creating VP setups, use SetupA-SetupD for sources C1-C4, in order. Place the saved setup file in the VirtualProbe Path folder.

Advanced uses custom panel setups saved from a WebEditor processor to apply virtual probing to the acquired signals. When creating the processing web, output math functions F9-F12 for sources C1-C4, in order. Place the saved setup file in the VirtualProbe Path folder.

VP@Receiver Settings

These settings are applied when the Virtual Probe Tool Selection is VP@Receiver.

VP@Receiver Path

Full path to the location of the setup files for channels with VP@Receiver functions.

<channel> VP@Receiver Setup File Name

Enter the name of the setup file to be used when applying VP@Receiver to the respective channel, C1-C4. The setup file name should include the .lss extension.

VirtualProbe Settings

These settings are applied when the Virtual Probe Tool Selection is VirtualProbe or Advanced.

VirtualProbe Setup Path

Full path to the location the setup file.

VirtualProbe Setup File Name

Name of the setup file that will be used to generate all signals under test. The setup file name should include the .lss extension.

Advanced Settings

These variables are designed to give advanced users more control over the QualiPHY script.

Time Per Division for Acquisition

Enter the Time/div in exponential notation (e.g., 5e-3 for 5 ms/div).

Jitter BER Level

Enter the BER level used to calculate total and deterministic tJIT(per)/tJIT(cc) in SDA. This is set up as the power of 10. Default is -12.

Timing Reference Horizontal Shift

Override horizontal shift value that will shift all signals relative to the timing reference in DDR Debug Toolkit views. Enter value in seconds.

Custom Level Settings

Auto, Standard or Custom Levels

Select the type of levels to apply:

- Auto uses levels QualiPHY calculates from the top and base of the acquired waveform.
- Standard uses the levels defined by the JEDEC specification.
- Custom uses the VIH/VIL AC/DC levels defined by the custom level variables.

VDD and VDDQ Level

Enter a custom voltage level for VDD and VDDQ.

VOH(AC) Level for DQ, DQS(se)

Enter a custom voltage level for VOH(AC).

VOL(AC) Level for DQ, DQS(se)

Enter a custom voltage level for VOL(AC).

VREF.CA Level

Enter a custom voltage level for VREF.CA.

VREF.DQ Level for Writes (Inputs)

Enter a custom voltage level for VREF.DQ, Writes (Inputs).

AC Threshold

Select an AC threshold for DQ and single-ended DQS signals. This value sets the delta from VREF.DQ for many measurements.

Input DC Threshold

Enter a custom DC threshold voltage.

AC Threshold (CA)

Select an AC threshold for Control, Clock and Address signals. This value sets the delta from VREF.CA for many measurements.

High/Low Levels Delta

Used to assist with preamble identification, it sets thesholds at + and - the selected value in the DQS signal.

DQS Read/Write Threshold (%)

Enter the hysteresis threshold for DQS Read/Write signals. Value is the % of the DQS peak-peak voltage.

DDR5 Limit Sets

The limits in use by the DDR5 tests are defined in the JEDEC DDR5 specification, JESD79-5B. The software includes limit sets for:

DDR5-3200, DDR5-3600, DDR5-4000, DDR5-4400, DDR5-4800, DDR5-5200, DDR5-5600, DDR5-6000, DDR5-6400, DDR5-6800, DDR5-7200, DDR5-7600, DDR5-8000, DDR5-8400.

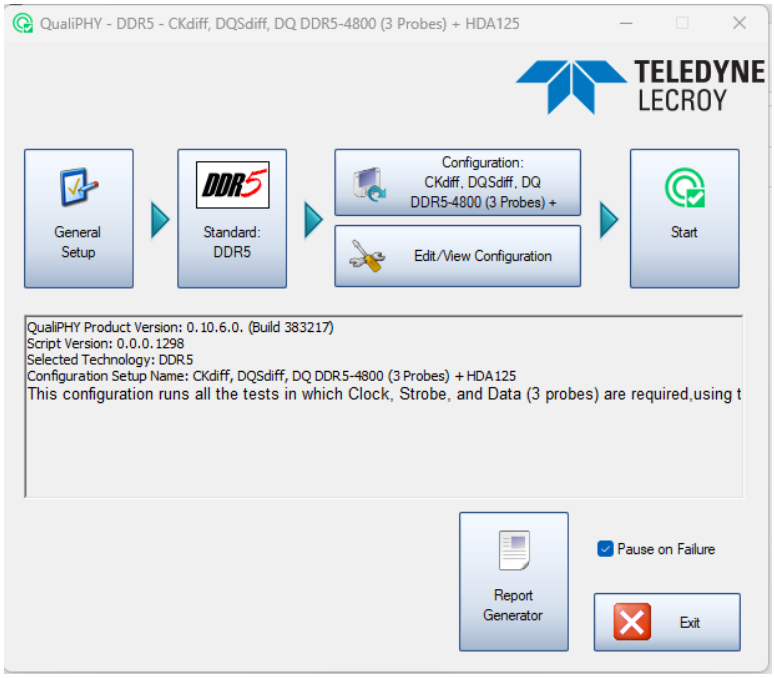
DDR5-4800 is used by default in the included configurations.

Using QualiPHY

This section provides an overview of the QualiPHY user interface and general procedures.

QualiPHY Test Process

1. Before beginning any test or data acquisition, warm the oscilloscope for at least 20 minutes and perform any other required set up.
2. Launch the QualiPHY wizard and select your **Standard**, then **Edit/View Configuration**.



3. Use the Setup and Variables tabs to make your individual test settings. Once you're happy with the all the settings, click **Save As.** Select your new **Configuration**, then click **Start**.
4. The connection diagrams and dialogs prompt you to connect the oscilloscope to the DUT. As you work, continue to follow the software prompts to confirm all signals are meeting the requirements for analysis.

   When all tests are successfully completed, both progress bars on the wizard dialog are completely green and the message "All tests completed successfully" appears.
5. If you have **Pause on Failure** checked, you'll be prompted to take action upon a failure. During this time, you may switch over to MAUI and use the DDR Debug Toolkit to analyze the failure.

   Once back to the QualiPHY wizard after a pause, choose to:

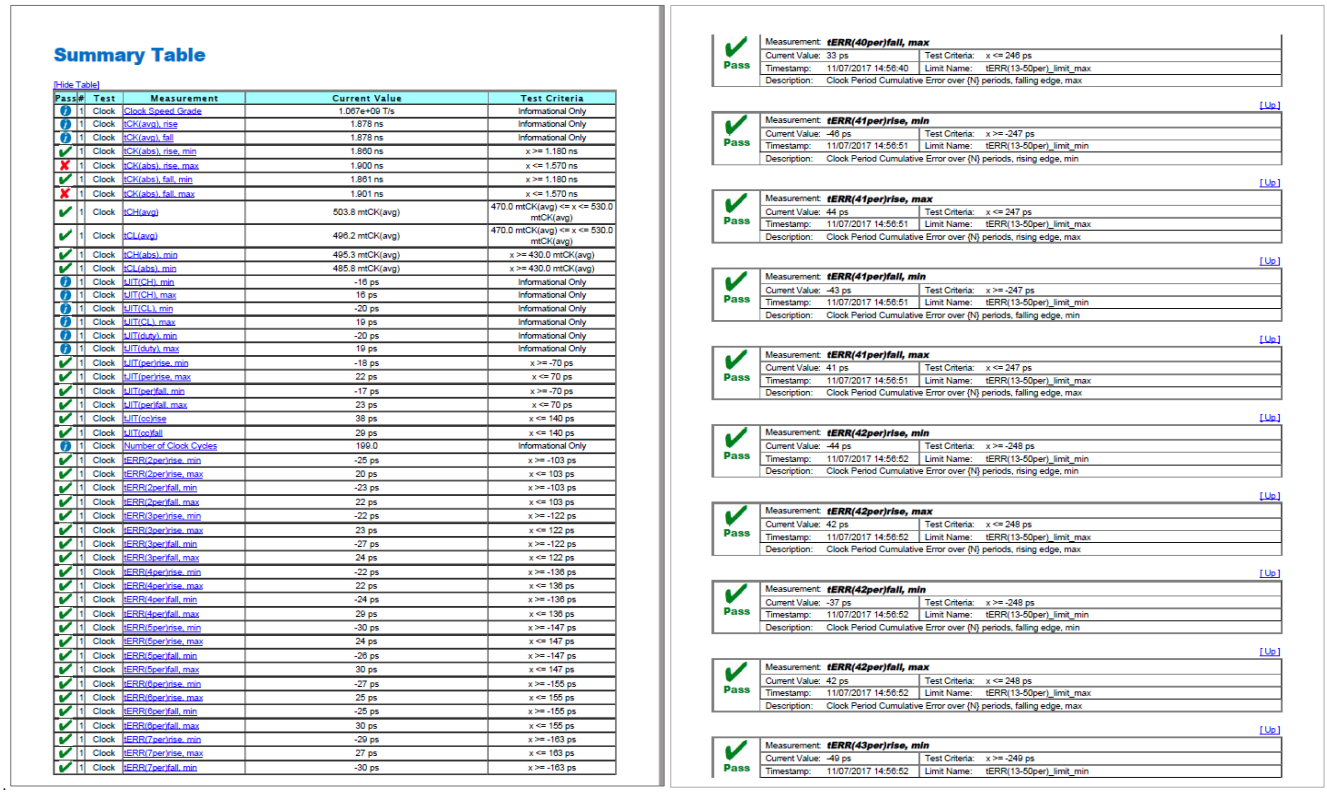
   - **Retry** the test from the latest established point defined in the script
   - **Ignore and Continue** with the next test
   - **Abort Session**

Generating Reports

The QualiPHY software automates report generation. On the wizard dialog, go to General Setup > Report to pre-configure reporting behavior. You can also manually launch the Report Generator from the wizard dialog after a test is completed.

The Report Generator offers the same selections as the Report tab, only applied to each report individually, rather than as a system setting. There are also options to link a custom style sheet (.xslt) to the report, or to Exclude Informative Results.

The Test Report includes a summary table with links to the detailed test result pages.



Summary Table

[Hide Table]

Pass	#	Test	Measurement	Current Value	Test Criteria
ℹ	1	Clock	Clock Speed Grade	1.067e+09 T/s	Informational Only
ℹ	1	Clock	tCK(avg), rise	1.878 ns	Informational Only
ℹ	1	Clock	tCK(avg), fall	1.878 ns	Informational Only
✔	1	Clock	tCK(abs), rise, min	1.860 ns	x >= 1.180 ns
✘	1	Clock	tCK(abs), rise, max	1.900 ns	x <= 1.570 ns
✔	1	Clock	tCK(abs), fall, min	1.861 ns	x >= 1.180 ns
✘	1	Clock	tCK(abs), fall, max	1.901 ns	x <= 1.570 ns
✔	1	Clock	tCK(avg)	503.8 mtCK(avg)	470.0 mtCK(avg) <= x <= 530.0 mtCK(avg)
✔	1	Clock	tCL(avg)	496.2 mtCK(avg)	470.0 mtCK(avg) <= x <= 530.0 mtCK(avg)
✔	1	Clock	tCH(abs), min	495.3 mtCK(avg)	x >= 430.0 mtCK(avg)
✔	1	Clock	tCL(abs), min	485.8 mtCK(avg)	x >= 430.0 mtCK(avg)
ℹ	1	Clock	UIT(CH), min	-16 ps	Informational Only
ℹ	1	Clock	UIT(CH), max	16 ps	Informational Only
ℹ	1	Clock	UIT(CL), min	-20 ps	Informational Only
ℹ	1	Clock	UIT(CL), max	19 ps	Informational Only
ℹ	1	Clock	UIT(duty), min	-20 ps	Informational Only
ℹ	1	Clock	UIT(duty), max	19 ps	Informational Only
✔	1	Clock	UIT(per)rise, min	-18 ps	x >= -70 ps
✔	1	Clock	UIT(per)rise, max	22 ps	x <= 70 ps
✔	1	Clock	UIT(per)fall, min	-17 ps	x >= -70 ps
✔	1	Clock	UIT(per)fall, max	23 ps	x <= 70 ps
✔	1	Clock	UIT(cc)rise	38 ps	x <= 140 ps
✔	1	Clock	UIT(cc)fall	29 ps	x <= 140 ps
ℹ	1	Clock	Number of Clock Cycles	199.0	Informational Only
✔	1	Clock	tERR(2per)rise, min	-25 ps	x >= -103 ps
✔	1	Clock	tERR(2per)rise, max	20 ps	x <= 103 ps
✔	1	Clock	tERR(2per)fall, min	-23 ps	x >= -103 ps
✔	1	Clock	tERR(2per)fall, max	22 ps	x <= 103 ps
✔	1	Clock	tERR(3per)rise, min	-22 ps	x >= -122 ps
✔	1	Clock	tERR(3per)rise, max	23 ps	x <= 122 ps
✔	1	Clock	tERR(3per)fall, min	-27 ps	x >= -122 ps
✔	1	Clock	tERR(3per)fall, max	24 ps	x <= 122 ps
✔	1	Clock	tERR(4per)rise, min	-22 ps	x >= -136 ps
✔	1	Clock	tERR(4per)rise, max	22 ps	x <= 136 ps
✔	1	Clock	tERR(4per)fall, min	-24 ps	x >= -136 ps
✔	1	Clock	tERR(4per)fall, max	29 ps	x <= 136 ps
✔	1	Clock	tERR(5per)rise, min	-30 ps	x >= -147 ps
✔	1	Clock	tERR(5per)rise, max	24 ps	x <= 147 ps
✔	1	Clock	tERR(5per)fall, min	-26 ps	x >= -147 ps
✔	1	Clock	tERR(5per)fall, max	30 ps	x <= 147 ps
✔	1	Clock	tERR(6per)rise, min	-27 ps	x >= -155 ps
✔	1	Clock	tERR(6per)rise, max	25 ps	x <= 155 ps
✔	1	Clock	tERR(6per)fall, min	-25 ps	x >= -155 ps
✔	1	Clock	tERR(6per)fall, max	30 ps	x <= 155 ps
✔	1	Clock	tERR(7per)rise, min	-29 ps	x >= -163 ps
✔	1	Clock	tERR(7per)rise, max	27 ps	x <= 163 ps
✔	1	Clock	tERR(7per)fall, min	-30 ps	x >= -163 ps

Pass — Measurement: **tERR(40per)fall, max** — Current Value: 33 ps — Test Criteria: x <= 246 ps — Timestamp: 11/07/2017 14:56:40 — Limit Name: tERR(13-50per)_limit_max — Description: Clock Period Cumulative Error over {N} periods, falling edge, max

[Up]

Pass — Measurement: **tERR(41per)rise, min** — Current Value: -46 ps — Test Criteria: x >= -247 ps — Timestamp: 11/07/2017 14:56:51 — Limit Name: tERR(13-50per)_limit_min — Description: Clock Period Cumulative Error over {N} periods, rising edge, min

[Up]

Pass — Measurement: **tERR(41per)rise, max** — Current Value: 44 ps — Test Criteria: x <= 247 ps — Timestamp: 11/07/2017 14:56:51 — Limit Name: tERR(13-50per)_limit_max — Description: Clock Period Cumulative Error over {N} periods, rising edge, max

[Up]

Pass — Measurement: **tERR(41per)fall, min** — Current Value: -43 ps — Test Criteria: x >= -247 ps — Timestamp: 11/07/2017 14:56:51 — Limit Name: tERR(13-50per)_limit_min — Description: Clock Period Cumulative Error over {N} periods, falling edge, min

[Up]

Pass — Measurement: **tERR(41per)fall, max** — Current Value: 41 ps — Test Criteria: x <= 247 ps — Timestamp: 11/07/2017 14:56:51 — Limit Name: tERR(13-50per)_limit_max — Description: Clock Period Cumulative Error over {N} periods, falling edge, max

[Up]

Pass — Measurement: **tERR(42per)rise, min** — Current Value: -44 ps — Test Criteria: x >= -248 ps — Timestamp: 11/07/2017 14:56:52 — Limit Name: tERR(13-50per)_limit_min — Description: Clock Period Cumulative Error over {N} periods, rising edge, min

[Up]

Pass — Measurement: **tERR(42per)rise, max** — Current Value: 42 ps — Test Criteria: x <= 248 ps — Timestamp: 11/07/2017 14:56:52 — Limit Name: tERR(13-50per)_limit_max — Description: Clock Period Cumulative Error over {N} periods, rising edge, max

[Up]

Pass — Measurement: **tERR(42per)fall, min** — Current Value: -37 ps — Test Criteria: x >= -248 ps — Timestamp: 11/07/2017 14:56:52 — Limit Name: tERR(13-50per)_limit_min — Description: Clock Period Cumulative Error over {N} periods, falling edge, min

[Up]

Pass — Measurement: **tERR(42per)fall, max** — Current Value: 42 ps — Test Criteria: x <= 248 ps — Timestamp: 11/07/2017 14:56:52 — Limit Name: tERR(13-50per)_limit_max — Description: Clock Period Cumulative Error over {N} periods, falling edge, max

[Up]

Pass — Measurement: **tERR(43per)rise, min** — Current Value: -49 ps — Test Criteria: x >= -249 ps — Timestamp: 11/07/2017 14:56:52 — Limit Name: tERR(13-50per)_limit_min

Figure 22. QualiPHY report Summary table and details.

Reports are output to the folder D:\QPHY\Reports, or else C:\LeCroy\QPHY\Reports if QualiPHY is installed on a remote PC.

You can add your own logo to the report by replacing the file *\QPHY\StyleSheets\CustomerLogo.jpg.

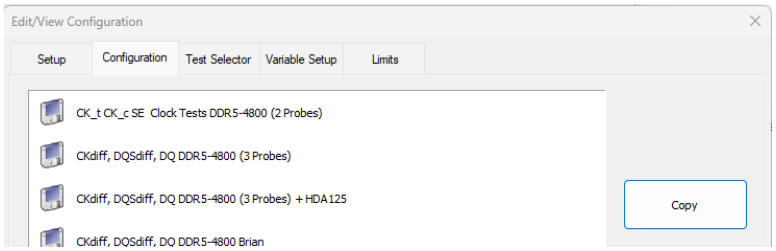
The recommended maximum size is 250x100 pixels at 72 ppi, 16.7 million colors, 24 bits. Use the same file name and format.

Customizing QualiPHY

The pre-loaded configurations cannot be modified. However, you can create your own test configurations by copying one of the pre-loaded configurations and modifying it.

Copy Configuration

1. Access the QualiPHY wizard dialog and select a **Standard**.
2. Click **Edit/View Configuration** and select the configuration upon which to base the new configuration. This can be a pre-loaded configuration or another copy.
3. Click **Copy** and enter a name and description. Once a custom configuration is defined, it appears on the Configuration tab followed by "(Copy)."

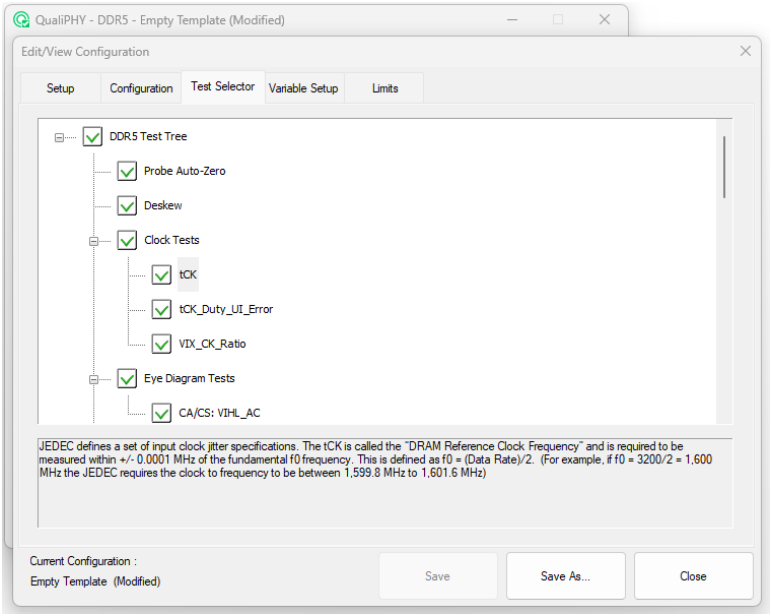


4. Select the new, custom configuration and follow the procedures below to continue making changes.

Note: If any part of a configuration is changed, the Save As button becomes active on the bottom of the dialog. If a custom configuration is changed, the Save button will also become active to apply the changes to the existing configuration, rather than create a new one.

Select Tests

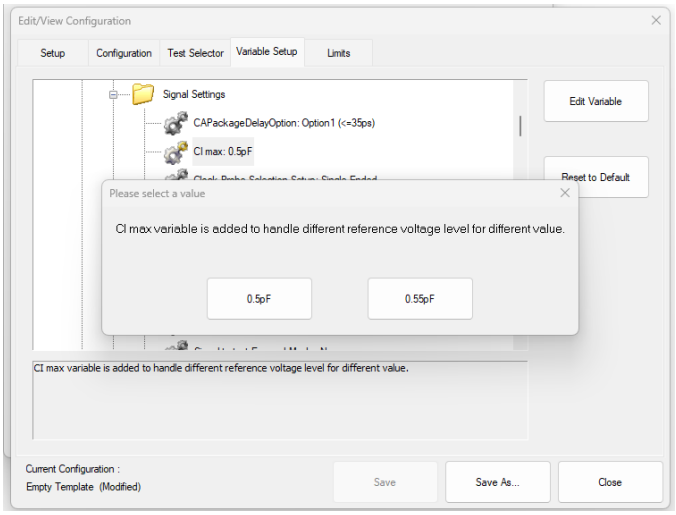
On the **Test Selector** tab, check the tests that make up the configuration. Each test is defined by the JEDEC standard. A description of each test is displayed when it is selected.



Edit Variables

The Variable Setup tab contains a list of test variables. To modify a variable:

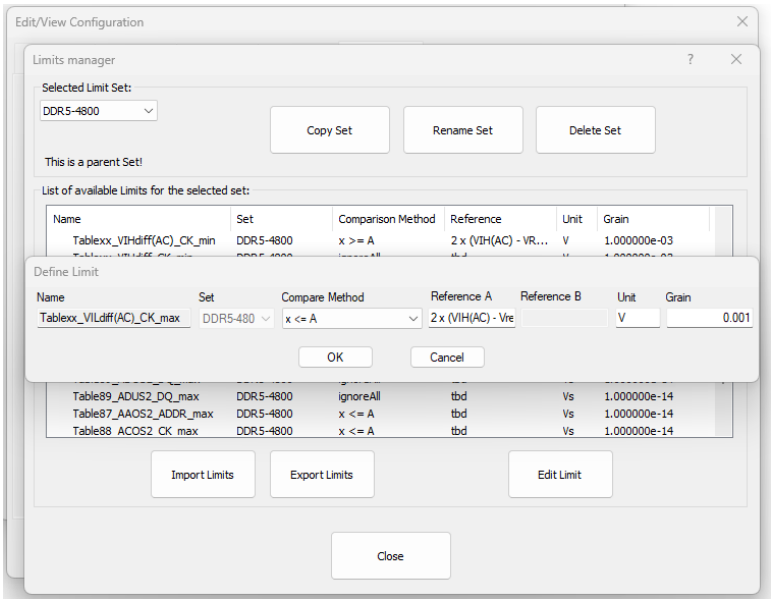
1. Select the variable on the Variable Setup tab, then click **Edit Variable**. (You can also choose to Reset to Default at any time.)
2. The conditions of this variable appear on a pop-up. Select or enter the new condition to apply.



Edit Test Limits

The Limits Manager shows the settings for every test limit in a limit set. Those in the default set are the limits defined by the standard. To create a custom limit set:

1. On the Limits tab, click **Limits Manager**.
2. With the default set selected, click **Copy Set** and enter a name for the new limit set.
3. Double click the limit to be modified, and in the pop-up enter the new values.



You can also Import Limits from a .csv file. Navigate to the file location after clicking the **Import Limits** button.

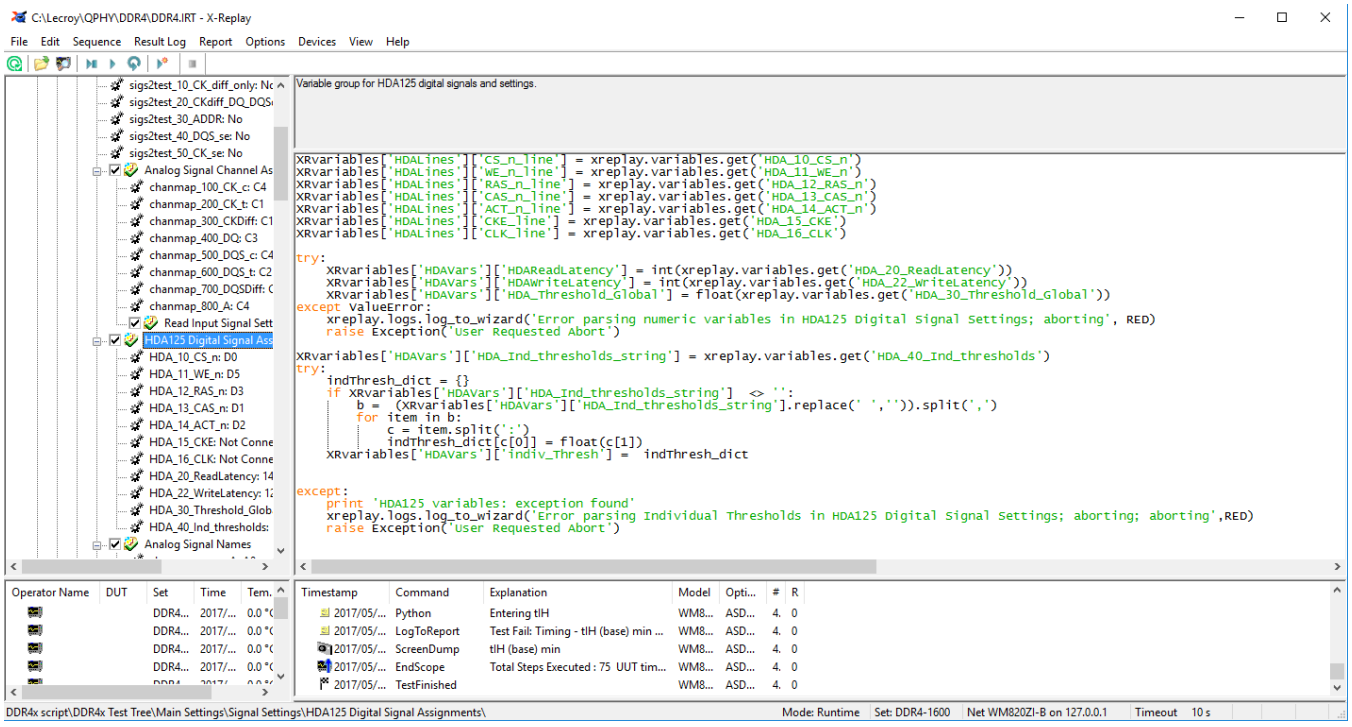
Tip: Likewise, Export Limits creates a .csv file from the current limit set. You may wish to do this and copy it to format the input .csv file.

X-Replay Mode

The X-Replay mode window is an advanced (“developer”) view of QualiPHY. The tree in the upper-left frame enables you to navigate to processes in the test script, in case you need to review the code, which appears in the upper-right frame.

Two other particularly useful features are:

- A list of recent test sessions in the lower-left frame. While you can only generate a report of the current test session in the QualiPHY wizard, in X-Replay Mode you can generate a report for any of these recent sessions. Right-click on the session and choose Create Report from context menu.
- The QualiPHY log in the bottom-right frame. The frame can be split by dragging up the lower edge. The bottom half of this split frame now shows the raw Python output, which can be useful if ever the script needs debugging.



Appendix A: Virtual Probing Set Up and Dependencies

Because the JEDEC electrical specifications are defined at the balls of the DDR DRAM, it is often necessary to use the virtual probing capabilities of the oscilloscope to get the best representations of the signals to be analyzed with DDR Debug Toolkit.

Also, if DDR Debug Toolkit and QPHY-DDR* are used together on the same device, it is good practice to ensure your DDR Debug virtual probing setup can also be used when you perform compliance testing using QualiPHY. QualiPHY has specific requirements for virtual probing that you will want to observe in the setup files you save and the selections you make in DDR Debug Toolkit.

The virtual probing capabilities described here become available with the installation of the SDAIII-CompleteLinQ or VirtualProbe software options.

Virtual Probing Methods

There are three methods for using virtual probing in DDR Debug Toolkit:

Method 1–Apply the VirtualProbe@Rcvr math processor to the input signals, then use the resulting math functions as inputs for DDR Debug. This math processor will apply the termination network parameters to the acquired signals.

Method 2–Use Virtual Probe software to apply S-parameter models to the input signals, then use the resulting VPOut* waveforms as inputs for DDR Debug. This method is good for using .s2p and .s4p files to deembed effects.

Method 3–Use WebEditor to apply the VirtualProbe math processor to the input signals, then use the resulting math functions as inputs for DDR Debug. This is an advanced approach that may be used to represent more complex S-parameters, such as interposer models.

Method 1–VirtualProbe@Rcvr Math Functions

The VirtualProbe@Rcvr math processor is recommended if the difference between the signal being probed and the desired signal can be defined as a simple RLC termination model with some transmission line delay, as shown in the following figure. Here, the probe point is the input (In) of the termination model and the desired signal is the output (Out) of the model.

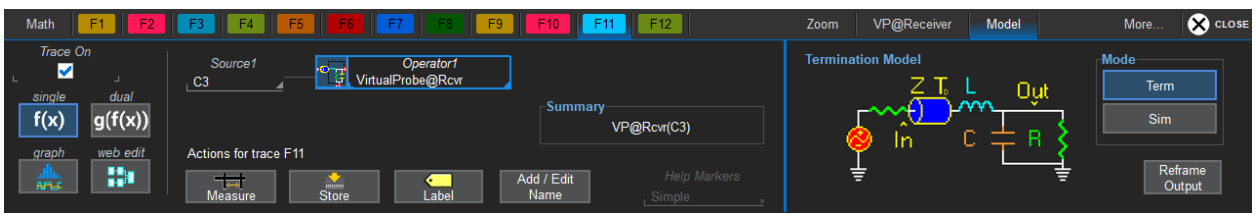
Create Math Functions

For each signal that you will analyze in DDR Debug Toolkit, apply the VirtualProbe@Rcv math processor to the acquired signals. For interoperability of DDR Debug Toolkit and QualiPHY, best practice is to use:

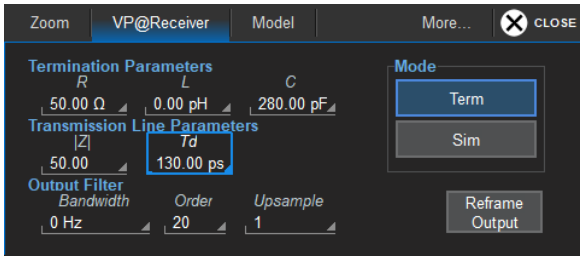
- CLK on C1 = source for F9
- DQS on C2 = source for F10
- DQ on C3 = source for F11
- Other (e.g., ADDR) on C4 = source for F12

For example, to apply the VirtualProbe@Rcv math function to DQ on C3:

1. Open the oscilloscope F11 setup dialog and choose C3 as Source1 and VirtualProbe@Rcvr as Operator1. On the Model subdialog, choose Term(ination) mode.



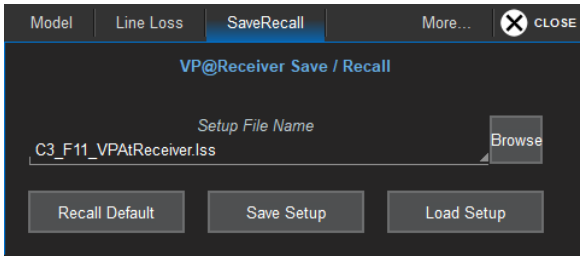
2. Open the VP@Receiver subdialog and input the termination network parameters:



For more information on using the VirtualProbe@Rcvr math processor, see the white paper.

Using the Virtual Probe at Receiver Math Operator to Eliminate Reflections

3. As you create each math function, go to the SaveRecall subdialog and Save Setup to an .lss file for each input signal.



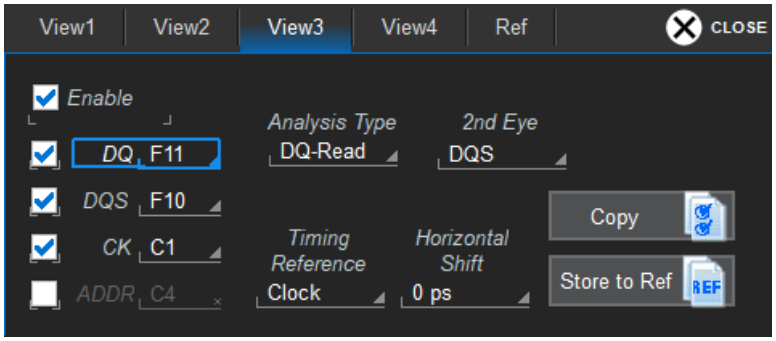
Tip: It will be easier to select files in QualiPHY if you include the input channel in the filename, for example, C3_F11_VPAtReceiver.lss.

4. Copy all files to an oscilloscope folder that QualiPHY can access. The default is D:\Applications\VPAtReceiver.

Configure DDR Debug Toolkit

When setting up your DDR Debug Toolkit Views, select the VirtualProbe@Rcvr math functions you created as the inputs for the signals, rather than the channels.

In this example, DQ is probed on C3 and DQS is probed on C2 of the oscilloscope. F11 and F10 are the VirtualProbe@Rcv math functions that were applied to the probed signals, respectively.

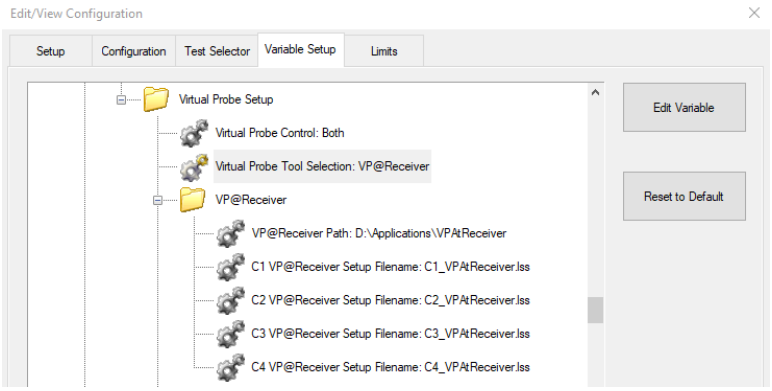


Using VirtualProbe@Rcvr with QualiPHY

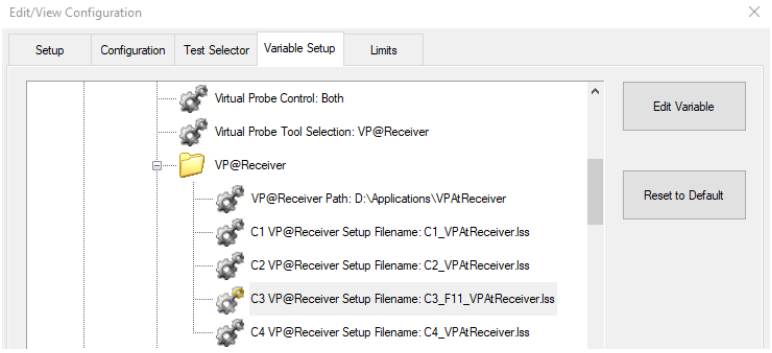
QualiPHY expects specific math functions to represent specific inputs when using the VirtualProbe@Rcvr method. When creating your math functions, use:

- C1 = Source for F9
- C2 = Source for F10
- C3 = Source for F11
- C4 = Source for F12

1. On the QualiPHY wizard, after selecting the configuration to use, choose View/Edit Configuration, then open the Variable Setup tab and:
2. Turn “Virtual Probe Control” to “Read”, “Write” or “Both” types of bursts (it is Off by default)
3. Choose “VP@Receiver” as the “Virtual Probe Tool Selection”:



4. In the VP@Receiver variable group, change:
   - "VP@Receiver Path" to the folder containing the saved setup files
   - "C*n* VP@Receiver Setup File" to the names of the files representing compensated input channels



Note: You will need to save these changes to a new configuration, which will then be ready for selection whenever you wish to apply VirtualProbe@Rcvr to this setup.

Method 2–Virtual Probe Software

The Virtual Probe method can be used if the difference between the signal being probed and the desired signal can be defined by one or more S-parameter touchstone files (.s2p for single-ended and .s4p for differential).

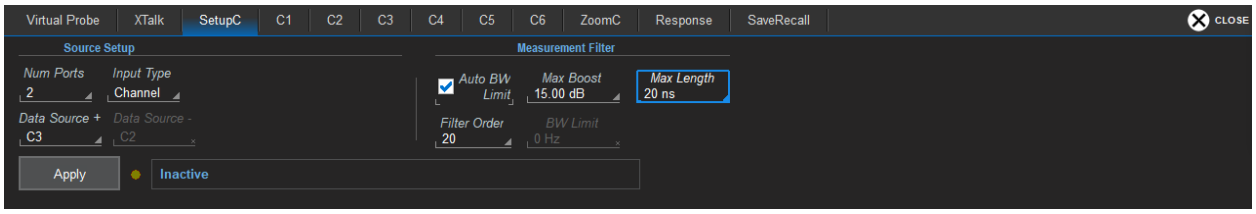
Configure Virtual Probe Setups

In the Virtual Probe software, S-parameters can be used to define multiple stages of the input/output signal flow. For interoperability of DDR Debug Toolkit and QualiPHY, best practice is to use:

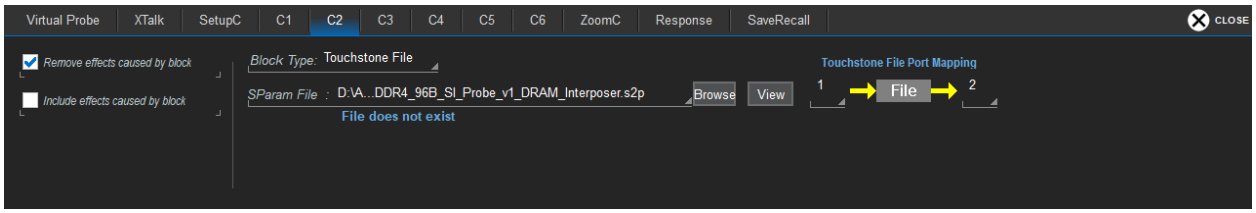
- CLK on C1 = source for SetupA
- DQS on C2 = source for SetupB
- DQ on C3 = source for SetupC
- Other (e.g., ADDR) on C4= source for SetupD

For example, to apply Virtual Probe Setup C to the DQ signal on C3:

1. Open the SetupC dialog and choose C3 as the Data Source.

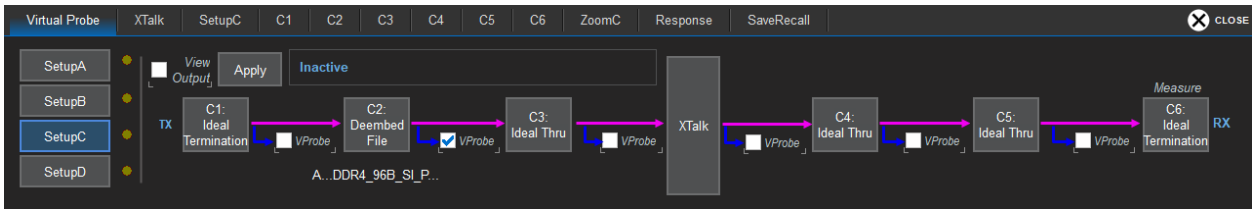


2. On the C2 dialog (or at whichever block of the circuit you wish to deembed), select "Remove effects caused by Clock" and import the .s2p file representing the fixture you want deembedded (here, the interposer):

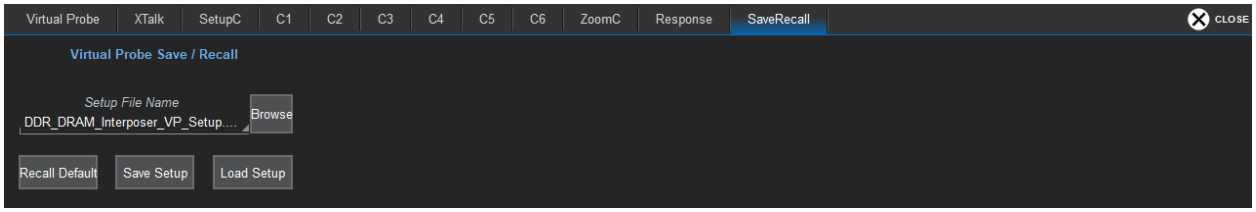


Note: In this example, C2 has nothing to do with the signal input channel, but represents the order of processing in the Virtual Probe "circuit". Setups A, B and D have similar blocks A2, B2 and D2.

3. On the Virtual Probe dialog, select block C2 (Deembed File):



4. Do the same for the other inputs that require virtual probing, following the conventions as to which Virtual Probe Setup to use for which input.
5. Open the SaveRecall dialog and save the Virtual Probe setup to an .lss file in an oscilloscope folder that QualiPHY can access. The default folder is oscilloscope D:\Applications\VirtualProbe.

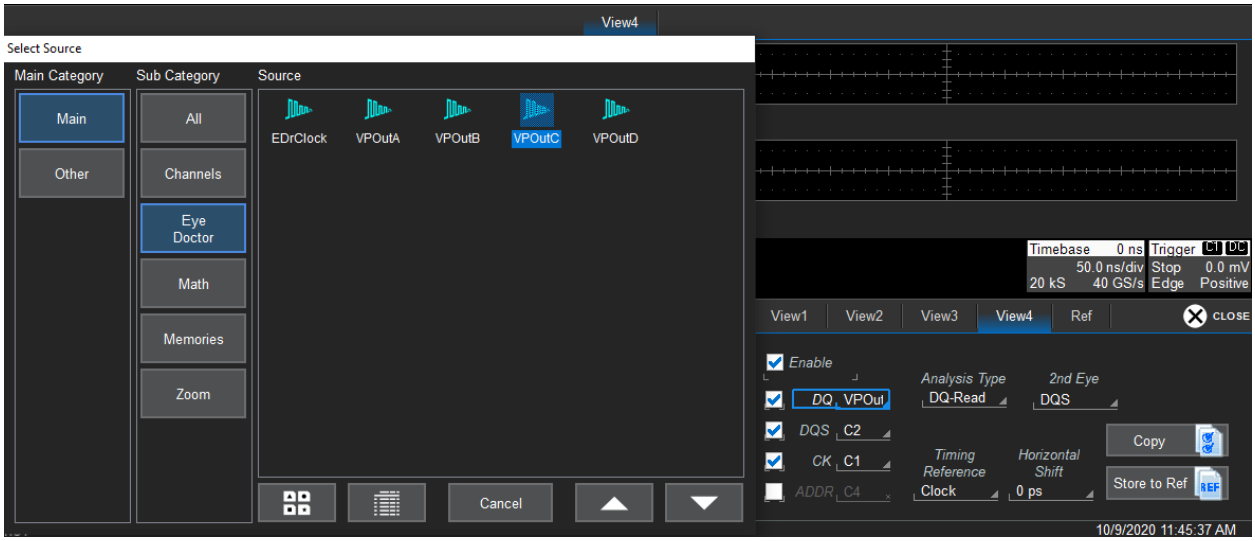


Note: With this method, there is only one setup file, vs.. four setup files for the VirtualProbe@Rcvr method.

Configure DDR Debug Toolkit

Select the VPOut* waveforms corresponding to each Virtual Probe Setup you created as the inputs for DDR Debug Toolkit views. Setup A will output VPOutA, and so forth.

In the example below, the DQ signal with the interposer deembedded is represented by VPOutC, so that waveform is selected as the DQ input in DDR Debug Toolkit, rather than the probed input C3:



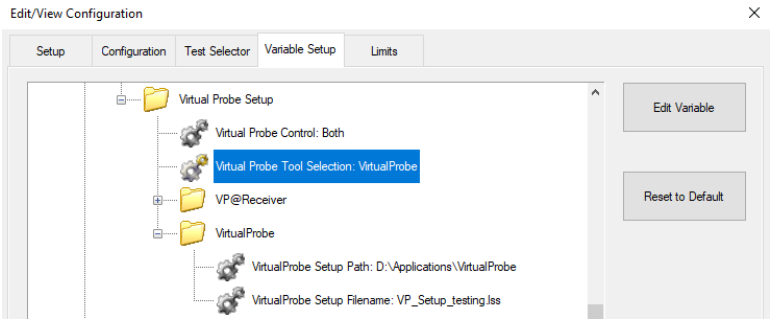
Note: VPOut* waveforms are in the Eye Doctor selector menu.

When Using Virtual Probe with QualiPHY

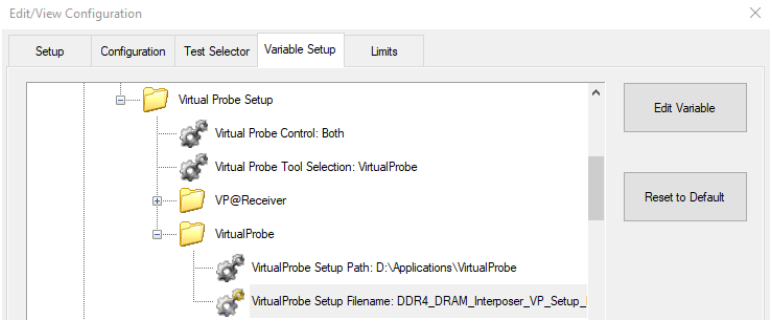
The Virtual Probe setups should correspond to the oscilloscope input channels as follows:

- C1 = Source for SetupA (VPOutA)
- C2 = Source for SetupB (VPOutB)
- C3 = Source for SetupC (VPOutC)
- C4 = Source for SetupD (VPOutD)

1. On the QualiPHY wizard, after selecting the configuration to use, choose View/Edit Configuration, then open the Variable Setup tab and:
2. Turn “Virtual Probe Control” to “Read”, “Write” or “Both” types of bursts (it is Off by default)
3. Choose “VirtualProbe” as the “Virtual Probe Tool Selection”:



4. In the VirtualProbe variable group, change:
   - “VirtualProbe Setup Path” to the full path to your setup file folder
   - “VirtualProbe Setup Filename” to the saved .lss file



Note: You will need to save these changes to a new configuration, which will then be ready for selection whenever you wish to apply Virtual Probe to this setup.

Method 3–WebEditor

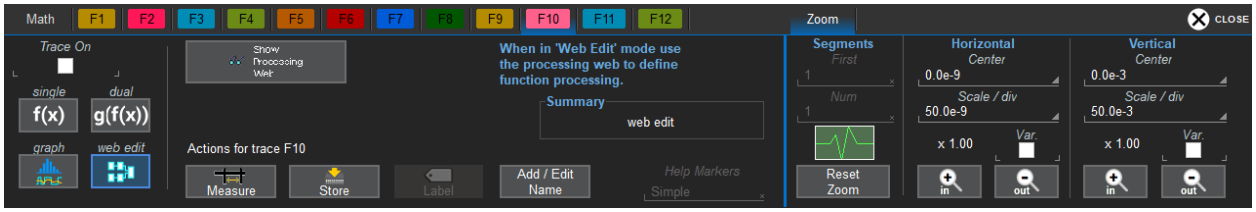
Some interposers use more sophisticated S-parameters than the 2- or 4-port models, such as .s3p and .s6p. For these cases, the netlist of the interposer can be defined using the oscilloscope WebEditor tool. The WebEditor will output math functions corresponding to the compensated channels, which will be used as inputs in DDR Debug Toolkit, similar to the VirtualProbe@Rcvr method. For interoperability of DDR Debug Toolkit and QualiPHY, best practice is to use:

- CLK on C1 = source for F9
- DQS on C2 = source for F10
- DQ on C3 = source for F11
- Other (e.g., ADDR) on C4 = source for F12

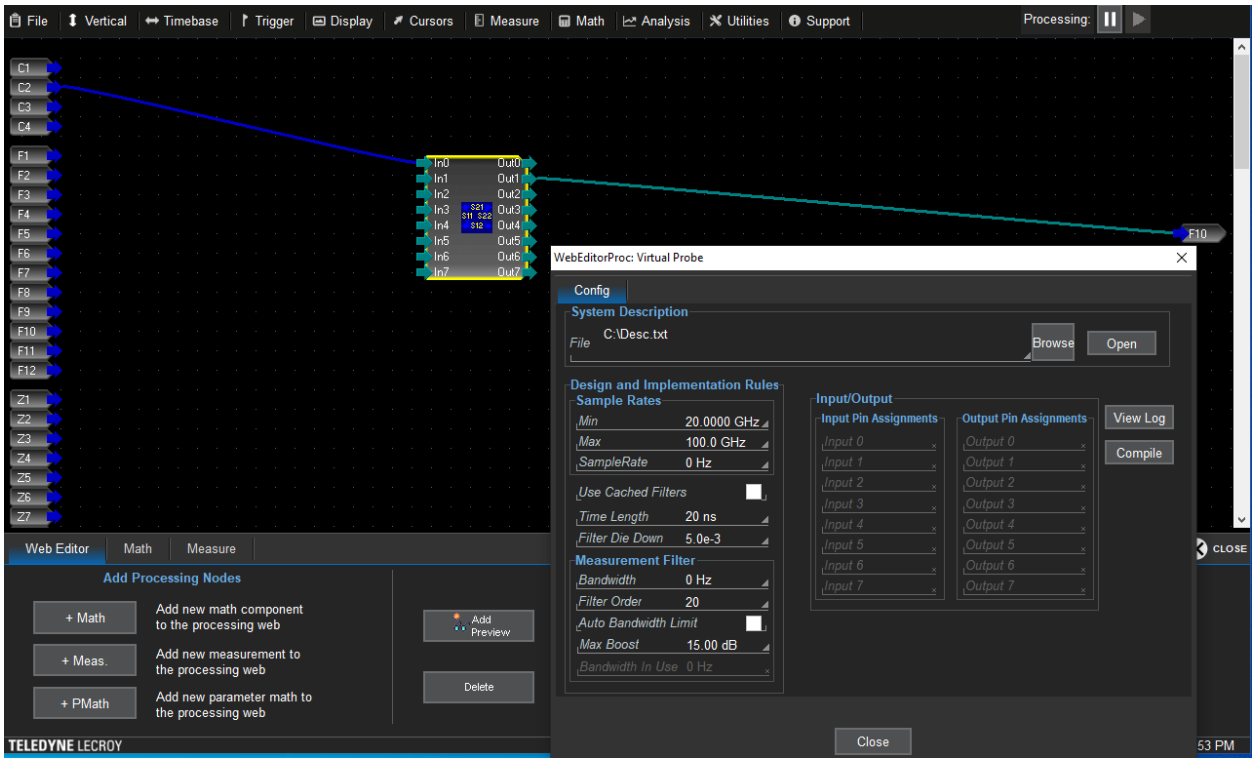
Define Netlist in WebEditor

In this example, the probed DQS and DQ signals are input on C2 and C3. These inputs will undergo the processing web to deembed the interposer from the signal.

1. To begin, open the F10 dialog and select web edit, then Show Processing Web.



This will take you to a screen like that below where you create a processing web that inputs C2 and C3, passes them through the VirtualProbe math processor, and outputs F10 and F11. The VirtualProbe processor allows you to configure the characteristics of the interposer, including applying signal filters and manually mapping input to output pins.



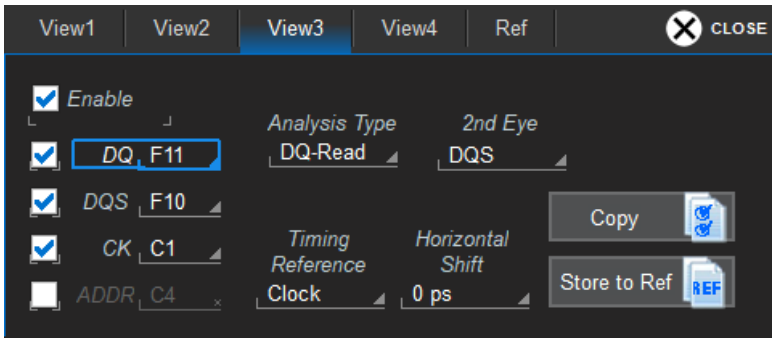
2. Do the same for C3-F11 and other inputs that require virtual probing, following the conventions below as to which math functions to use for which channels. Both F10 and F11, and any other math functions needed, can be placed on the same processing web.
3. Save the configuration to an .lss file in an oscilloscope folder where QualiPHY can access it.

Note: With this method, there is only one setup file, vs.. the four setup files for VirtualProbe@Rcvr math functions.

Contact Teledyne LeCroy support for more information about creating and saving your processing web.

Configure DDR Debug Toolkit

Choose the math functions resulting from the processing web as the inputs for the DDR Debug Toolkit views:

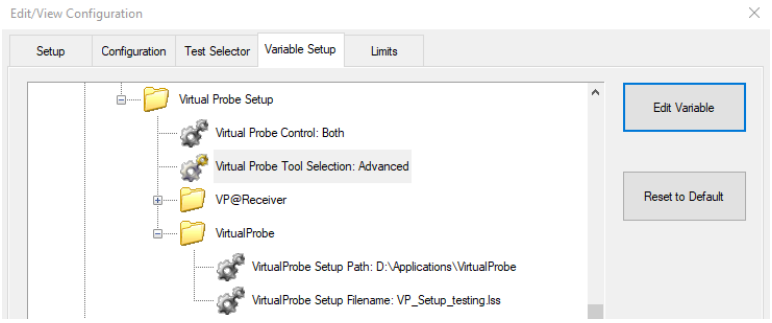


Using WebEditor with QualiPHY

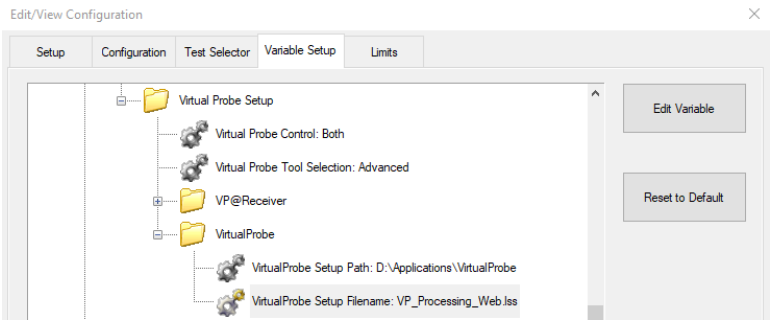
The math functions output by the WebEditor processing web should correspond to the following oscilloscope input channels:

- C1 = Source for F9
- C2 = Source for F10
- C3 = Source for F11
- C4 = Source for F12

1. On the QualiPHY wizard, after selecting the configuration to use, choose View/Edit Configuration, then open the Variable Setup tab and:
2. Turn “Virtual Probe Control” to “Read”, “Write” or “Both” types of bursts (it is Off by default)
3. Choose “Advanced” as the “Virtual Probe Tool Selection”:



4. In the Virtual Probe variable group, change:
   - “VirtualProbe Setup Path” to the full path to your setup file folder
   - “VirtualProbe Setup Filename” to the saved .lss file.



Note: You will need to save these changes to a new configuration, which will then be ready for selection whenever you wish to apply the processing web to this setup.

Appendix B: File Name Conventions for Saved Waveforms

QPHY-DDR5-SYS saves the waveforms from each acquisition using a specific file name convention. This specific waveform name definition must be used in order to re-run any acquisition to recreate specific test results.

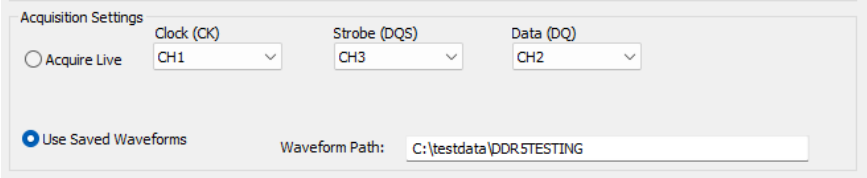
The waveform naming convention is: <Channel> <Probe Setup> <Analog Signal Name> <File Index>

Here are examples of working waveform names loaded by QualiPHY when choosing to *Use Saved Waveforms*:

- C1_CKDQ0DQS3_CK_00014.trc
- C2_CKDQ0DQS3_DQ0 _00014.trc
- C3_CKDQ0DQS3_DQS3_00014.trc

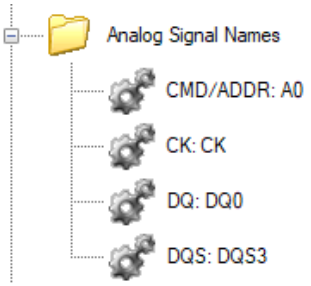
<Channel> (example: C2): This is the input channel used to acquire the signal. In this case C2 was used. This portion of the name must match the <Signal> Input Channel variable. Possible values: C1, C2, C3, C4.

Note: The channel setup must match the file name. In the above example C1=CK, C2=DQ, C3=DQS.



<Probe Setup> (example: CKDQ0DQS3): This is the probe setup used during the acquisition. This will change depending on whether there are 1, 2, 3 or 4 signals being analyzed.

<Analog Signal Name> (example: DQS3): This is the signal name for this trace as it was set using the Analog Signal Name variable tab. The waveform must match the Signal Name variable. Possible values: DQ0-63, DQS0-15.



<File Index> (example: 00014): This is the file number. Each new acquisition saved typically adds to this count and QPHY will automatically increment this by one on each run. When running in Use Saved Waveforms, the recalled Waveform File Index variable. Possible values: Any five-digit number.

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