TELEDYNE LECROY
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QPHY-DDR4

DDR4, LPDDR4 and LPDDR4X
Serial Data Compliance Software

Instruction Manual

November, 2023

Relating to:

MAUI® version 10.5.x.x and later

QualiPHY® version 10.5.x.x and later

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About This Manual

This manual assumes that you are familiar with using an oscilloscope, in particular the Teledyne LeCroy oscilloscope that will be used with QualiPHY and that you have purchased the QPHY-DDR4 software option.

Some of the images in this manual may show QualiPHY products other than QPHY-DDR4, or were captured using different model oscilloscopes, as they are meant to illustrate general concepts only. Rest assured that while the user interface may look different from yours, the functionality is identical.

Introduction

QualiPHY is highly automated compliance test software meant to help you develop and validate the PHY (physical-electrical) layer of a device, in accordance with the official documents published by the applicable standards organizations and special interest groups (SIGs). You can additionally set custom variables and limits to test compliance to internal standards.

QualiPHY is composed of a "wizard" application that enables the configuration and control of separate tests for each standard through a common user interface. Features include:

- **User-Defined Test Limits** to ensure devices are well within the passing region, even if subsequently measured with different equipment.
- **Flexible Test Results Reporting** that includes XML Test Record generation to better understand device performance distribution or obtain process related information from the devices under test.

QPHY-DDR4 is an automated test package performing all the real-time oscilloscope tests for DDR4 and LPDDR4/4X designs in accordance with JEDEC Standard No. JESD79-4D and JESD209-4-1A. These standards are available from jedec.org.

Conventions

This manual follows these documentation conventions:

- The terms "application" and "software" without any other identifier refer to the QualiPHY DDR4 software option.
- The term "DUT" is an abbreviation for Device Under Test.
- The term "select" is a generic term referring to any method for activating a software control, either using a pointing device or a touch screen.
- The term "Note:" identifies important information.

Technical Support

Live Support

Registered users can contact their local Teledyne LeCroy service center at the number listed on our website. You can also submit Technical Support requests via the website at:

teledynelecroy.com/support/techhelp

Resources

Teledyne LeCroy publishes a free Technical Library on its website. Manuals, tutorials, application notes, white papers, and videos are available to help you get the most out of your Teledyne LeCroy products. Visit:

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Software Installation and Setup

QualiPHY is a Windows-based application that can be configured with one or more serial data compliance components. Each compliance component is purchased as a software option.

Oscilloscope Requirements

Hardware

The software requires an oscilloscope with at least 13 GHz of bandwidth.

A 13 GHz WaveMaster/SDA 8Zi-B or higher performance oscilloscope is recommended for all speeds of DDR4/LPDDR4/4x testing.

In some cases, at lower memory transfer speeds, 8 GHz bandwidth may be sufficient. Verify the needed slewrates and harmonics will be satisfactory with your chosen oscilloscope bandwidth.

While not required, we recommend for convenience running QualiPHY on an oscilloscope equipped with an additional monitor. This allows the waveforms and measurements to be shown on the oscilloscope display, while the QualiPHY application is displayed on the attached monitor.

See the oscilloscope *Operator's Manual* for instructions on setting up dual monitor display.

See the DDR4/LPDDR4 Testing section for other required test hardware.

Software

For the software as shown here, the oscilloscope must be installed with:

- MAUI version 10.5.x.x minimum* with an activated QPHY-DDR4 option key
- QualiPHY version 10.5.x.x minimum* with an activated QPHY-DDR4 component

  Note: The versions listed above are the minimum versions required for the product as shown here. MAUI and QualiPHY software versions must match to the second point, so upgrade your version of QualilPHY if you have upgraded your oscilloscope firmware. The QualiPHY software may be installed on a remote PC, but all other software must be run on the oscilloscope.
- SDAIII, SDAIII-CompleteLinQ, SDA Expert-NRZ or SDA Expert Complete

  Note: SDAIII is standard on SDA 8Zi-B model oscilloscopes; you do not need an additional installation.
- Optional, but highly recommended: VirtualProbe software (for fixing reflections, termination, probe points, de-embedding, etc.)

  Note: VirtualProbe is included with SDAIII-CompleteLinq and SDA Expert Complete.

Update Oscilloscope Firmware

We recommend updating your Windows OS with the latest security patches before installing our software.

Download the latest version of the MAUI firmware from:

teledynelecroy.com/support/softwaredownload/ under Oscilloscope Downloads > Software Utilities

Follow the instructions included with the download to install it.

Install QualiPHY Application

Download the latest version of the QualiPHY software from:

teledynelecroy.com/support/softwaredownload/ under Oscilloscope Downloads > Software Utilities

The application can be installed on either the test oscilloscope or on a remote host computer. For remote execution, see Set Up Remote Control.

If the oscilloscope is not connected to the Internet, copy the installer onto a USB memory stick then transfer it to the oscilloscope desktop or a folder on the D:\ drive to execute it.

Run **QualiPHYInstaller.exe** and follow the installer prompts. Choose all the components you plan to activate. If you omit any components now, you will need to update the installation to activate them later.

By default, the oscilloscope appears as local host when QualiPHY is executed on the oscilloscope. Follow the steps under Add Oscilloscope Connection to QualiPHY to check that the IP address is 127.0.0.1.

Activate QualiPHY Components in MAUI

The serial data compliance components are factory installed as part of the oscilloscope application (MAUI) and are individually activated through the use of an alphanumeric code uniquely matched to the oscilloscope's serial number. This option key code is what is delivered when purchasing a software option.

To activate a component on the oscilloscope:

1. From the menu bar, choose Utilities > Utilities Setup.
2. On the Options tab, click Add Key.
3. Use the Virtual Keyboard to Enter Option Key, then click OK.

   If activation is successful, the key code now appears in the list of Installed Option Keys.
4. Restart the application by choosing File > Exit, then double-clicking the Start DSO icon on the desktop.

Activate Other Teledyne LeCroy Software

If newly purchased, activate any other required Teledyne LeCroy software options, such as SDAIII-CompleteLinq. The software is included with the latest firmware, you need only install your option key using the procedure above to activate it.

Set Up Remote Control (optional)

Usually, the oscilloscope is the host computer for the QualiPHY software, and all models that meet the acquisition requirements will also meet the host system requirements. However, the QualiPHY software can be executed from a remote host computer.

To run QualiPHY remotely:

- The oscilloscope must be connected to a LAN and assigned an IP address (fixed or dynamic).
- The host computer must be on the same LAN as the oscilloscope.

Remote Host Computer Requirements

If you wish to run the QualiPHY software from a remote computer, these minimum requirements apply:

- Windows 10 Professional operating system (Windows 11 not currently supported)
- 1 GHz or faster processor
- 1 GB (32-bit) or 2 GB (64-bit) of RAM
- Ethernet (LAN) network capability
- Hard Drive:
  - At least 100 MB free to install the wizard application
  - Up to 2 GB per standard installed to store the log database (each database grows from a few MB to a maximum of 2 GB)

Configure Oscilloscope for Remote Control

1. From the oscilloscope menu bar, choose Utilities → Utilities Setup...
2. Open the Remote tab and set Remote Control to TCP/IP.
3. Verify that the oscilloscope shows an IP address.

Add Oscilloscope Connection to QualiPHY

1. On the host PC, download and run QualiPHYInstaller.exe.
2. Start QualiPHY and click the General Setup button.
3. On the Connection tab, click Scope Selector.
4. Click Add and choose the connection type. Enter the oscilloscope IP address from Step 3 above. Click OK.
5. When the oscilloscope is properly detected, it appears on the Scope Selector dialog. Select the connection and click OK. QualiPHY is now ready to control the oscilloscope.

Select Oscilloscope Connection

Multiple oscilloscopes may be accessible to a single remote host. In that case, go to the QualiPHY General Setup Connection tab and use the Scope Selector at the start of each session to choose the correct connection.

QualiPHY tests the oscilloscope connection when starting a test. The software warns you if there is a connection problem.

Set Up Dual Monitor Display (optional)

If you are not executing QualiPHY from a remote PC, we recommend attaching a second monitor to the oscilloscope. This allows the waveforms and measurements to be shown on the oscilloscope LCD display while the QualiPHY application and test results are displayed on a second monitor.

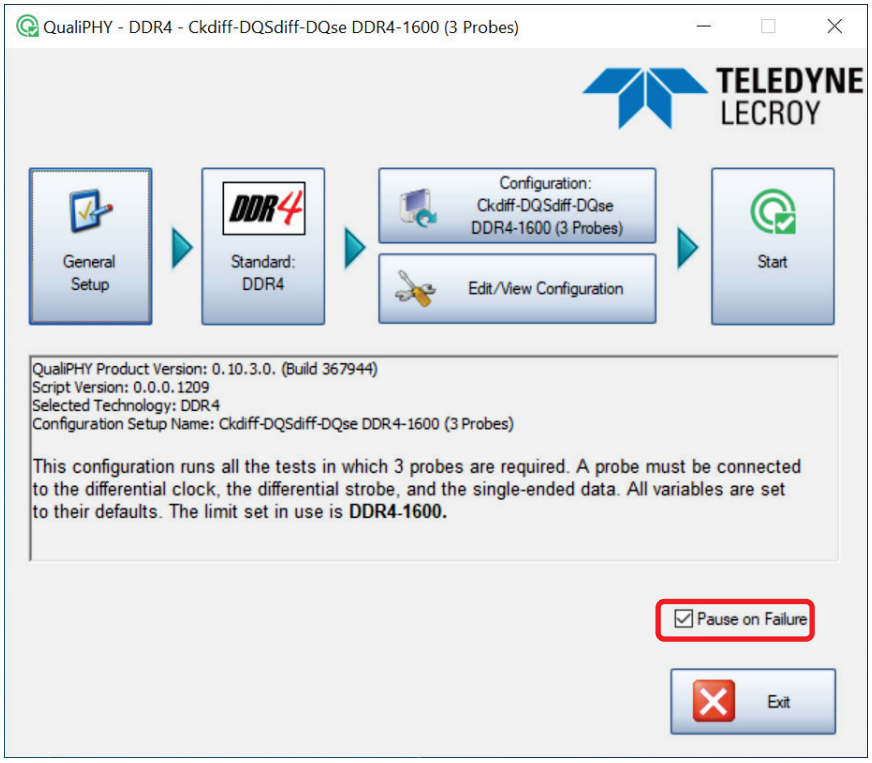
See the oscilloscope *Operator's Manual* for instructions on setting up dual monitor display.

Set Up the QualiPHY Application

The following general settings will persist with each test session you run in QualiPHY. We recommend these be made as part of initial installation. To begin, access the QualiPHY wizard by either:

- Choosing **Analysis > QualiPHY** from the oscilloscope menu bar
- Double-clicking the **QualiPHY desktop icon**  on a remote computer or oscilloscope desktop.

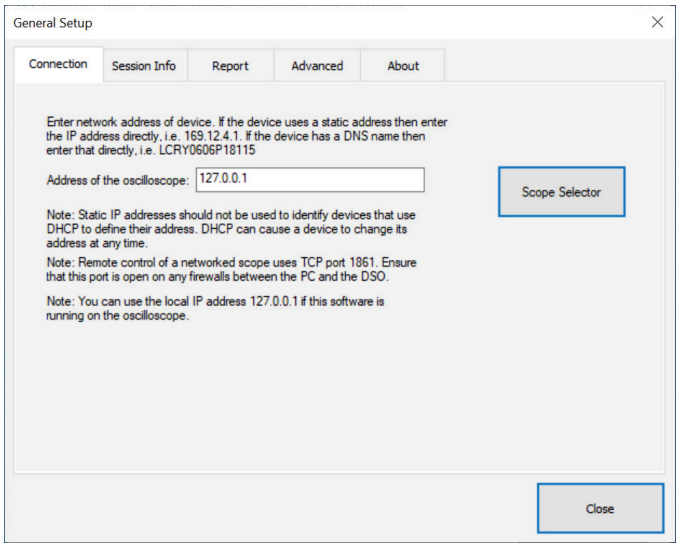
When **Pause on Failure** is checked, QualiPHY will pause execution whenever a test fails and prompt you to make corrections before retrying a measurement. You may open DDR Debug Toolkit to analyze the failure, even if you have not purchased the Debug Toolkit license.



On the Wizard, click the **General Setup** button to continue.

Connection Tab

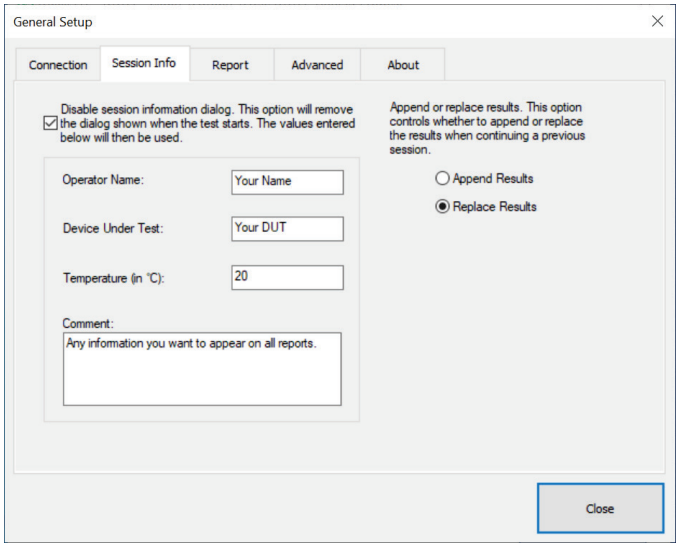
The Connection tab shows the **Address of the oscilloscope** is local host 127.0.0.1 when QualiPHY is run from the oscilloscope. If you are running QualiPHY from a remote computer, this will show the network IP address of the oscilloscope to which QualiPHY is currently connected.



The **Scope Selector** button allows you to choose the oscilloscope used for testing when several are connected to the QualiPHY application on a remote host. See Set Up Remote Control for details.

Session Info tab

The Session Info tab contains information that appears on reports, such as: **Operator Name**, **Device Under Test** (DUT) name, **Temperature (in °C)** of the test location, and any additional **Comments**.

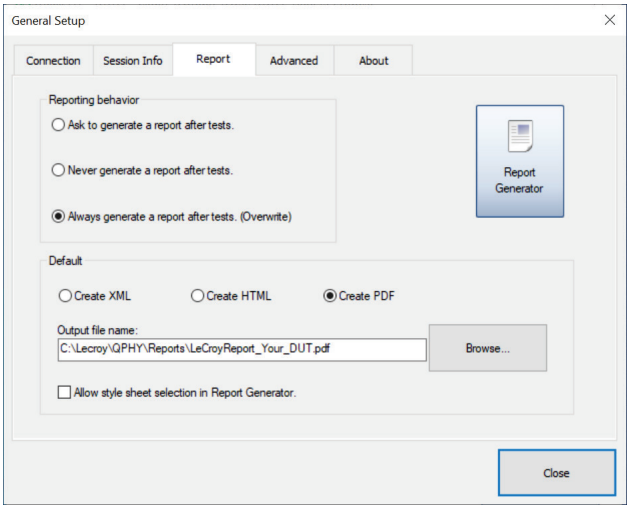


If you check **Disable session information dialog**, these global settings will be used on all reports. Otherwise, you will be presented with a dialog at the start of each session that overrides these settings.

There is also a selection to **Append Results** or **Replace Results** (overwrite) when continuing a previous test session.

Report tab

The Report tab contains settings related to report generation.



Choose a **Reporting behavior** of:

- "Ask to generate a report after tests"—you'll be prompted to create a new file for each set of test results.
- "Never generate a report after tests"—you'll need to manually execute the Report Generator.
- "Always generate a report after tests" will autogenerate a report of the latest test results.

Choose a **Default** report output file format of XML, HTML, or PDF.

Optionally, check **Allow style sheet selection in Report Generator** to enable the use of a custom .xslt when generating XML and HTML reports. The path to the .xslt is entered on the Report Generator dialog.

The **Report Generator** button launches the Report Generator dialog, which contains the same settings as the Report tab, only applied to individual reports. This dialog appears automatically at the conclusion of each test group if you have selected "Ask to generate a report after tests."

DDR4/LPDDR4 Testing

If you are new to QualiPHY, review Using QualiPHY to understand the conventions of the user interface.

Required Hardware

In addition to the oscilloscope, you will need the following to run the DDR4/LPDDR4 tests:

- 3 to 4 DHXX-PB2 Series probes and DH-SI solder tips. This is to measure the DQ (Data), CK (Clock), DQS (Strobe) and possibly the CA (Command Address).
- Interposers make a world of difference in a high-quality setup. They are soldered between the PCB and the DRAM chip to provide easy probing points. Reach out to Nexus (world-wide) or EyeKnowHow (Europe).
- A HDA125 Logic Analyzer is a modular and upgradable MSO that probes the Command Address lanes to trigger and decode. It vastly improves the Read / Write packet separation and is highly recommended.

Test Preparation

Before beginning any test or data acquisition, allow the oscilloscope and probes to warm up for at least 30 minutes after powering on.

Oscilloscope calibration is automatically performed by the oscilloscope application; no manual calibration is required. The calibration procedure will be run again if the temperature of the oscilloscope changes by more than a few degrees.

Connecting Probes

Determining Signals to Access

The required signals to probe depend up on which tests are being run in QPHY-DDR4. The configurations are tailored to different probe setups to allow you to easily see which signals are required for a particular test.

Best Places to Probe

The DDR4, LPDDR4 and LPDDR4X specifications are defined by the JEDEC standards to be tested at the balls of the DRAM (BGA). The probes should be placed as close to the DRAM as possible in order to follow the JEDEC defined specification. This is important to minimize signal quality issues, such as reflections that can occur on the signals.

For the best signal fidelity capture, it's recommended that an interposer be soldered in between the DRAM and the PCB. Typically, the DRAM sits on the interposer, which sits on a riser board, which sits on the PCB. By using an interposer, the solder-down probe leads can easily be accessed with little impact to the signal.

Two companies that offer interposers and/or installation in circuit are Nexus Technologies (world wide) and EyeKnowHow (Europe).

Another commonly used method is to place vias on the PCB to access the data, strobe, clock or command address signals. These typically are too small, so during layout it's recommended to run traces to make them easier to solder to and place them at similar distances from the BGA. The closer you are to the BGA the better, to help ensure fewer reflections due to trace length. If using this method, apply VirtualProbe software to de-embed the trace lengths with simulated S-parameter files.

Deskewing Probes

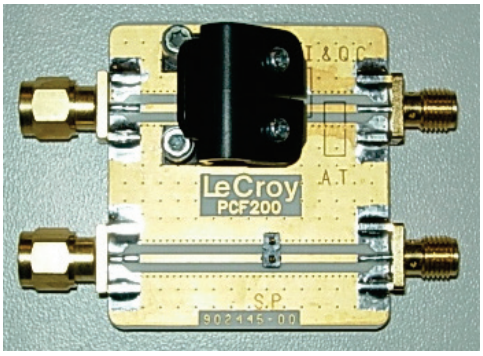
For DDR measurements, it is crucial properly deskew probes before running tests to ensure proper signal timing. Ideally, the same settings should be used when deskewing as when acquiring signals for analysis. This will ensure that the channels are deskewed using the same setup as when running compliance tests. Deskew values are saved and stored by QualiPHY at the beginning of each run.

For ease of connectivity, we recommend using the SP tip to deskew, but as long as the same tip is used to deskew each probe, it does not matter which style of tip is used.

Required Equipment

- PCF200 deskew fixture. The fixture has two signal paths:
    - The upper path (with the black clip) is for Solder-In (SI), Quick-Link Solder-In (QL-SI), Quick-Connect (QC) and Adjustable Tip (AT) probe tips.
    - The lower path is for Square-Pin (SP) probe tips.
- 50 Ω terminator

Note: Alternatively, use an LPA-K-A adapter and SMA cable.

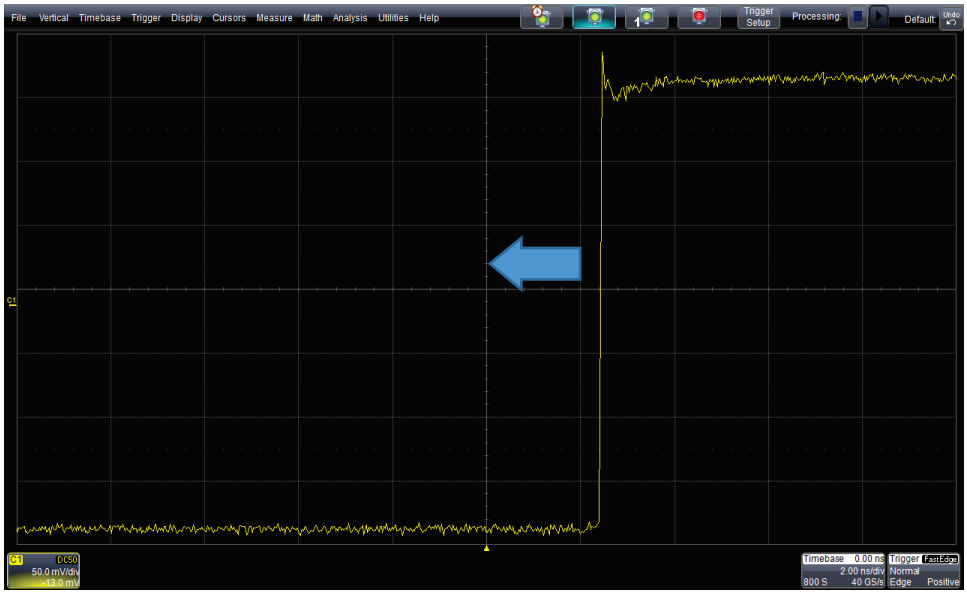


Deskew Method

Before beginning the procedure, be sure to warm the oscilloscope for at least 30 minutes.

1. Connect the PCF200 to the oscilloscope's fast edge output.
2. Connect probes electrically in a single-ended arrangement using their designated area on the fixture:
    - Connect the positive side of the probe to the signal trace (in between the two white strips). The positive polarity is indicated on the tip of the probe by a plus sign.
    - Connect the negative side to the ground plane (outside of the white strips).
    - To minimize reflections, apply a 50 Ω terminator to the end of the signal path in use. If a 50 Ω terminator is not available, an SMA cable can be used to terminate the PCF200 to one of the oscilloscope's outputs.
3. Set the oscilloscope Trigger Source to Fast Edge, Trigger Type to Edge.
4. Set a Timebase of approximately 10 ns/div and Timebase Delay of 0.

    Once everything is properly set up, the oscilloscope display should look similar to the figure below. If there is no propagation delay due to the probe, and no internal oscilloscope channel propagation delay, the 50% trigger level will be at the center line of the oscilloscope grid.



5. From the channel setup dialog (C*n*):
    - Enable **Sinx/x** interpolation and set the **Averaging** to **50** sweeps.
    - Touch the **Deskew** field once to highlight it, then adjust the deskew value to move the rising edge of the trace to the center of the display.
6. Now, decrease the **Timebase** to around **20 ps/div** and once again adjust the **Deskew** value so that the 50% rising edge point is centered in time.

Repeat this deskew procedure for each probe using the same probe tip.

Note: Before moving on to the next probe, reset Averaging to 1 sweep and turn off Sinx/x interpolation.

When QualiPHY is started, the deskew values from each channel dialog are saved and stored by QPHY at the beginning of each run. However, at the end of testing these values will be erased. By saving a panel setup (.lss file), it is possible to refer to the deskew values after testing has completed.

Read (R) and Write (W) Burst Requirements

Read/Write Burst Separation

One of the most critical aspects of memory testing is separating the bi-directional Data (DQ) and Strobe (DQS) lines, which each have data moving in two directions ("Write" packets from the PHY controller and "Read" packets from the DRAM). If you're testing DDR4 or LPDDR4/4X, there are three different methods for burst separation. Some are more reliable based on the allowable variations of the JEDEC standards.

Phase Detection

In DDR4 we can separate Read and Write bursts depending upon the skew relationship between the Data (DQ) and Strobe (DQS) signals. For a Write burst, the JEDEC standard and the QPHY-DDR4 software expect to see that the DQ and DQS signals are approximately a quarter cycle (~90 degrees) out of phase. For a Read burst, QPHY-DDR4 expects that the DQ and DQS signals are in phase.

Preamble Detection

In LPDDR4/4X we can separate the Read and Write bursts depending on a unique set of characteristics of the preamble/postamble relationship of the Data (DQ) and Strobe (DQS). Some designs allow a "don't care" state before the typical idle state of the preamble. For these designs, if there are other signal quality issues, there can be problems separating the burst packets. In that case, use the CMD Address method with the HDA125.

Command Address Detection (with HDA125)

For both DDR4 and LPDDR4/4X, the most reliable solution for R/W burst separation is using the HDA125 High-speed Data Analyzer. By probing the Command Address (CA) lines we can determine exactly when the memory is communicating Read or Write information, and the QPHY-DDR4 software uses this for packet separation to overcome any signal quality issues that might cause algorithm challenges.

Read/Write Burst Generation

It is recommended to capture a minimum of 10 Read and 10 Write bursts during each acquisition, but for greater statistical significance, it is encouraged to capture more.

DDR4 Burst Generation

Programs that can communicate with the DRAM and controller are widely available. For PCs, one popular option is *Memtest86+*, which is available for download from memtest.org as well is integrated in some PC BIOS menus.

When using Memtest, it is recommended to randomly generate the amount of data. We've found test mode 7, which will randomly generate both Read and Write bursts, to be successful. Other custom programs like *Windows Memory Diagnostic* can be used to stimulate the transfer of data to DIMM.

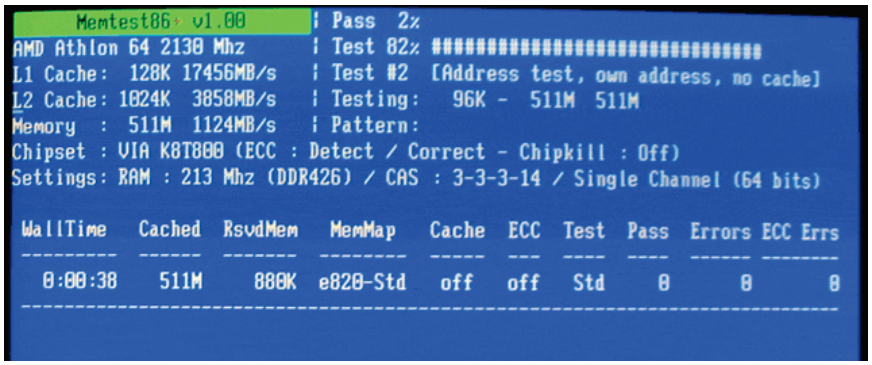


Figure 1. Memtest86+ software.

LPDDR4/4X Burst Generation

Testing of LPDDR4/4X can be more difficult, as the design is not usually on a PC. Thus, the implementer will typically have a manual way of controlling the DRAM communication in order to generate Read or Write packets. Configure QPHY-DDR4 to analyze either Read or Write packets in the wizard Setup tab, “Burst Under Test”.

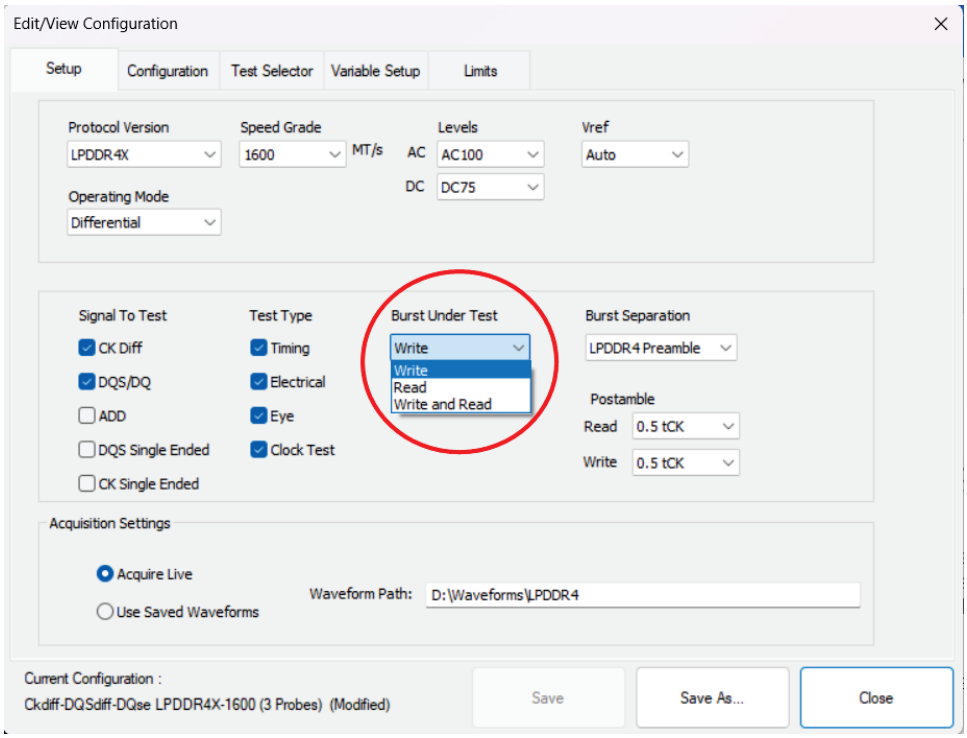


Figure 2. Choose to analyze Read or Write burst types only.

Initial Signal Checking

Before running QualiPHY to test DDR4, LPDDR4 or LPDDR4X, check the signals to verify that they make sense. This section covers some of the basic things which should be verified by the operator before running QPHY-DDR4.

Expected Channels

By default, QPHY-DDR4 expects to see the Clock (CK) on CH1, Strobe (DQS) on CH2 and Data (DQ) on CH3. This is what is shown in the connection diagram. The Input Channel variable can always be used to modify any of these channel assignments.

Signal Amplitude Clipping

For best results, it is recommended that the signals take up 80% of the vertical graticule for the best measurement accuracy. Avoid allowing the signal to go outside the oscilloscope vertical screen, as this clips and removes the usable data.

Clock Frequency

By applying the Frequency measurement parameter to the CK signal, you can verify that the DDR/LPDDR system is running at the expected transfer rate (Transfer Rate = Frequency * 2). This will also help in the limit selection. Do a quick visual inspection to ensure that the signal does not have any non-monotonic edges due to reflections.

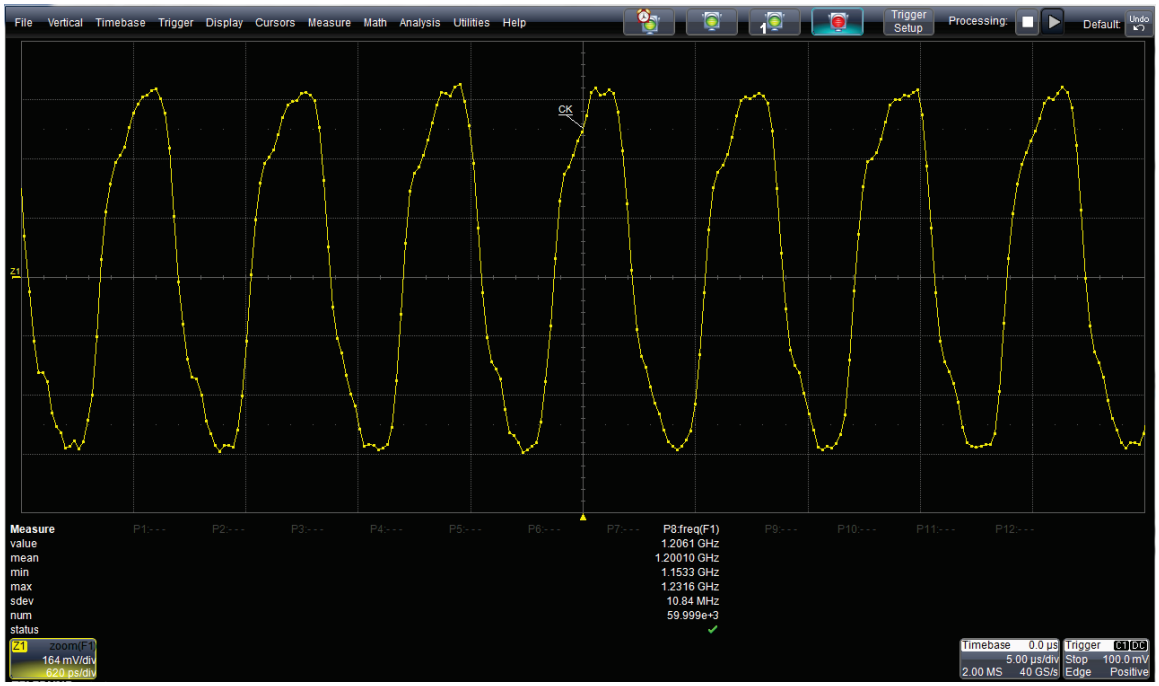


Figure 3. Verification of CK signal.

Presence of Read/Write Burst

In DDR4, a quick check can evaluate the quality of the burst packets. As a general rule of thumb during a Read burst, DQ and DQS should be in phase, and during a Write burst, DQ and DQS should be a quarter cycle out of phase as seen in Figure 4. Additionally, the signal amplitude can be used to determine the presence of R and Write bursts. If probing at the memory, users can typically expect Read bursts will have a larger amplitude than Write bursts

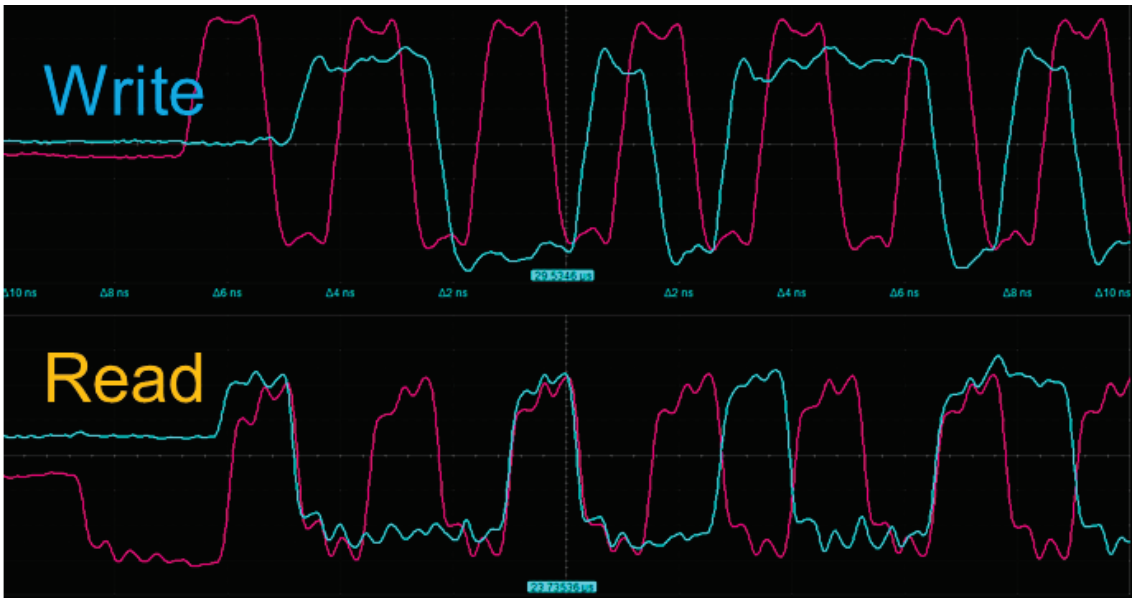


Figure 4. DDR4 Signal Phase verification (Write out of phase, Read in phase).

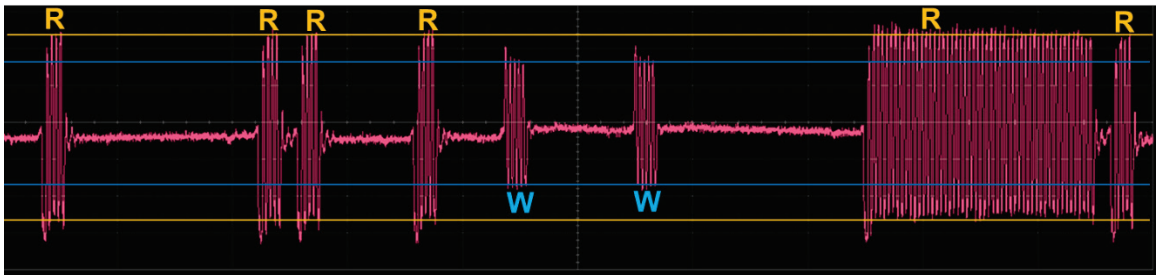


Figure 5. Amplitude can help validate if different burst packets are present.

Idle Levels

Before running test on DDR4, validate the signal idle levels. Signal idle levels that are off will have an impact on the R/W burst detection, electrical, and timing measurements. DQS should have an idle level of ~ 0 mV. In DDR4, the DQ should have an idle level ~0 V to 1.2 V and a DQS ~ 0 V. In LPDDR4/4X this range can be as low as ~0 V or can be in a "don't care" state on the DQS. Refer to the JEDEC specification for official requirements.

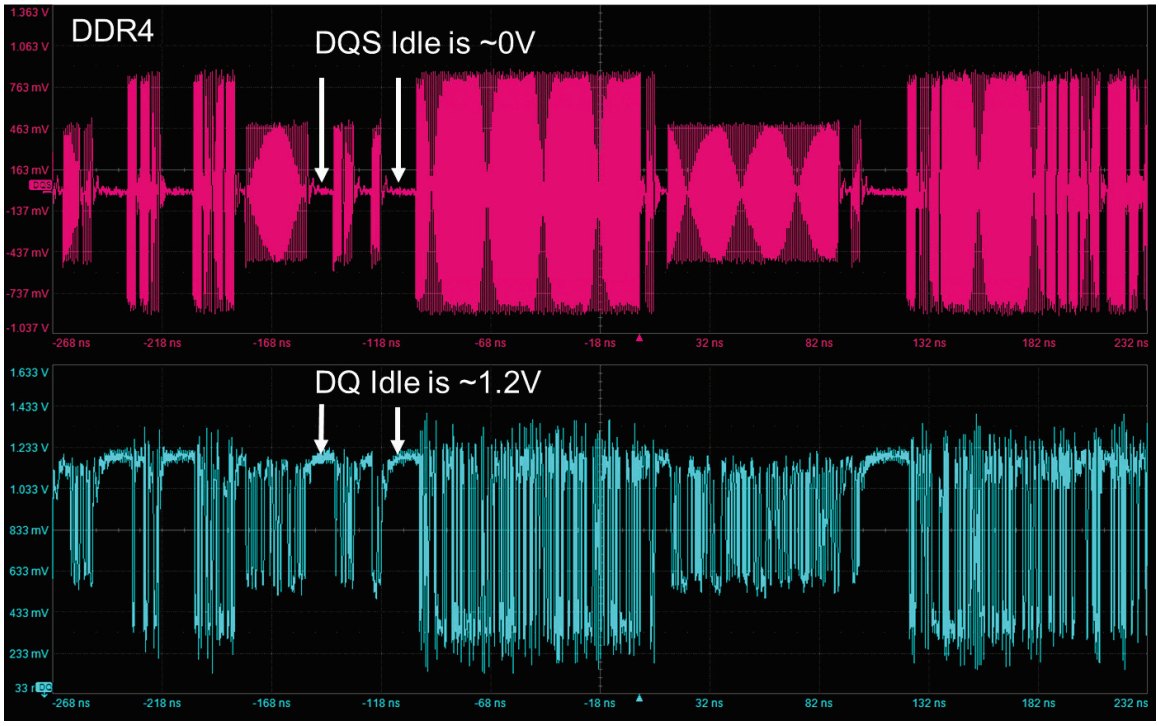
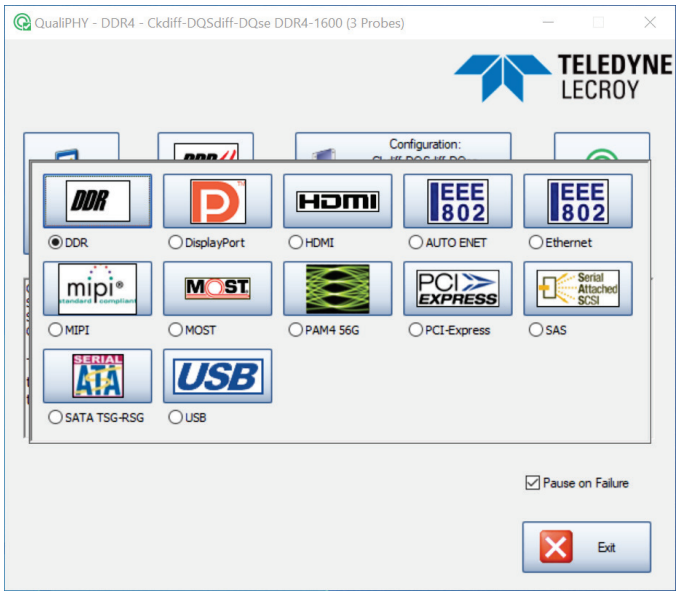


Figure 6. Verification of Idle levels.

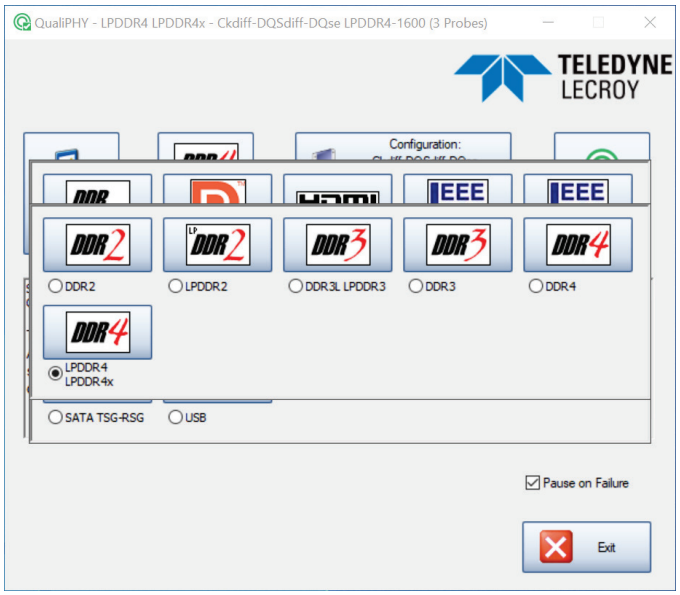
Test Initiation

Follow these steps to begin a new DDR test session in QualiPHY:

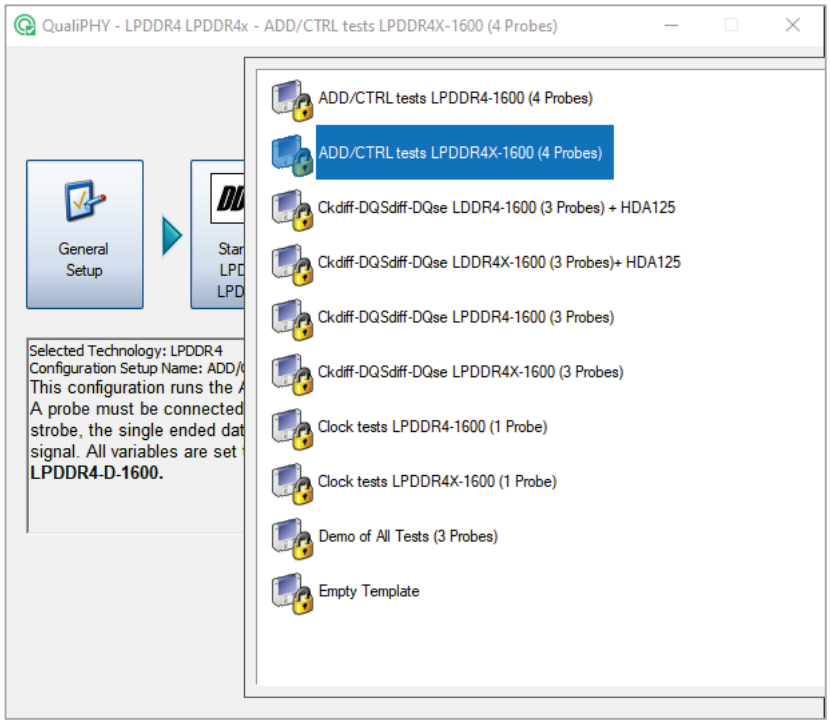
1. Access QualiPHY by either:
   - Choosing **Analysis > QualiPHY** from the oscilloscope menu bar
   - Double-clicking the **QualiPHY desktop icon**  on a remote computer or oscilloscope desktop.
2. Open the QualiPHY wizard, select the **Standard** button and choose **DDR**:



3. Select the memory type you wish to test (e.g., DDR4 or LPDDR4 / LPDDR4X).



4. On the wizard, click the **Configuration** button and select the test configuration you wish to run. Different configurations are designed to set key variables as required for different probing setups or testing different types of DUTs, etc.



Note: Standard configurations are locked and cannot be changed. If you need to change any test variables, you will be prompted to Save As a new copy. See Customizing QualiPHY for more information about creating custom configurations.

5. Click **Edit/View Configuration** and modify any variables required on the **Setup** tab. The standard configurations are preset to run tests according to JEDEC test standards.

   For DDR4 testing, set:

   a. **Speed Grade**: Select the operating memory speed.

   b. Make sure the **Limit Set** matches the Speed Grade. (For example, speed grade 2400 MT/s should match a limit set of DDR4-2400.)

   For LPDDR4 testing, set:

   a. **Protocol Version**: LPDDR4

   b. **Speed Grade**: Select the operating memory speed.

   c. Select the **Signal(s) to Test** (e.g., CK Diff, DQS/DQ, Add or single-ended connections to probes).

   d. Choose the **Test Type(s)** you're interested in running (e.g., Timing, Electrical, Eye, Clock). The individual tests and measurement explanations can be found on the Test Selector tab.

   e. Indicate whether it is the Read or Write **Burst Under Test**.

   f. Choose a **Burst Separation** method. If using the Preamble method, also enter the number of tCKs in the Read or Write burst **Postamble**. This will help with separation.

   g. Whether to **Acquire Live** or **Used Saved Waveforms**. If saved waveforms, enter the **Waveform Path**.

For LPDDR4X testing, set:

a. **Protocol Version**: LPDDR4X

b. The output signals of Strobe (DQS) and Clock (CK) of LPDDR4X can operate as single-ended or differential. In SE mode, the DRAM conserves power and uses only the True and not the Compliment portion of the Clock and Strobe. It's important to properly select the **Operating Mode** that represents the memory's output configuration.

c. **Speed Grade:** Select the operating memory speed. If in Single-Ended Operation Mode, only speeds at or below 1600 MT/s are available.

d. Select the **Signal(s) to Test** (e.g., CK Diff, DQS/DQ, Add or single-ended connections to probes).

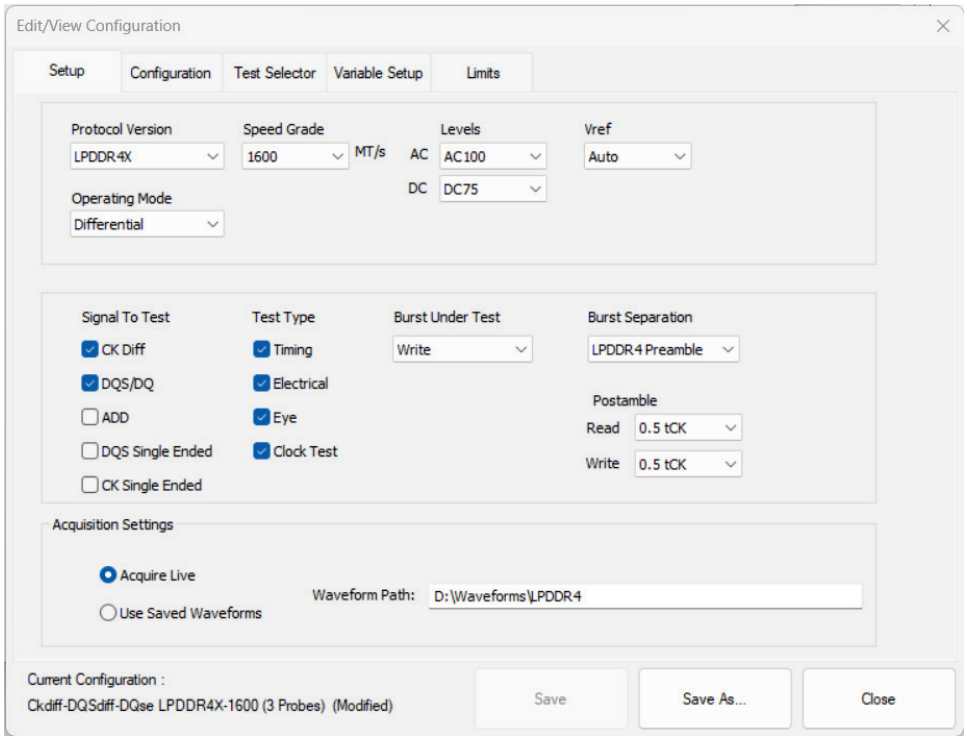
Note: If in Single Ended Operating Mode, only select Single Ended signals.

e. Choose the **Test Type(s)** you're interested in running (e.g., Timing, Electrical, Eye, Clock). The individual tests and measurement explanations can be found on the Test Selector tab.

f. Indicate whether it is the Read or Write **Burst Under Test**.

g. Choose a **Burst Separation** method. If using the Preamble method, also enter the number of tCKs in the Read or Write burst **Postamble**. This will help with separation.

h. Whether to **Acquire Live** or **Used Saved Waveforms**. If saved waveforms, enter the **Waveform Path**.



When done making changes, **Save As** a new configuration and **Close** the dialog.

6. Select the new, modified Configuration, then click the Start button on the QualiPHY wizard.

7. As configuration diagrams appear, follow the instructions to set up the test equipment.

DDR4 and LPDDR4/4X Test Configurations

Test configurations include basic test selections, variable settings and limit sets. You may load a test configuration, edit it for the desired speed and setup, then save it for future use. See DDR4/LPDDR4 Test Descriptions and DDR4/LPDDR4 Variables and Limits for more information about each.

Note: The configurations below are customized for DDR4, LPDDR4 or LPDDR4X. For example, the configuration named ADD/CTRL Tests DDR4-1600 (4 Probes) will test at DDR4 limits, while that named ADD/CTRL Tests LPDDR4-1600 (4 Probes) will test at LPDDR4 limits. For the most part, tests are conducted in the same manner, regardless of the standard. Exceptions will be noted in the manual.

Important: Custom configurations will be erased when making a firmware upgrade.

ADD/CTRL Tests DDR4/LPDDR4/LPDDR4X-1600 (4 Probes)

This configuration runs the Address/Control tests for which four probes are required. A probe must be connected to the differential clock, the differential strobe, the single-ended data, and the single-ended Address/Control signal. All variables are set to their defaults. The limit set in use is DDR4-1600, LPDDR4-1600 or LPDDR4X-1600, depending on which standard you are testing.

Ckdiff-DQSdiff-DQse DDR4/LPDDR4/LPDDR4X-1600 (3 Probes) + HDA125

This configuration runs all tests for which three probes are required, using the HDA125 for burst separation. A probe must be connected to the differential clock, the differential strobe, and the single-ended data. All variables are set to their defaults. The limit set in use is DDR4-1600, LPDDR4-1600 or LPDDR4X-1600, depending on which standard you are testing.

Ckdiff-DQSdiff-DQse DDR4/LPDDR4/LPDDR4X-1600 (3 Probes)

This configuration runs all tests for which three probes are required, using either Read or Write bursts (as selected in Configuration Setup). A probe must be connected to the differential clock, the differential strobe, and the single-ended data. All variables are set to their defaults. The limit set in use is DDR4-1600, LPDDR4-1600 or LPDDR4X-1600, depending on which standard you are testing.

Clock Tests DDR4/LPDDR4/LPDDR4X-1600 (1 Probe)

This configuration runs all the clock tests (only) and requires one probe to be connected to the differential clock. All variables are set to their defaults. The limit set in use is DDR4-1600, LPDDR4-1600 or LPDDR4X-1600, depending on which standard you are testing.

Demo of All Tests (3 Probes)

This configuration uses saved waveforms stored in the Waveform Path folder to run the three probe tests. When running normally on the oscilloscope, the path is D:\Waveforms\<standard>. All variables are set to their defaults, except Use Stored Waveforms is set to Yes. The limit set is either DDR4-1600 or LPDDR4-1600, depending on which standard you are testing.

Empty Template

All tests are left deselected to allow creation of a custom configuration. The limit set in use is either DDR4-1600 or LPDDR4-1600, depending on which standard you are testing. All variables are set to their defaults.

DDR4 and LPDDR4/4X Test Descriptions

These are the DDR4, LPDDR4 and LPDDR4X compliance tests. Unless stated, tests are conducted in the same manner for all three JEDEC memory standards.

Probe Auto Zero

This selection will prompt you to perform an Auto Zero of probes at the beginning of the test session. It should always be performed when changing the probe setup or at the first run after power-up. If Deskew is selected, Auto Zero will be performed during Deskew. It is selected by default for the test configurations; deselected by default for the Demo configuration.

Deskew

This selection will guide you step-by-step through the probe deskew process at the beginning of the test session. Deskew should always be performed when changing the probe setup. It is selected by default for the test configurations; deselected by default for the Demo configuration.

Clock Tests

To add these tests, on the Setup tab, check the box under 'Signal to Test' for *CK Diff* or *CK Single Ended,* then select the "Clock Test" category. This will automatically select the appropriate clock measurements from the Test Selector tab. For a list of explanations, please refer to the measurements below.

tCK(avg) and tCK(abs)

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

tCK(abs) is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge.

tCH(avg), tCH(abs), tCL(avg) and tCL(abs)

tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.

tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.

tJIT(duty) (DDR4 only)

tJIT(duty) is defined as the cumulative set of tCH jitter and tCL jitter over 200 consecutive cycles.

tCH jitter is the largest deviation of any single tCH from tCH(avg) and tCL jitter is the largest deviation of any single tCL from tCL(avg).

tJIT(duty) = Min/max of {tJIT(CH), tJIT(CL)} where, tJIT(CH) = {tCHi - tCH(avg) where i=1 to 200} and

tJIT(CL) = {tCLi - tCL(avg) where i=1 to 200}.

At the completion of the tCK, tCH, tCL, and tJIT(duty) tests, the oscilloscope is in the following state:

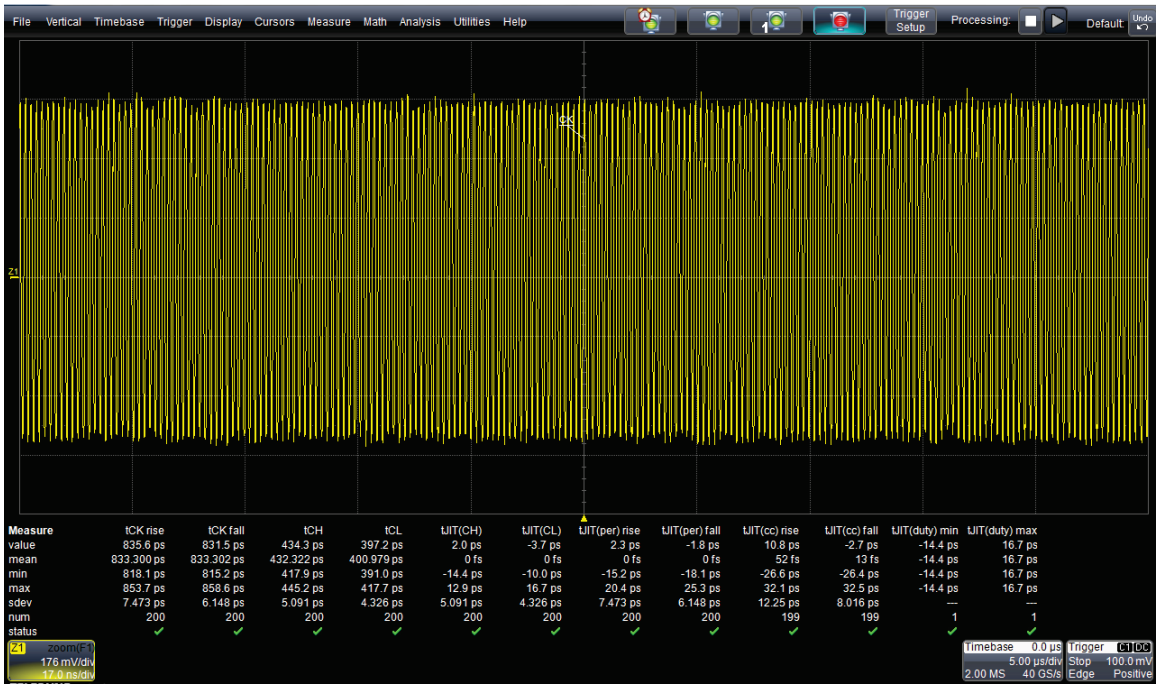


Figure 7. Oscilloscope configuration after tCK, tCH, tCL and tJIT(duty) tests.

Shown on the screen: Z1 is a zoom of the differential clock signal.

In the Measure table:

- **tCK rise** (P1) is the period measurement at Vref (0 mV) of Z1 (differential clock signal) on only the rising edges. The mean value is the measured value for **tCK(avg), rise**. The minimum value is the measured value for **tCK(abs), rise, min** reported in mtCK(avg). The maximum value is the measured value for **tCK(abs), rise, max** reported in mtCK(avg).
- **tCK fall** (P2) is the period measurement at Vref (0 mV) of Z1 (differential clock signal) on only the falling edges. The mean value is the measured value for **tCK(avg), fall**. The minimum value is the measured value for **tCK(abs), fall, min** reported in mtCK(avg). The maximum value is the measured value for **tCK(abs), fall, max** reported in mtCK(avg).
- **tCH** (P3) is the width measure at Vref (0 mV) of Z1 (differential clock signal) on only the high pulses. The mean value is the measured value for **tCH(avg)** reported in mtCK(avg). The minimum value is the measured value for **tCH(abs), min** reported in mtCK(avg).
- **tCL** (P4) is the width measure at Vref (0 mV) of Z1 (differential clock signal) on only the low pulses. The mean value is the measured value for **tCL(avg)** reported in mtCK(avg). The minimum value is the measured value for **tCL(abs), min** reported in mtCK(avg).
- **tJIT(CH)** (P5) subtracts the mean of P3 (tCH(avg)) from all of the tCH values. The minimum value is the measured value for **tJIT(CH), min** and the maximum value is the measured value for **tJIT(CH), max**.
- **tJIT(CL)** (P6) subtracts the mean of P4 (tCL(avg)) from all of the tCL values. The minimum value is the measured value for **tJIT(CL), min** and the maximum value is the measured value for **tJIT(CL), max**.
- **tJIT(per) rise** (P7) subtracts the mean of P1 (tCK(avg), rise) from all of the tCK rise values. This is displayed for informational purposes only and correlates to the legacy tJIT(per) measurement.

- tJIT(per) fall (P8) subtracts the mean of P2 (tCK(avg), fall) from all of the tCK fall values. This is displayed for informational purposes only and correlates to the legacy tJIT(per) measurement.
- tJIT(cc) rise (P9) takes the difference between the clock period of two consecutive cycles for only the rising edge. This is displayed for informational purposes only and correlates to the legacy tJIT(cc) measurement.
- tJIT(cc) fall (P10) takes the difference between the clock period of two consecutive cycles for only the falling edge. This is displayed for informational purposes only and correlates to the legacy tJIT(cc) measurement.
- tJIT(duty) min (P11) is the minimum value of the difference between minimum tCH/tCL clock period and the average tCH/tCL. This is the measured value for tJIT(duty), min in mUI.
- tJIT(duty) max (P12) is the maximum value of the difference between minimum tCH/tCL clock period and the average tCH/tCL. This is the measured value for tJIT(duty), min in mUI.

tJIT(per) (DDR4 and LPDDR4/4X) and tJIT(per)_dj (DDR4 only)

tJIT(per) measures Total jitter (Tj) and in DDR4 the test includes Deterministic jitter (Dj) using the dual-Dirac jitter model, where period measurements constitute the data set for the measurement. Tj and/or Dj are determined at a BER configured.

At the completion of tJIT(per)_dj (DDR4 only), the oscilloscope displays the following:

Figure 8. Oscilloscope configuration after tJIT(per) and tJIT(per)_dj tests.

Shown on the screen: RjBUjSpect is the RjBUj Spectrum of the differential clock signal. The signal type on the signal input section of SDA III is setup to measure a Clock and to use "Period" as the Jitter Parameter.

In the SDA Jitter table:

- Tj(1e-12) is the total jitter calculated using the spectral direct method in SDA III. You can modify the BER level using the *Jitter BER Level* variable (see Jitter BER Level for more information). This value is reported as tJIT(per)_total in ps for informational purposes. The value is also reported in UI to be tested against the limit from the specification.
- Rj(spD) is the random jitter calculated using the spectral direct method in SDA III. This value is reported for informational purposes.
- Dj(spD) is the deterministic jitter calculated using the spectral direct method in SDA III. This value is reported as tJIT(per)_dj in ps for informational purposes. The value is also reported in UI to be tested against the limit from the specification.

tJIT(cc)

This test measures Total jitter (Tj) using the dual-Dirac jitter model, where cycle-to-cycle measurements constitute the data set for the measurement. Tj is determined at a BER configured.

At the completion of the tJIT(cc) test, the oscilloscope shows the following (slight differences between DDR4 and LPDDR4/4X measurement results):

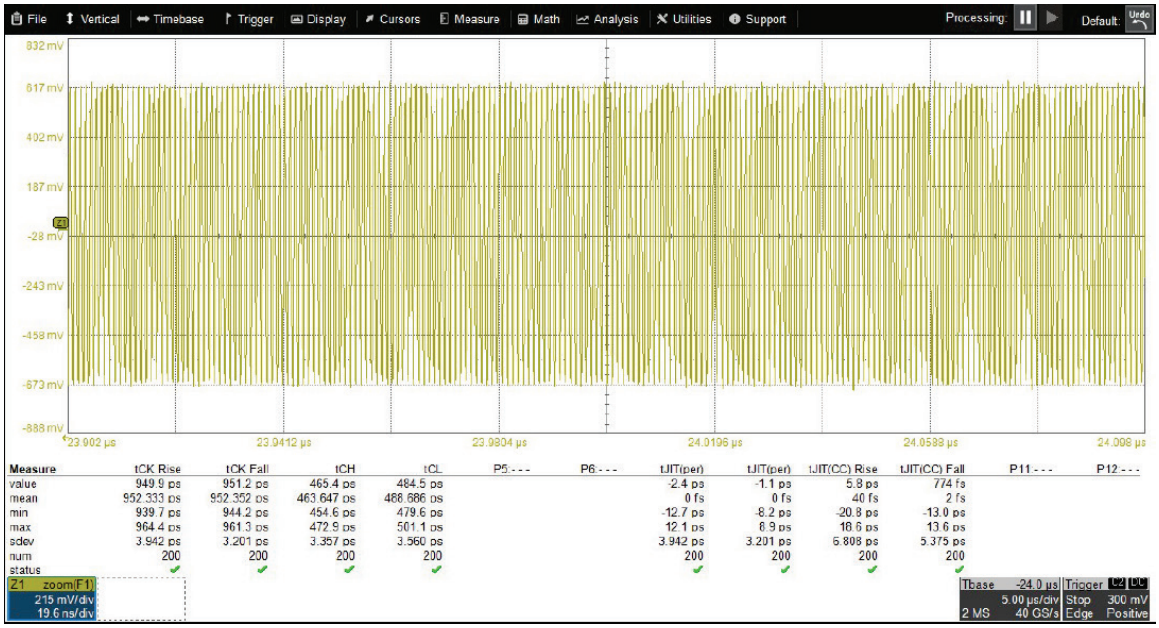


Figure 9. Oscilloscope configuration after tJIT(cc) tests.

tERR(nper) (DDR4 only)

tERR(nper) is defined as the cumulative error across n multiple clock cycles from tCK(avg). This test is performed with *n* ranging from 2 to 50 clock periods.

There are 12 different tests: tERR(2per), tERR (3per), tERR (4per), tERR (5per), tERR(6per), tERR (7per), tERR (8per), tERR (9per), tERR (10per), tERR (11per), tERR (12per), tERR (13-50per).

Note: Only tERR(2per), tERR (3per), tERR (4per), and tERR (5per) will be discussed below. The setup for all tERR(nper) tests is exactly the same.

At the completion of the tERR(2per), tERR (3per), tERR (4per), and tERR (5per) tests, the oscilloscope is in the following state:

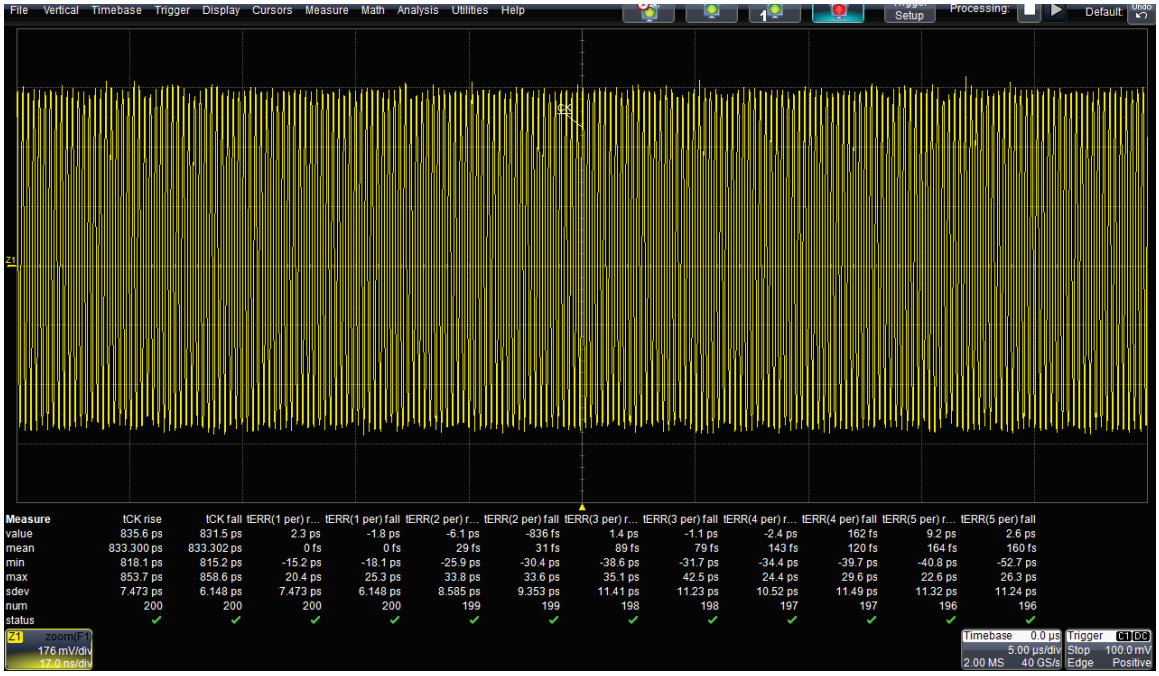


Figure 10. Oscilloscope configuration after tERR(2per), tERR (3per), tERR (4per) and tERR (5per) tests.

Shown on the screen: Z1 is a zoom of the differential clock signal.

In the Measure table:

- **tCK rise** (P1) is the period measurement at Vref (0 mV) of Z1 (differential clock signal) on only the rising edges. This value is used for the tERR calculation on the rising edge.
- **tCK fall** (P2) is the period measurement at Vref (0 mV) of Z1 (differential clock signal) on only the falling edges. This value is used for the tERR calculation on the rising edge.
- **tERR(1 per) r** (P3) is the TIE measure at Vref (0 mV) of Z1 (differential clock signal) on only the rising edges (positive pulses). It is set up to measure edges at intervals of 1. This is reported as informational only.
- **tERR(1 per) fall** (P4) is the TIE measure at Vref (0 mV) of Z1 (differential clock signal) on only the falling edges (negative pulses). It is set up to measure edges at intervals of 1. This is reported for information only.
- **tERR(2 per) r** (P5) is the TIE measure at Vref (0 mV) of Z1 (differential clock signal) on only the rising edges (positive pulses). It is set up to measure edges at intervals of 2. The minimum value is measured as **tERR(2per)rise, min** reported in mUI and the maximum value is measured as **tERR(2per)rise, max** reported in mUI.

- tERR(2 per) fall (P6) is the TIE measure at Vref (0 mV) of Z1 (differential clock signal) on only the falling edges (negative pulses). It is set up to measure edges at intervals of 2. The minimum value is measured as tERR(2per)fall, min reported in mUI and the maximum value is measured as tERR(2per)fall, max reported in mUI.
- tERR(3 per) r (P7) is the TIE measure at Vref (0 mV) of Z1 (differential clock signal) on only the rising edges (positive pulses). It is set up to measure edges at intervals of 3. The minimum value is measured as tERR(3per)rise, min reported in mUI and the maximum value is measured as tERR(3per)rise, max reported in mUI.
- tERR(3 per) fall (P8) is the TIE measure at Vref (0 mV) of Z1 (differential clock signal) on only the falling edges (negative pulses). It is set up to measure edges at intervals of 3. The minimum value is measured as tERR(3per)fall, min reported in mUI and the maximum value is measured as tERR(3per)fall, max reported in mUI.
- tERR(4 per) r (P9) is the TIE measure at Vref (0 mV) of Z1 (differential clock signal) on only the rising edges (positive pulses). It is set up to measure edges at intervals of 4. The minimum value is measured as tERR(4per)rise, min reported in mUI and the maximum value is measured as tERR(4per)rise, max reported in mUI.
- tERR(4 per) fall (P10) is the TIE measure at Vref (0 mV) of Z1 (differential clock signal) on only the falling edges (negative pulses). It is set up to measure edges at intervals of 4. The minimum value is measured as tERR(4per)fall, min reported in mUI and the maximum value is measured as tERR(4per)fall, max reported in mUI.
- tERR(5 per) r (P11) is the TIE measure at Vref (0 mV) of Z1 (differential clock signal) on only the rising edges (positive pulses). It is set up to measure edges at intervals of 5. The minimum value is measured as tERR(5per)rise, min reported in mUI and the maximum value is measured as tERR(5per)rise, max reported in mUI.
- tERR(5 per) fall (P12) is the TIE measure at Vref (0 mV) of Z1 (differential clock signal) on only the falling edges (negative pulses). It is set up to measure edges at intervals of 5. The minimum value is measured as tERR(5per)fall, min reported in mUI and the maximum value is measured as tERR(5per)fall, max reported in mUI.

Eye Diagram Tests on Write Bursts

DQ and DQS Eye

This is an informational only test that creates an eye diagram for DQ and DQS of all the Write bursts detected in the acquisition. DQS is the timing reference for both eye diagrams and the reference point is shown on the center screen.

At the completion of the test, the oscilloscope is in the following state:

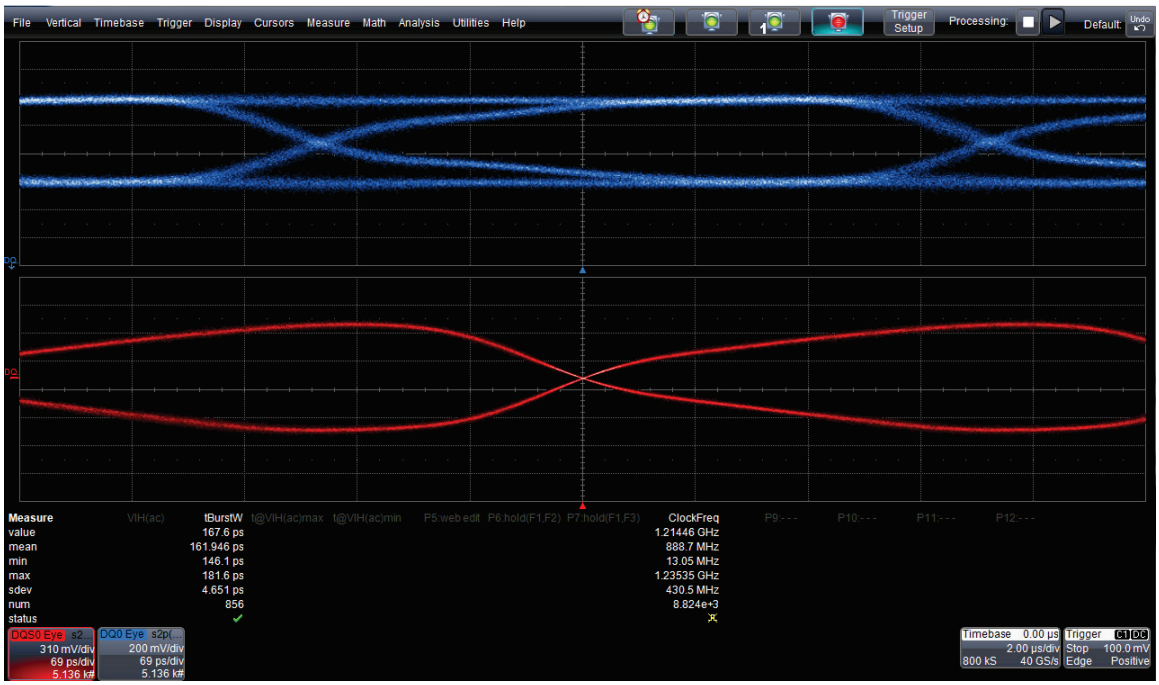


Figure 11. Oscilloscope configuration after Write Bursts (Inputs) – DQ and DQS Eyes.

Shown on the screen:

- F6 is the DQS Eye diagram of the write bursts from the acquired signal. DQS is used as the timing reference for this test which causes the eye to come to a "pin point" on the center grid. This math function is assigned an alias based on the assigned DQS signal name. The number of bits contained in the eye diagram is displayed in the bottom row of the F6 descriptor box. In this case there are 5,136 DQS bits in the eye.
- F7 is the DQ Eye diagram of the write bursts from the acquired signal. This math function is assigned an alias based on the assigned DQ signal name. The number of bits contained in the eye diagram is displayed in the bottom row of the F7 descriptor box. In this case there are 5,136 DQ bits in the eye.

In the Measure table:

- tBurst W (P2) displays the number of Write bursts detected in the acquisition.
- ClockFreq (P8) is the measured clock frequency from the acquired waveform.

DQ Write Input Compliance Mask

This tests the DQ Write Eye against the mask defined in the specification. The mask is created from the TdIVW_total and VdIVW_total limits for different speeds.

At the completion of the DQ Input Compliance Mask test, the oscilloscope is in the following state:

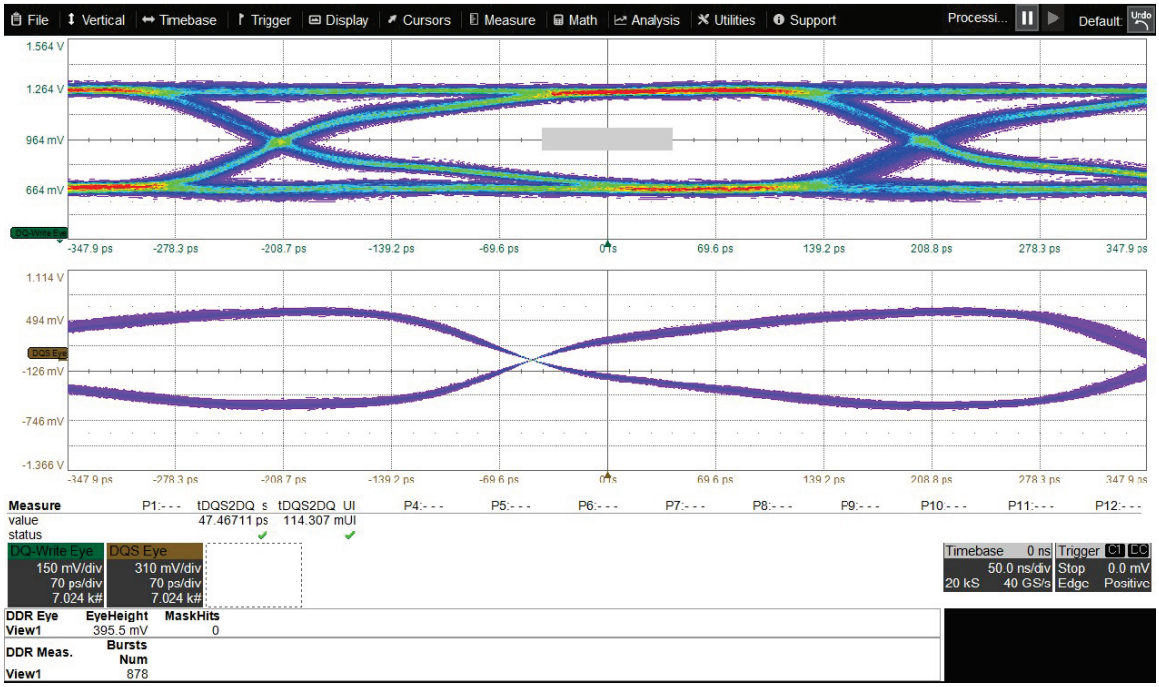


Figure 12. Oscilloscope configuration after DQ Write Input Compliance Mask test.

VIHL_AC

VIHL_AC will test the peak-to-peak amplitude of the DQ signal for each UI. The DQ signal must meet or exceed the specified level at any point over the total UI. It is measured as a peak-to-peak voltage centered at Vref.

At the completion of the VIHL_AC test, the oscilloscope is in the following state:

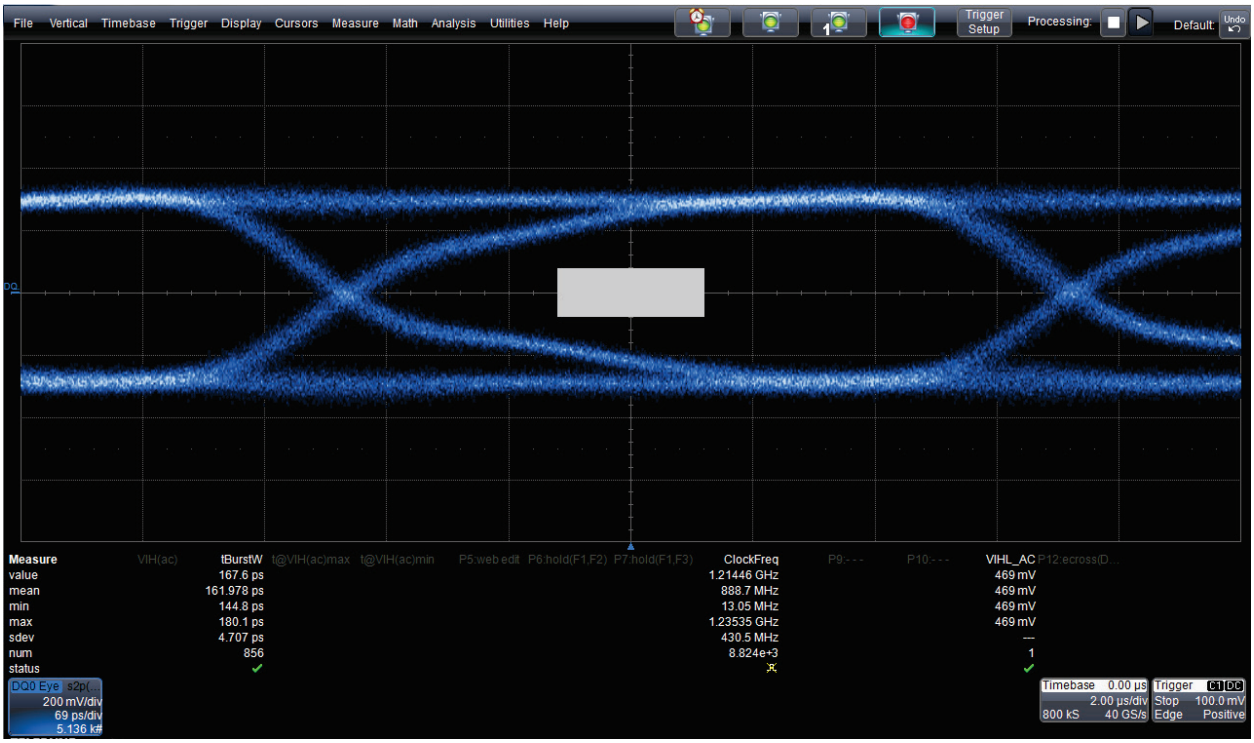


Figure 13. Oscilloscope configuration after VIHL_AC test.

Shown on the screen: F7 is the DQ Eye diagram of the Write bursts from the acquired signal. The DQS signal is the timing reference for this eye diagram. This math function is assigned an alias based on the assigned DQ signal name. The number of bits contained in the eye diagram is displayed in the bottom row of the F7 descriptor box. In this case there are 5,136 DQ bits in the eye.

In the Measure table:

- tBurst W (P2) displays the number of Write bursts detected in the acquisition.
- ClockFreq (P8) is the measured clock frequency from the acquired waveform.
- VIHL_AC (P11) calculates the minimum eye opening for each UI. The measured value is reported as VIHL_AC min.

tDQS2DQ (DDR4)

tDQS2DQ will measure the timing offset in Unit Intervals (DDR4) or pico-seconds (LPDDR4/4X) of the Rx Mask that is set up. This is the DQS_t DQS_c crossing in reference to the position of the DQ Rx Mask center position. There is an allowable range given by the JEDEC that is tested against to validate the timing offset is within the correct range.

Eye Diagram Tests on Read Bursts

DQ and DQS Eye

This is an informational test that creates an eye diagram for DQ and DQS of all of the Read bursts detected in the acquisition. DQS is the timing reference for both eyes and the reference point is shown on the second division.

At the completion of Read Bursts: DQ & DQS Eye, the oscilloscope is in the following state:

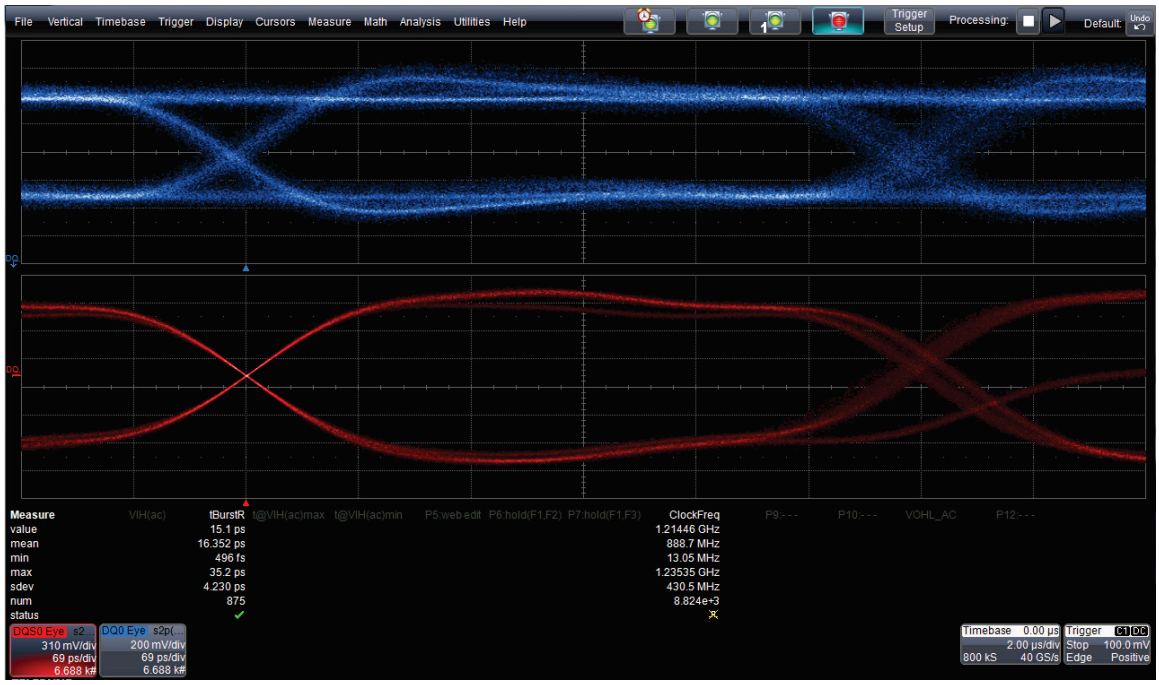


Figure 14. Oscilloscope configuration after Read Bursts (Outputs) test.

Shown on the screen:

- F6 is the DQS Eye diagram of Read bursts from the acquired signal. DQS is used as the timing reference for this test which causes the eye to come to a "pin point" on the second division. This math function is assigned an alias based on the assigned DQS signal name. The number of bits contained in the eye diagram is displayed in the bottom row of the F6 descriptor box. Here there are 7,000 DQS bits in the eye.
- F7 is the DQ Eye diagram of Read bursts from the acquired signal. This math function is assigned an alias based on the assigned DQ signal name. The number of bits contained in the eye diagram is displayed in the bottom row of the F7 descriptor box. Here there are 7,000 DQ bits in the eye.

In the Measure table:

- tBurst R (P2) displays the number of Read bursts detected in the acquisition.
- ClockFreq (P8) is the measured clock frequency from the acquired waveform.

tQW_total (LPDDR4/4X only)

tQW_total is a measurement that occurs on window time (think of it as the DQ Eye diagram width) of the read packet, which is the output data of the DRAM to the controller. This occurs at a selected DQx pin and is also defined by the JEDEC as when the Data Bus Inversion (DBI) is disabled.

Eye Diagram Tests on CA/CS (LPDDR4/4X only)

Analysis on the Command Address (CA) or Chip Select (CS) lines is important for signal quality inspection. Testing one or more signal lines is preferred, but the shortest and longest trace lengths will typically give you a good approximation.

CA/CS Eye

This is an informational only test that creates an eye diagram for CA or CS signals of all the Write bursts (input signals) detected in the acquisition. Vcent_CA is the timing reference for these eye diagrams.

CA/CS Mask

The test verifies no signal from the eye diagram goes through the JEDEC defined mask. The parameters for the mask are created from the TdIVW and VdIVW limits that change based on the designated DQ signal speed.

VIHL_AC for CA/CS

VIHL_AC will test the peak-to-peak amplitude of the CA or CS signal for each UI. The signal must meet or exceed the specified level at any point over the total UI. It is measured as a peak-to-peak voltage centered at Vcent_CA or Vcent_CS.

tDVAC (DDR4 only)

The purpose of this test is to verify the allowed time before ringback for the differential CK signal. It is measured as the time above the VIH(ac) level and below the VIL(ac) level. The clock signal is only measured when a Write burst has been detected.

Note: Only tDVAC measured on above VIH(ac) will be discussed below. The measurement methodology is exactly same for below VIL(ac).

At the completion of the tDVAC test, the oscilloscope is in the following state:

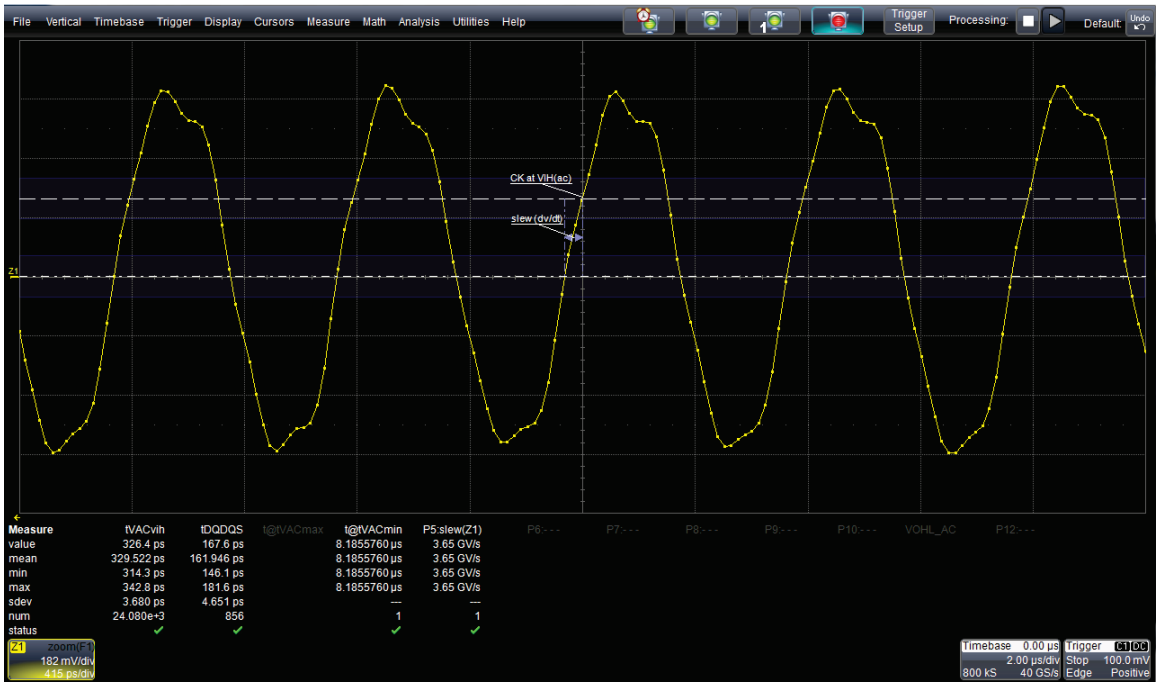


Figure 15. Oscilloscope configuration after the tDVAC test.

Shown on the screen: Z1 is a zoom of F1, the acquired CK signal after any probe deskew has been applied. The zoom is positioned at the location of the "worst case" tDVAC measurement indicated by t@tVACmin. A label is applied to this trace according to the signal name assigned to CK and placed at the VIH(ac) level.

In the Measure table:

- tVACvih (P1) is measuring the time above VIH(ac) for CK. VIH(ac) is indicated by the trace label "CK at VIH(ac)". The minimum value is the measured value for tDVAC min of CK. Because the limit is undefined by the specification, this test is Informational only.
- tDQDQS (P2) is measuring the skew between DQ and DQS. Since this measurement is performed once per burst, this shows how many Write bursts were in the acquired waveform.
- t@tVACmin (P4) displays the location of where the minimum value of tDVAC occurred. This is used to position the zoom traces at the location of the "worst case results".
- Slew(z1) is measuring the slewrate on the rising edge of CK at t@tVACmin from Vref to VIH(ac). This value is used to determine the appropriate limit for tDVAC.

Electrical Tests on Write Bursts (Inputs)

Input Slewrate

The purpose of these tests is to characterize the slewrate on all the Write (input) signals. The tests are performed on both rising and falling edges. By default the slewrate is measured on different signal types (DQ, DQS, CK, CA) depending on the measurement standard and their defined thresholds.

SRIdiff (DQS and CK)

For DDR4, the input slewrate is measured only on DQS. It's measured on each Input packet using the reference level of VIHdiff to VILdiff that is defined by the JEDEC per speed.

For LPDDR4/4X, the input slewrate is measured on DQS and CK. It's measured on each Input packet using the reference level of VIHdiff to VILdiff that is defined by the JEDEC per speed.

The QualiPHY report will show the result of the slewrate measured between the VILdiff and VIHdiff locations. The result will also show a separate min/max value that is tested to the JEDEC's limit. Results are in volts per nanoseconds (V/ns).

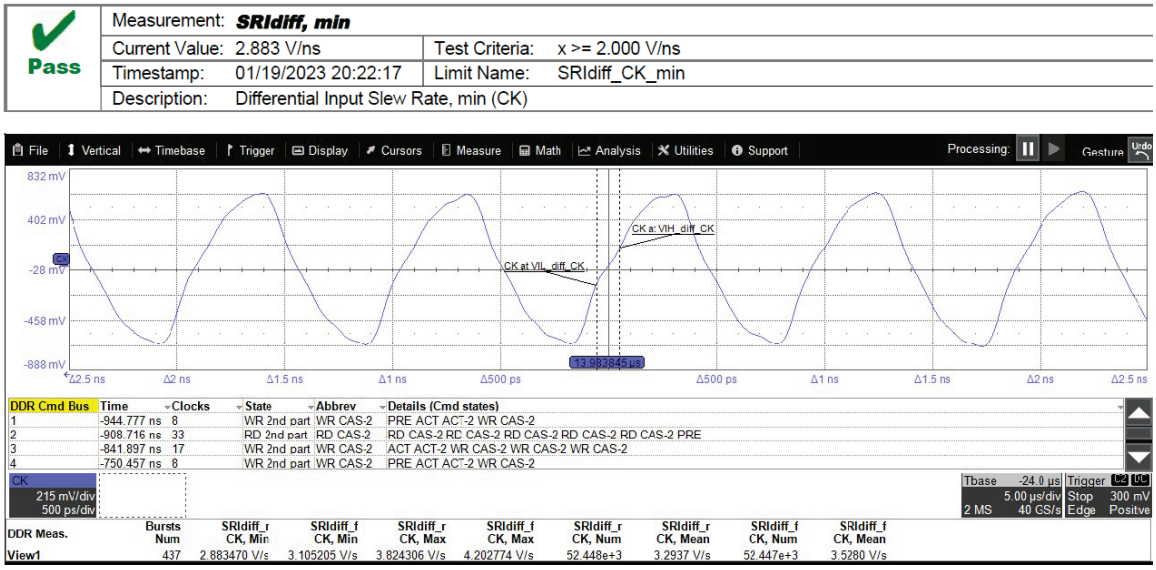


Figure 16. Oscilloscope configuration after SRIdiff_CK test.

srr1 and srf1 (DDR4 only)

This test measures the slewrate on DQ for rising and falling edges during Write bursts. The srr1 and srf1 are measuring the slew by dividing the voltage VDIVW(max) (speed-grade dependent) by the time found to traverse Vref.DQ(Write) +/- 0.5 * VDIVW(max). Both minimum and maximum values are measured for srr1 and srf1.

srr2 and srf2 (DDR4 only)

This test measures the slewrate on DQ for rising and falling edges during Write bursts above and below the mask voltage. Both minimum and maximum values are measured for srr2 and srf2.

srr2 = (VIHL_AC(min) - VdIVW(max)) / (2*tr2)

srf2 = (VIHL_AC(min) - VdIVW(max)) / (2*tf2)

SRIN_dIVW and SRIN_cIVW (LPDDR4/4X only)

These tests measure the Input Slewrate Rise and Fall over the VdiVW_total for the DQ and CA signals. Being based on the VdiVQ means that the high and low level of the Rx Mask (height) will define the upper and lower thresholds for the slewrate in reference to the center at either Vcent_DQ or Vcent_CA.

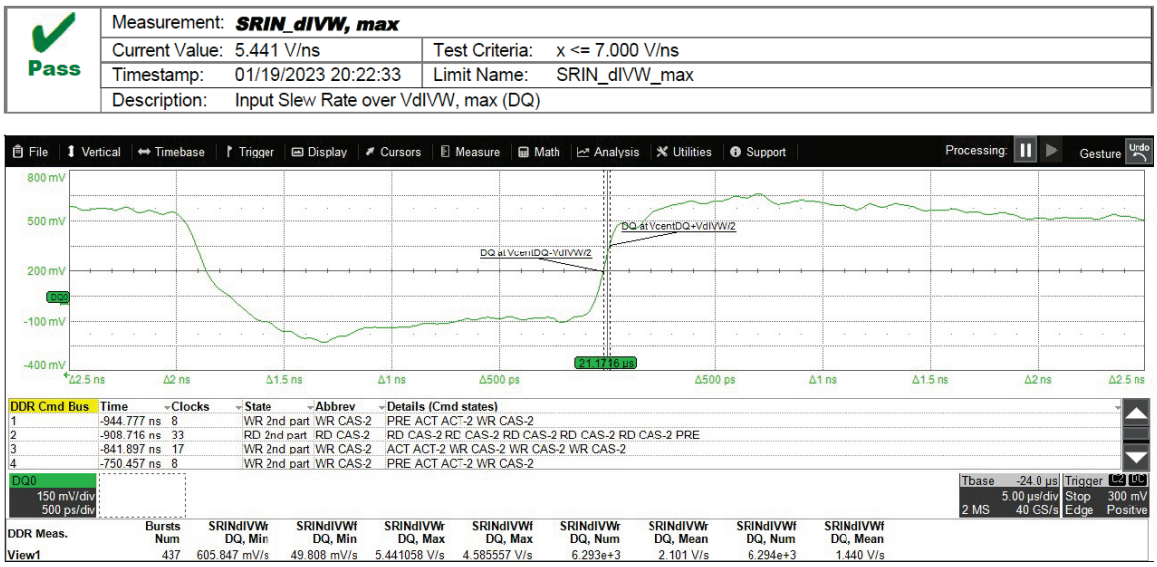


Figure 17. Oscilloscope configuration after SRIN_diVW, max test.

AC Over/Undershoot Peak and Area

The purpose of this test group is to characterize the overshoot above VDDQ and undershoot below VSSQ on DQ, DQS, CK and CA/ADDR during Write bursts. Both peak amplitude and area are tested.

Note: Only DQ overshoot will be shown here. The measurement methodology is exactly same for the DQS, CK, and CA/ADDR. The measurement methodology is also identical for undershoot and overshoot, except that VSSQ is used for undershoot instead of VDDQ.

DQ

This test measures the overshoot/undershoot, peak and area measurements on DQ signals:

- VDOSP: Maximum peak amplitude above VDOS
- VDUSP: Maximum peak amplitude below VDUS
- ADOS1: Maximum overshoot area per 1 UI between VDDQ and VDOS

- ADOS2: Maximum overshoot area per 1 UI above VDOS
- ADUS1: Maximum undershoot area per 1 UI between VSSQ and VDUS1
- ADUS2: Maximum undershoot area per 1 UI below VDUS

At the completion of the DQ Peak Amplitude test, the oscilloscope is in the following state:

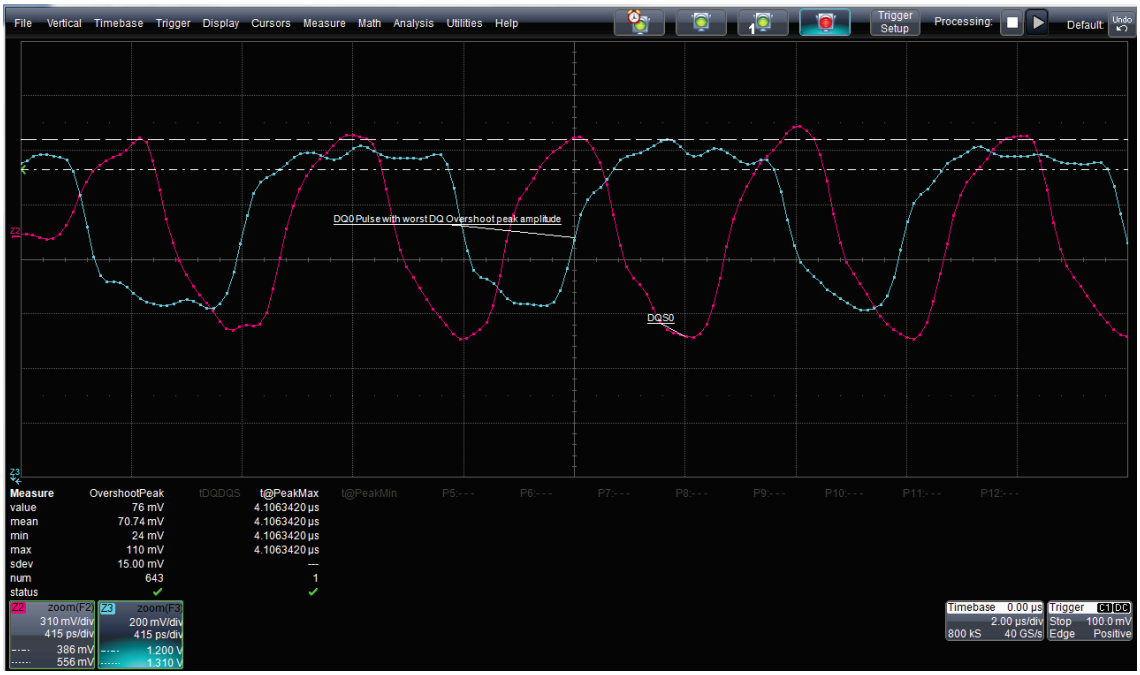


Figure 18. Oscilloscope configuration after Overshoot Peak Amplitude test.

Shown on the screen:

- Z2 is a zoom of F2, the acquired DQS signal after any probe deskew has been applied. The zoom is positioned at the location of the "worst case" Overshoot Peak Amplitude measurement indicated by t@PeakMax. This signal is not measured in this test and is only provided as a visual reference.
- Z3 is a zoom of F3, the acquired DQ signal after any probe deskew has been applied. The zoom is position at the location of the "worst case" Overshoot Peak Amplitude measurement indicated by t@PeakMax. A trace label is applied on the pulse with the worst overshoot peak amplitude. This is the signal which is measured in this test.

In the Measure table:

- OvershootPeak (P1) is measuring the overshoot peak amplitude above VDDQ for of each DQ pulse. The VDDQ level is indicated by alternating dashed cursor and the peak amplitude level is indicator by the other cursor. The peak amplitude is measured only 1 UI after a transition. If the peak value does not exceed VDDQ the measured value will return a negative result. The maximum value is the measured value for DQ Overshoot peak amplitude Max. This test is considered passing if the measured value is less than 400 mV.
- t@PeakMax (P3) displays the location of where the maximum value of OvershootPeak occurred. This is used to position the zoom traces at the location of the "worst case results".

DQS
This test measures the overshoot/undershoot, peak and area measurements on single-ended DQS_t and DQS_c signals, using the methodology described above:

- VDOSP: Maximum peak amplitude above VDOS
- VDUSP: Maximum peak amplitude below VDUS
- ADOS1: Maximum overshoot area per 1 UI between VDDQ and VDOS
- ADOS2: Maximum overshoot area per 1 UI above VDOS
- ADUS1: Maximum undershoot area per 1 UI between VSSQ and VDUS1
- ADUS2: Maximum undershoot area per 1 UI below VDUS

CK
This test measures the overshoot/undershoot, peak and area measurements on single-ended CK_t and CK_c signals, using the methodology described above:

- VCOSP: Maximum peak amplitude above VCOS
- VCUS: Maximum peak amplitude allowed for undershoot
- ACOS1: Maximum overshoot area per 1 UI between VDD and VDOS
- ACOS2: Maximum overshoot area per 1 UI above VCOS
- ACUS: Maximum undershoot area per 1 UI below VSS

CA/ADDR
This test measures the overshoot/undershoot, peak and area measurements on single-ended Command and Address signals, using the methodology described above:

- VAOSP: Maximum peak amplitude above VAOS
- VAUS: Maximum peak amplitude allowed for undershoot
- AAOS1: Maximum overshoot area per 1 tCK between VDD and VAOS
- AAOS2: Maximum overshoot area per 1 tCK above VDOS
- AAUS: Maximum undershoot area per 1 tCK below VSS

Differential Amplitude and Levels: Vindiff, VIHdiff, VILdiff (LPDDR4 only)

Vindiff (CK or DQS)
The minimum differential voltage input (peak to peak) needed to satisfy the JEDEC requirement for input receiver voltage is measured as Vindiff. The JEDEC specification sets out minimum pk-pk voltage ranges based on the signal's data rate and type. A (Max Peak Voltage – Minimum Peak Voltage) is performed and reported against all test pulses, and if any differential signal is below the accepted limit, the test is reported as a failure.

VIHdiff (CK or DQS)
The differential input voltage for the CK or DQS is defined as the High point. This value is measured to the JEDEC standard and used for making differential slewrate measurements.

VILdiff (CK or DQS)
The differential input voltage for the CK or DQS is defined as the Low point. This value is measured to the JEDEC standard and used for making differential slewrate measurements.

Single-ended Tests: Vinse

The Voltage Input Single-Ended test measures both the high limit and low limit in reference to the VrefDQ level.

CK_t, CK_c (DDR4 and LPDDR4/4X)

This measurement of the signal amplitude confirms no packets of the Clock (CK_t or CK_c) are outside their JEDEC defined limits.

DQS_t, DQS_c (LPDDR4/4X only)

This measurement of the signal amplitude confirms no packets of the Strobe (DQS_t or DQS_c) are outside their JEDEC defined limits.

Electrical Tests on Read Bursts (Outputs)

Output Slewrate

The purpose of these tests is to characterize the slewrate on DQ and DQS of all the Read bursts (output) in the acquisition. This test is performed on the Slewrate (SR) of the Query Output (Q) for both Single-ended (SE) and Differential (diff) setups (ie SRQse and SRQdiff). The rising and falling edges are measured against the minimum and maximum values allowed by the JEDEC standard for its corresponding speed.

Note: Only slewrate measured on the rising edge of DQ is shown below. The measurement methodology is exactly same for the falling edge, except the slewrate is measured from VOH(ac) to VOL(ac) instead of VOL(ac) to VOH(ac). The measurement methodology is also identical for DQS.

SRQse

This test measures the slewrate of the single ended DQ output signals during Read bursts. Slew is measured between VOH(AC) and VOL(AC). Both the max and min values are measured.

At the completion of the SRQse test, the oscilloscope is in the following state:

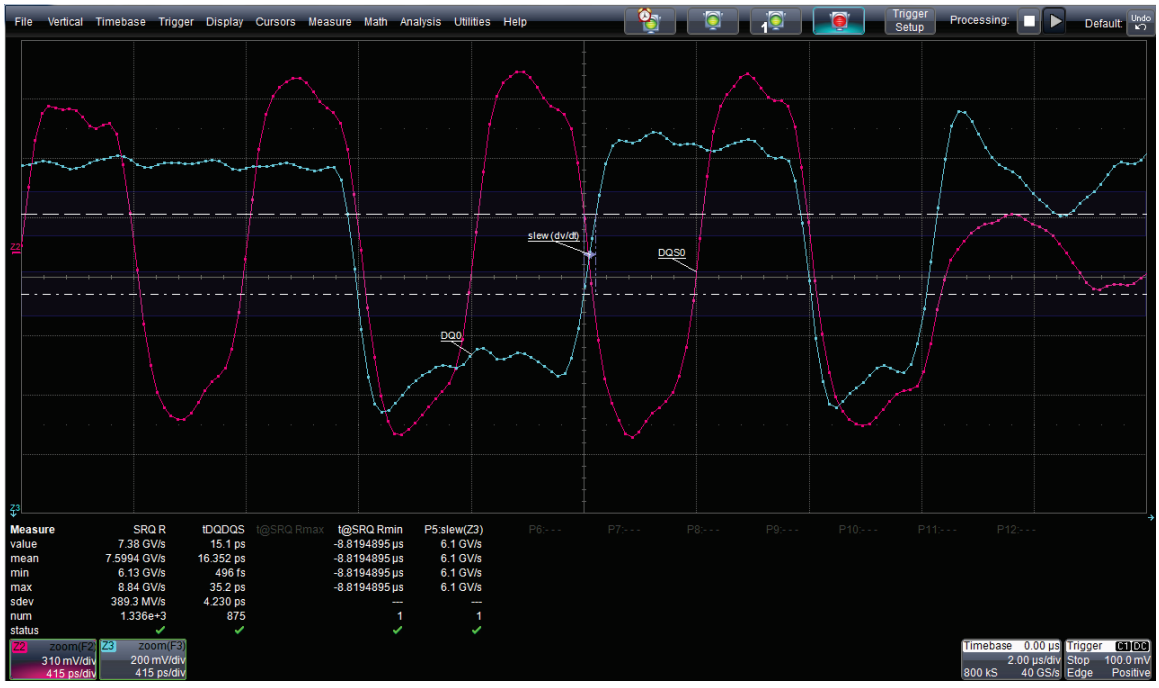


Figure 19. Oscilloscope configuration after the SRQ test.

Shown on the screen:

- Z2 is a zoom of F2, the acquired DQS signal after any probe deskew has been applied. The zoom is positioned at the location of the "worst case" SRQ R measurement indicated by t@SRQ Rmin. This signal is not measured and is only provided as a visual reference.
- Z3 is a zoom of F3, the acquired DQ signal after any probe deskew has been applied. The zoom is position at the location of the "worst case" SRQ R measurement indicated by t@SRQ Rmin. This is the signal that is measured in this test.

In the Measure table:

- SRQ R (P1) is measuring the slewrate of DQ on the rising edges. The slewrate on the rising edge is measured from VOL(ac) to VOH(ac). The minimum value is the measured value for SRQ R of DQ min. This test is passed if the measured value is greater than 4 GV/s.
- tDQDQS (P2) is measuring the skew between DQ and DQS. Since this measurement is performed once per burst, this shows how many Read bursts were in the acquired waveform.
- t@SRQ Rmin (P4) displays the location of where the minimum value of SRQ R occurred. This is used to position the zoom traces at the location of the "worst case results".
- P5: slew(Z3) displays the minimum value of SRQ R and is used to display the slewrate measurement markers.

R/F Ratio (LPDDR4 only)

This test measures the Output slew-rate matching Ratio (Rise to Fall) for single-ended signals, as defined by the JEDEC standard. The reference levels are the VOL(AC) = 0.2*VOH(DC) and VOH(AC) = 0.8*VOH(DC).

SRQdiff

This test measures the slewrate of the differential DQS output signals during Read bursts. Slew is measured between VOH.Diff(AC) and VOL.Diff(AC). Both the max and min values are measured.

Timing Tests on Write Bursts

Timing Tests on Bits (not using interpolation)

tDQSS (DDR4 only)

This test characterizes the allowed range for a rising DQS edge relative to CK on Write bursts. This measures the time from CK rising at Vref to the nearest DQS rising at Vref. Both the maximum and minimum values are measured. This test is very similar to tDQSCK, which is measured on Read bursts.

At the completion of the tDQSS test, the oscilloscope is in the following state:

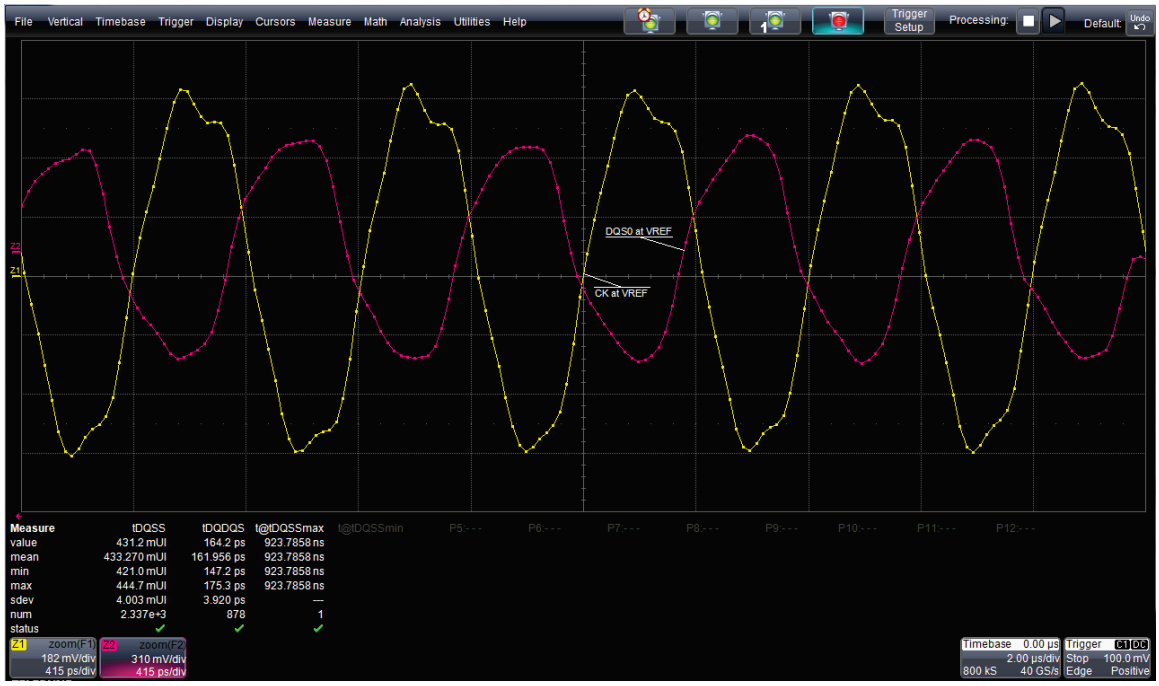


Figure 20. Oscilloscope configuration after the tDQSS test.

Shown on the screen:

- Z1 is a zoom of F1, the acquired CK signal after any probe deskew has been applied. The zoom is position at the location of the "worst case" tDQSS measurement indicated by t@tDQSSmax. A trace label is applied on this trace at Vref.
- Z2 is a zoom of F2, the acquired DQS signal after any probe deskew has been applied. The zoom is positioned at the location of the "worst case" tDQSS measurement indicated by t@tDQSSmax. A trace label is applied at Vref on this trace according to the signal name assigned to DQS.

In the Measure table:

- tDQSS (P1) is measuring the skew between CK and DQS. The skew is measured between CK rising at Vref to the nearest DQS rising at Vref. Essentially the time between the two trace labels is measured. The maximum value is the measured value for tDQSS max and is reported in mtCK(avg). This test is considered informational only since the limit is undefined.
- tDQDQS (P2) is measuring the skew between DQ and DQS. Since this measurement is performed once per burst, this shows how many Write bursts were in the acquired waveform.
- t@tDQSSmax (P3) displays the location of where the maximum value of tDQSS occurred. This is used to position the zoom traces at the location of the "worst case results".

tDQSH and tDQSL

These tests measure the high (tDQSH) and low (tDQSL) pulse widths of each DQS signal during a W burst. Both the maximum and minimum tDQSH/tDQSL values are measured. This tests are very similar to tQSH and tQSL, which are measured on Read bursts.

Note: Only tDQSH will be discussed below. The measurement methodology is the same for the tDQSL expect the measurement is made on DQS from falling edge to a rising edge instead of a rising edge to a falling edge.

At the completion of the tDQSH test, the oscilloscope is in the following state:

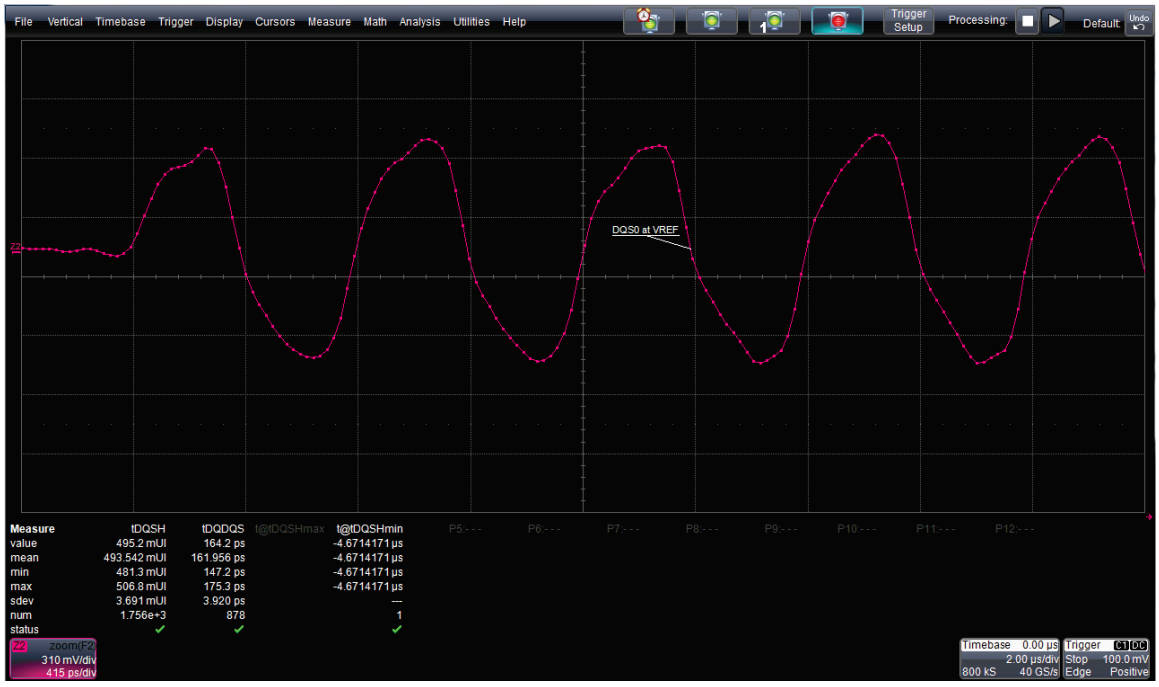


Figure 21. Oscilloscope configuration after the tDQSH test.

Shown on the screen: **Z2** is a zoom of F2, the acquired DQS signal after any probe deskew has been applied. The zoom is positioned at the location of the "worst case" tDQSH measurement indicated by t@tDQSHmin. A trace label is applied at Vref on this trace according to the signal name assigned to DQS.

In the Measure table:

- **tDQSH** (P1) is measuring the high time of DQS. The high time is determined by measuring the time DQS crosses Vref on a rising edge at to the time DQS crosses the next associated falling edge at Vref. The minimum value is the measured value for **tDQSH min** and is reported in mtCK(avg). This test is considered informational only since the limit is undefined.
- **tDQDQS** (P2) is measuring the skew between DQ and DQS. Since this measurement is performed once per burst, this shows how many Write bursts were in the acquired waveform.
- **t@tDQSHmin** (P4) displays the location of where the minimum value of tDQSH occurred. This is used to position the zoom traces at the location of the "worst case results".

TdIPW

This test measures the pulse widths of the DQ signal during the Write burst. The minimum value is measured on both high and low pulses.

At the completion of the TdIPW test, the oscilloscope is in the following state:

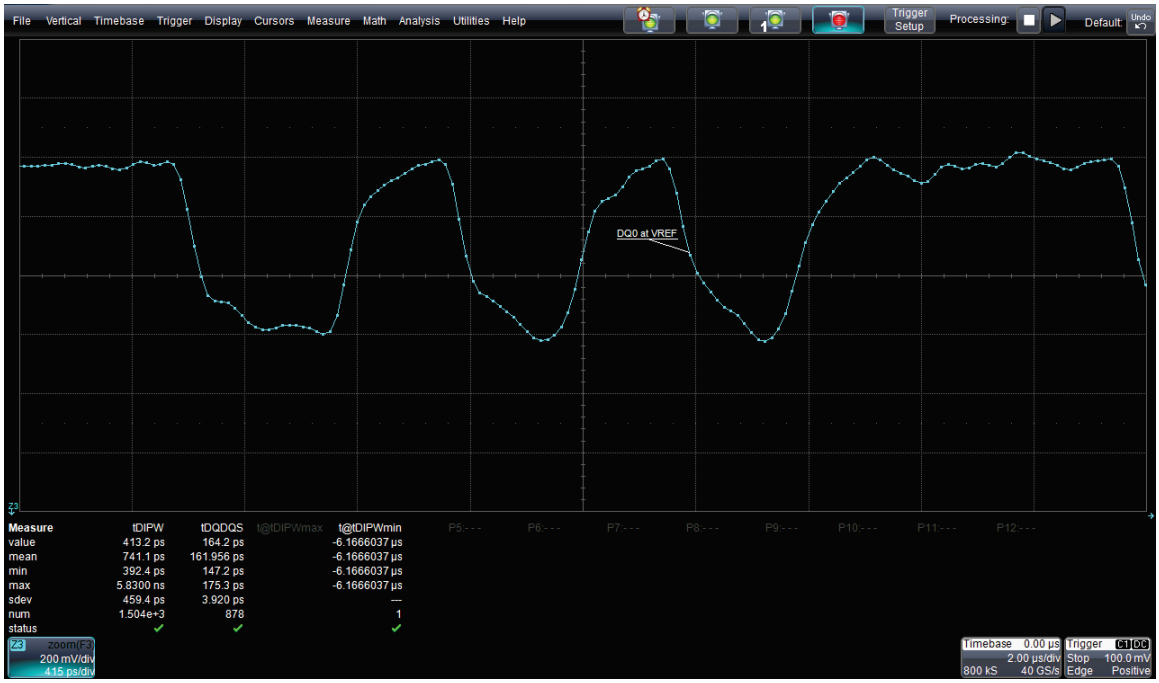


Figure 22. Oscilloscope configuration after the TdIPW test.

Shown on the screen:

- Z3 is a zoom of F3, the acquired DQ signal after any probe deskew has been applied. The zoom is positioned at the location of the "worst case" tDIPW measurement indicated by t@tDIPWmin. A trace label is applied at Vref on this trace according to the signal name assigned to DQ.

In the Measure table:

- TdIPW (P1) is the high time of DQS. The high time is determined by measuring the time DQ crosses Vref on a rising edge (centered on the screen) at to the time DQ crosses the next associated falling edge at Vref (indicated by the trace label). The minimum value is the measured value for TdIPW min High and is reported in mUI. This test is considered passing if the minimum value is greater than 0.58 UI.
- tDQDQS (P2) is the skew between DQ and DQS. Since this measurement is performed once per burst, this shows how many Write bursts were in the acquired waveform.
- t@tDIPWmin (P4) displays the location of where the minimum value of TdIPW occurred. This is used to position the zoom traces at the location of the "worst case results".

tDSS and tDSH

These tests characterize the setup and hold time for a falling DQS edge to the rising CK edge on Write bursts. The minimum value is measured for both tDSS and tDSH.

Note: Only tDSS will be discussed below. The measurement methodology is the same for the tDSH expect the hold time is measured rather than the setup time.

At the completion of the tDSS test, the oscilloscope is in the following state:

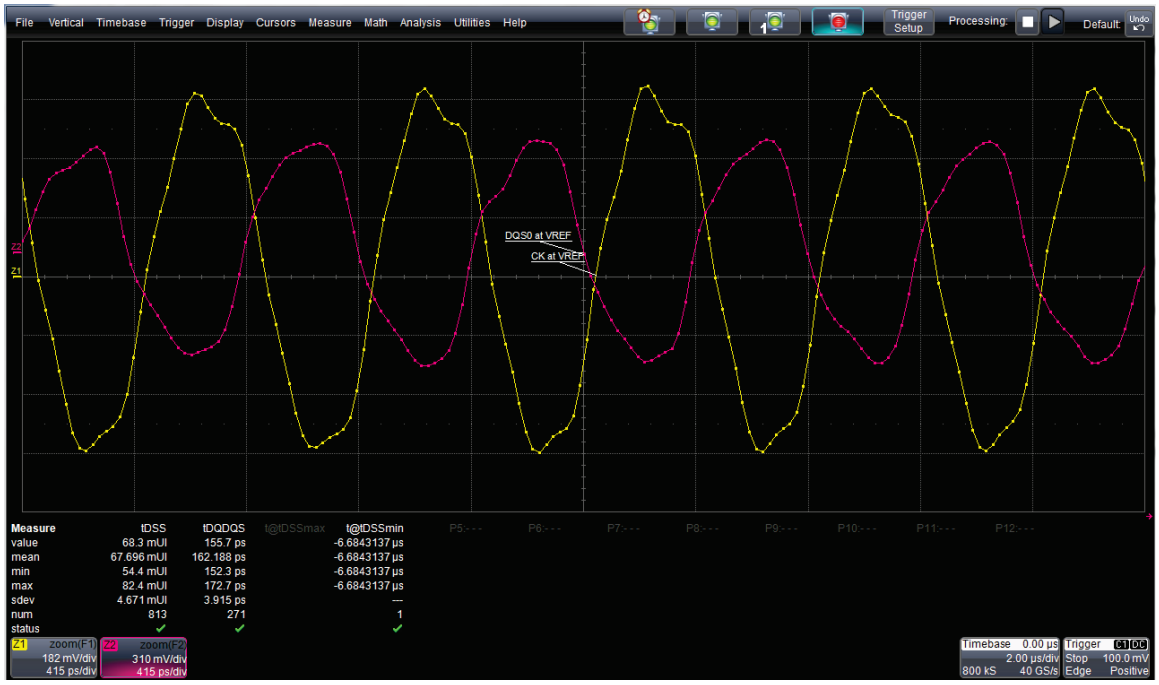


Figure 23. Oscilloscope configuration after the tDSS test.

Shown on the screen:

- Z1 is a zoom of F1, the acquired CK signal after any probe deskew has been applied. The zoom is position at the location of the "worst case" tDSS measurement indicated by t@tDSSmax. A trace label is applied on this trace at Vref.
- Z2 is a zoom of F2, the acquired DQS signal after any probe deskew has been applied. The zoom is positioned at the location of the "worst case" tDSS measurement indicated by t@tDSSmax. A trace label is applied at Vref on this trace according to the signal name assigned to DQS.

In the Measure table:

- tDSS (P1) is measuring the setup time from when the DQS falling edge crossed Vref to when the Ck rising edge crosses Vref. Essentially the time between the two trace labels is measured. The minimum value is the measured value for tDSS min and is reported in mtCK(avg). This test is considered informational only since the limit is undefined.
- tDQDQS (P2) is measuring the skew between DQ and DQS. Since this measurement is performed once per burst, this shows how many Write bursts were in the acquired waveform.
- t@tDSSmin (P4) displays the location of where the minimum value of tDSS occurred. This is used to position the zoom traces at the location of the "worst case results".

Timing Tests on CA/ADDR

tIS (base) (DDR4 only)

This test measures the setup time between a command or address line at VIL(AC) and CK_t/CK_c crossing or at CKdiff=0 V.

tIH (base) (DDR4 only)

This test measures the setup time between a command or address line at VIL(DC) and CK_t/CK_c crossing or at CKdiff=0 V.

TcIPW (LPDDR4 only)

This test measures the Command Address input pulse width in reference to the Vcent_CA (pin mid). There are different minimum pulse widths allowed by speed grade, and QPHY-DDR4 checks for this.

Timing Tests on Pre/Postamble (using interpolation)

tWPRE and tWPST

These tests characterize the Preamble and Postamble times for all Write bursts detected in the acquisition. Both tests use an interpolation algorithm to determine the point where the signal begins, which depending upon the signal shape can lead to some inaccuracies. Only tWPST is shown below.

- tWPRE measures the timing between when preamble starts (DQS comes out of idle) and where the preamble ends (DQS at Vref).
- tWPST measures the timing between when the postamble starts (DQS at Vref) and where the postamble ends (DQS begins to returns to idle).

At the completion of the tWPST test, the oscilloscope is in the following state:

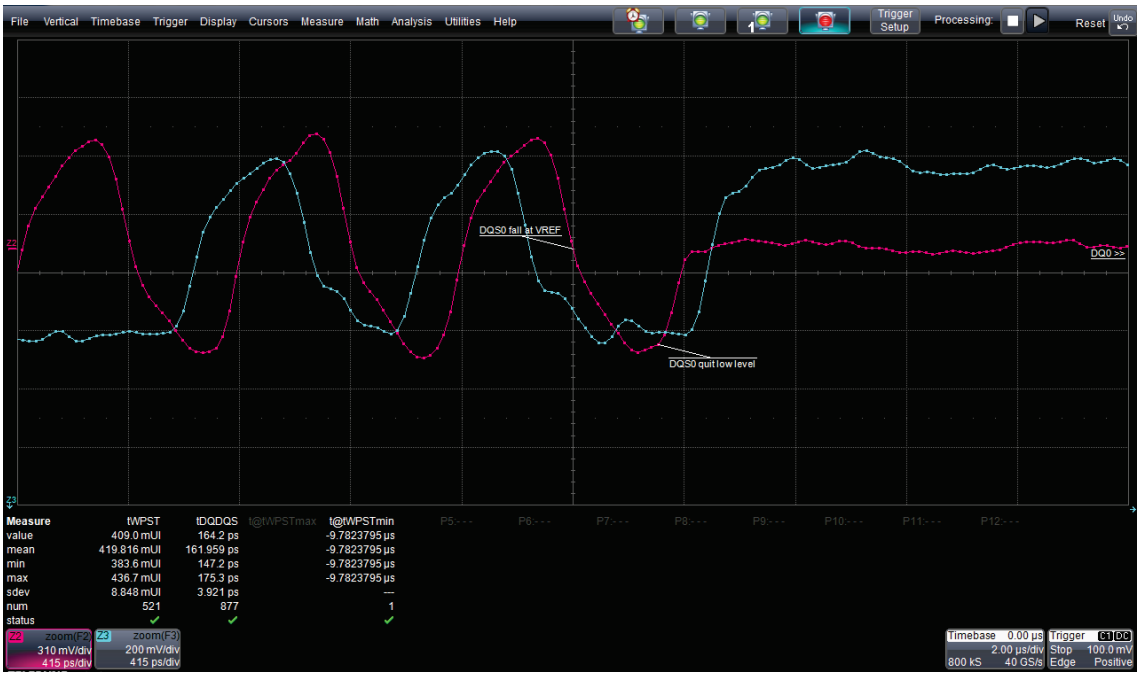


Figure 24. Oscilloscope configuration after the tWPST test.

Shown on the screen:

- Z2 is a zoom of F2, the acquired DQS signal after any probe deskew has been applied. The zoom is positioned at the location of the “worst case” tWPST measurement indicated by t@tWPSTmin. A trace label is applied to indicate where the interpolation algorithm has determined where the device is no longer driving and Vref.

In the Measure table:

- tWPST (P1) is measuring the time from DQS begins to return to idle to the last falling edge on DQS at Vref. The low level quit time found through interpolation is marked by the trace label. Essentially the time between the two trace labels is measured. The minimum value is the measured value for tWPST min reported in mtCK(avg). This test is considered informational only since the limit is undefined.
- tDQDQS (P2) is measuring the skew between DQ and DQS. Since this measurement is performed once per burst, this shows how many Write bursts were in the acquired waveform.
- t@tWPSTmin (P4) displays the location of where the minimum value of tWPST occurred. This is used to position the zoom traces at the location of the “worst case results”.

Timing Tests on Read Bursts (Outputs)

Timing Tests on Bits (not using interpolation)

tDQSQ

The tDQSQ is a timing test, defined as the total skew between the DQS crossing (DQS_t and DQS_c) and the widest DQ edge of a Read output burst (in the same DQS group). The scope software measures the maximum skew between DQS/DQ in the same DQS packet and determine if the value is within the max limit set by the JEDEC standard.

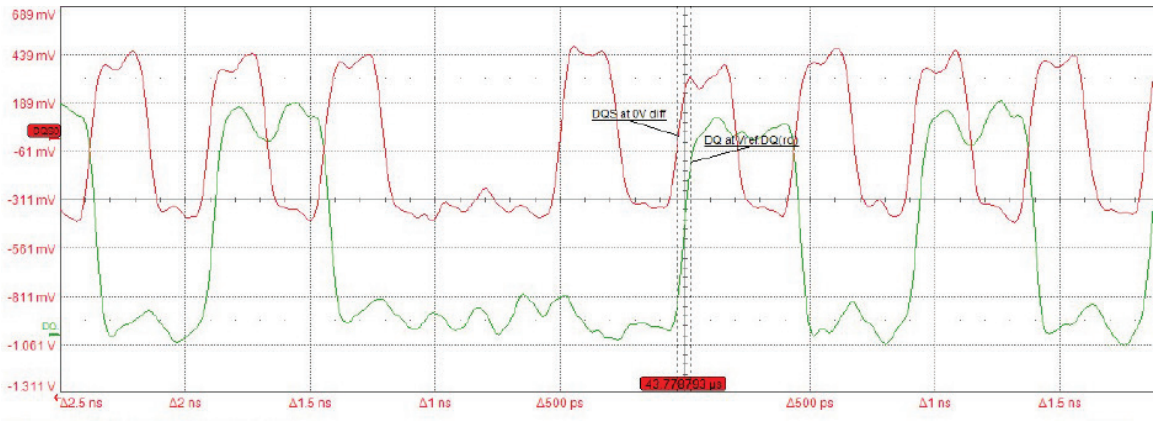


Figure 25. Oscilloscope tDQSQ test – largest DQS to DQ skew.

tQSH and tQSL

These tests measure the high time (tQSH) and low time (tQSL) for each valid DQS transition during an R burst. Both maximum and minimum tQSH/tQSL values are measured. The tests are very similar to tDQSH and tDQSL, which are measured on Write bursts. Only tQSH is shown here. The measurement methodology is the same for the tQSL except the measurement is made on DQS from falling to rising edge instead of rising to falling edge.

At the completion of the tQSH test, the oscilloscope is in the following state:

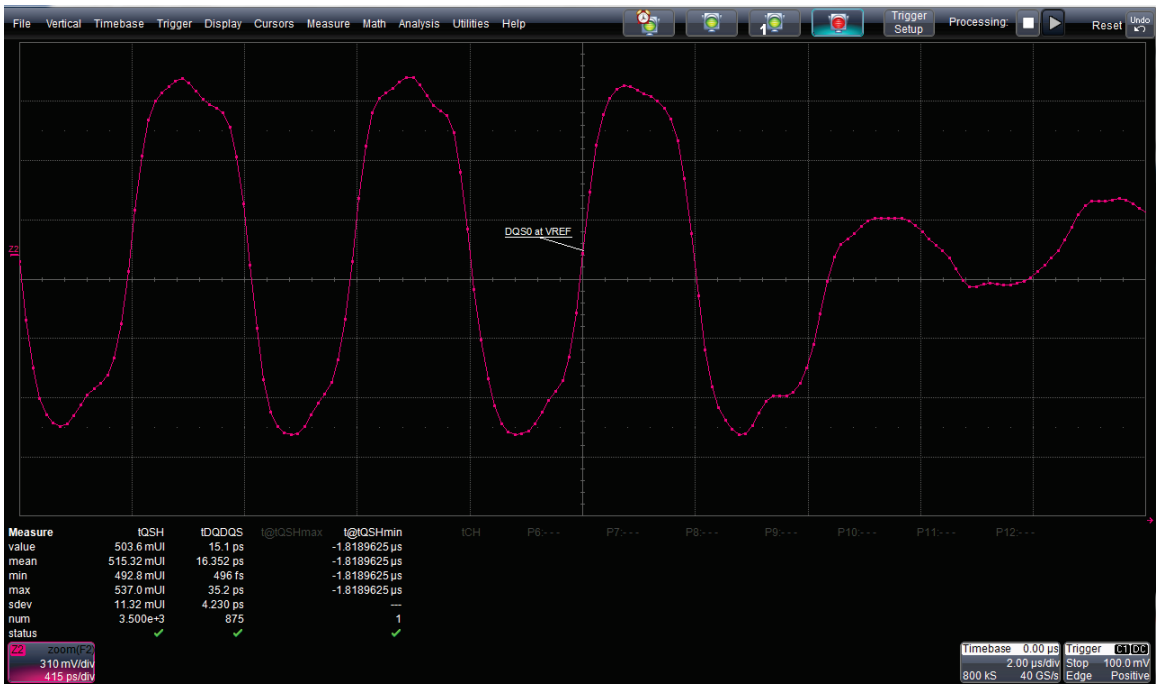


Figure 26. Oscilloscope configuration after the tQSH test.

Shown on the screen: Z2 is a zoom of F2, the acquired DQS signal after any probe deskew has been applied. The zoom is positioned at the location of the "worst case" tQSH measurement indicated by t@tQSHmin. A trace label is applied at Vref on this trace according to the signal name assigned to DQS.

In the Measure table:

- tQSH (P1) is measuring the high time of DQS. The high time is determined by measuring the time DQS crosses Vref on a rising edge at to the time DQS crosses the next associated falling edge at Vref. The minimum value is the measured value for tQSH min reported in mUI. This test is considered informational only since the limit is undefined.
- tDQDQS (P2) is measuring the skew between DQ and DQS. Since this measurement is performed once per burst, this shows how many Read bursts were in the acquired waveform.
- t@tQSHmin (P4) displays the location of where the minimum value of tQSH occurred. This is used to position the zoom traces at the location of the "worst case results".

tQH

The purpose of this test is to characterize the earliest invalid transition of DQ. This measures the minimum time from DQS at Vref to the next DQ transition at Vref.

At the completion of the tQH_total test, the oscilloscope is in the following state:

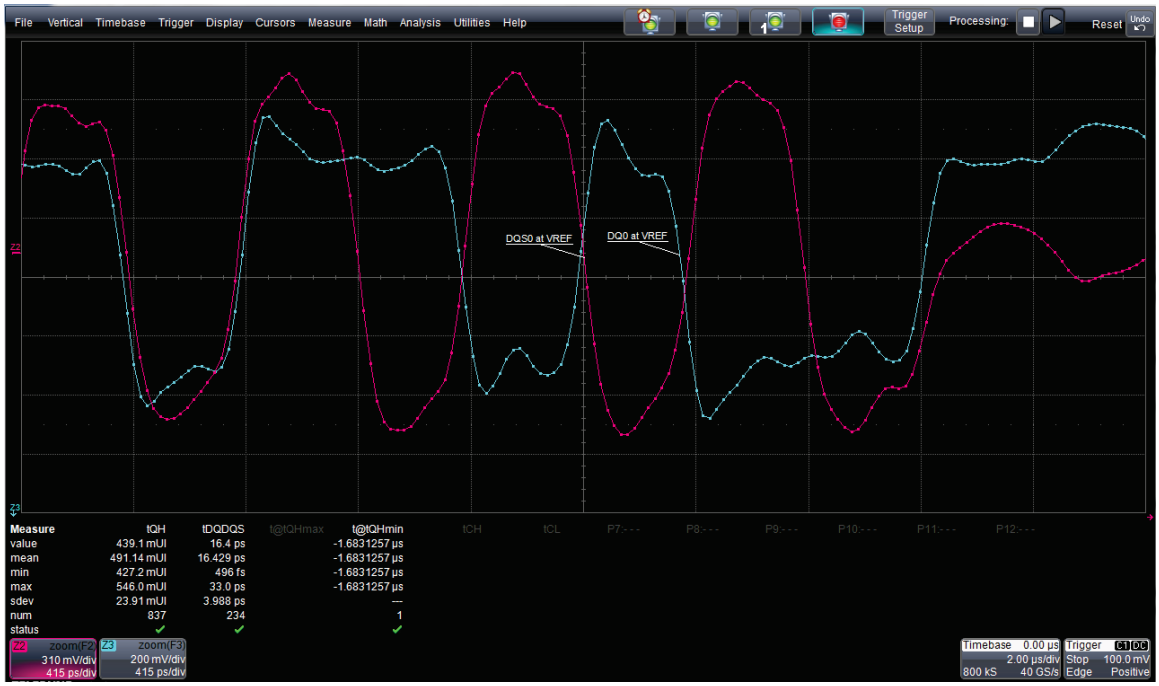


Figure 27. Oscilloscope configuration after the tQH_total test.

Shown on the screen:

- Z2 is a zoom of F2, the acquired DQS signal after any probe deskew has been applied. The zoom is positioned at the location of the "worst case" tQH measurement indicated by t@tQHmin. A trace label is applied at Vref on this trace according to the signal name assigned to DQS.
- Z3 is a zoom of F3, the acquired DQ signal after any probe deskew has been applied. The zoom is position at the location of the "worst case" tQH measurement indicated by t@tQHmin. A trace label is applied at Vref on this trace according to the signal name assigned to DQ.

In the Measure table:

- tQH (P1) is measuring the hold time of DQ. The hold time is determined by measuring the time from **DQS at Vref to the next DQ transition at Vref**. Essentially the time between the two trace labels is measured. The minimum value is the measured value for tQH_total Min reported in mUI. This test is considered informational only since the limit is undefined.
- tDQDQS (P2) is measuring the skew between DQ and DQS. Since this measurement is performed once per burst, this shows how many Read bursts were in the acquired waveform.
- t@tQHmin (P4) displays the location of where the minimum value of tQH occurred. This is used to position the zoom traces at the location of the "worst case results".

tDQSCK (DDR4 only)

The purpose of this test is to characterize the allowed range for a rising data strobe edge relative to CK on Read bursts. This measures the time from CK rising at Vref to the nearest DQS rising at Vref. Both the maximum and minimum values are measured. This test is very similar to tDQSS, which is measured on Write bursts.

At the completion of the tDQSCK test, the oscilloscope is in the following state:

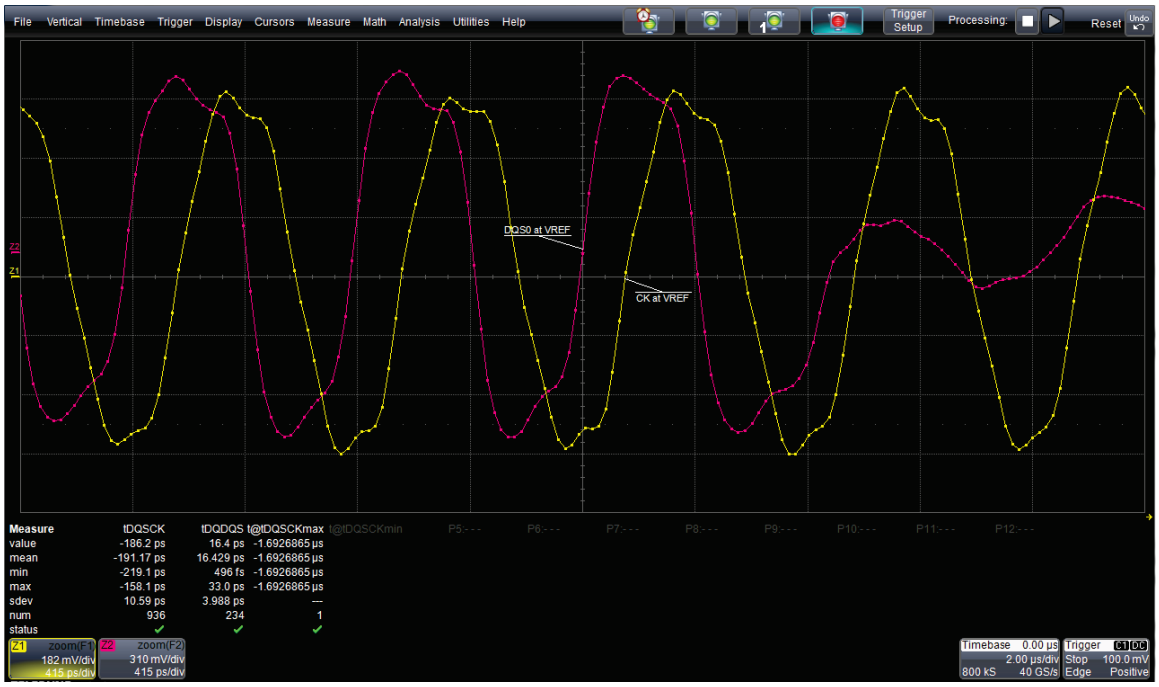


Figure 28. Oscilloscope configuration after the tDQSCK test.

Shown on the screen:

- Z1 is a zoom of F1, the acquired CK signal after any probe deskew has been applied. The zoom is position at the location of the "worst case" tDQSCK measurement indicated by t@tDQSCKmax. A trace label is applied on this trace at Vref.
- Z2 is a zoom of F2, the acquired DQS signal after any probe deskew has been applied. The zoom is positioned at the location of the "worst case" tDQSCK measurement indicated by t@tDQSCKmax. A trace label is applied at Vref on this trace according to the signal name assigned to DQS.

In the Measure table:

- tDQSCK (P1) is measuring the skew between CK and DQS. The skew is measured between **CK rising at Vref to the nearest DQS rising at Vref**. Essentially the time between the two trace labels is measured. The maximum value is the measured value for tDQSCK max. This test is considered informational only since the limit is undefined.
- tDQDQS (P2) is measuring the skew between DQ and DQS. Since this measurement is performed once per burst, this shows how many Read bursts were in the acquired waveform.
- t@tDQSCKmax (P4) displays the location of where the minimum value of tDQSCK occurred. This is used to position the zoom traces at the location of the "worst case results".

Timing Tests on Pre/Postamble (using interpolation)

tHZ(DQ) and tLZ(DQ), tHZ(DQS) and tLZ(DQS) (DDR4 only)

The purpose of these tests is to characterize the High and Low Impedance times. These tests measure the timing between when the device quits driving (tHZ) or begins driving (tLZ) and the CK at Vref. All tests use an interpolation algorithm to determine the point where the signal begins and depending upon the signal shape this can lead to some inaccuracies. Only tHZ(DQ) is shown below.

- tHZ(DQ) and tHZ(DQS) test the maximum time from when DQ/DQS quits driving to CK.
- tLZ(DQ) and tLZ(DQS) test both minimum and maximum time from when DQ/DQS begins driving to CK.

At the completion of the tHZ(DQ) test, the oscilloscope is in the following state:

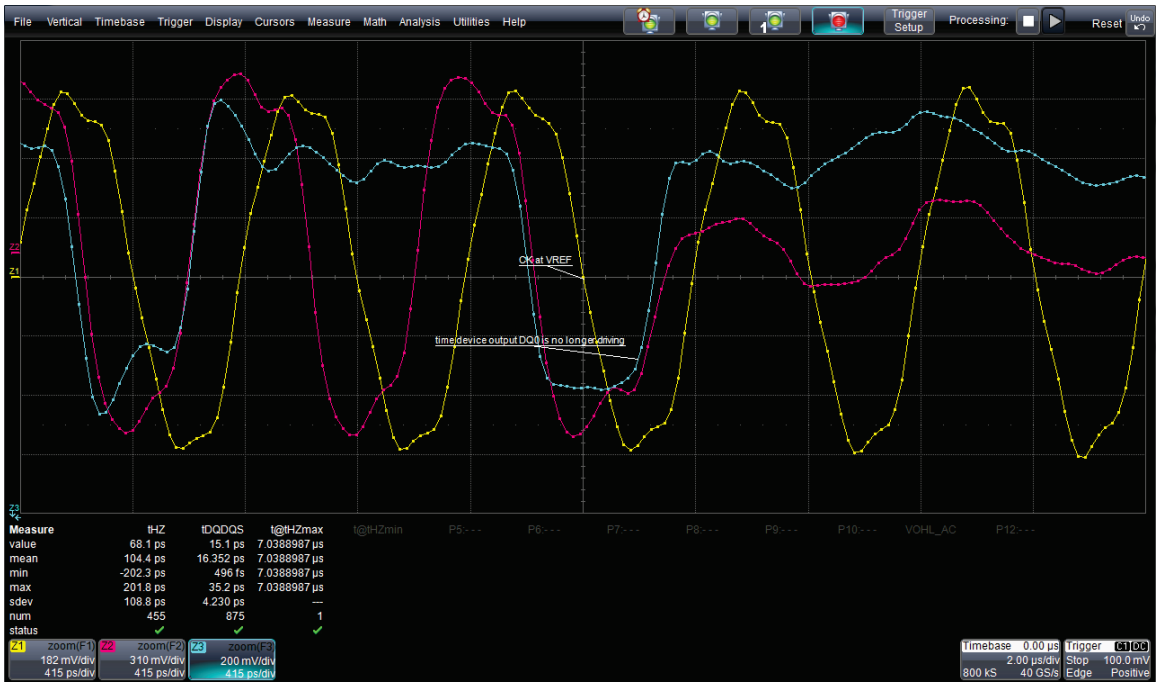


Figure 29. Oscilloscope configuration after the tHZ(DQ) test.

Shown on the screen:

- Z1 is a zoom of F1, the acquired CK signal after any probe deskew has been applied. The zoom is position at the location of the "worst case" tHZ measurement indicated by t@tHZmax. A trace label is applied on this trace at Vref.
- Z2 is a zoom of F2, the acquired DQS signal after any probe deskew has been applied. The zoom is positioned at the location of the "worst case" tHZ measurement indicated by t@tHZmax. This signal is not measured in this test and is only provided as a visual reference.
- Z3 is a zoom of F3, the acquired DQ signal after any probe deskew has been applied. The zoom is position at the location of the "worst case" tHZ measurement indicated by t@tHZmax. A trace label is applied on this trace according to the signal name assigned to DQ to indicate where the interpolation algorithm has determined where the device is no longer driving. This is the signal measured in this test.

In the Measure table:

- tHZ (P1) is measuring the time from CK at Vref to the time DQ quits driving. This time is indicated by the trace label which is found through interpolation. Essentially the time between the two trace labels is measured. The maximum value is the measured value for tHZ(DQ) max. This test is considered informational only since the limit is undefined.
- tDQDQS (P2) is measuring the skew between DQ and DQS. Since this measurement is performed once per burst, this shows how many Read bursts were in the acquired waveform.
- t@tHZmax (P3) displays the location of where the maximum value of tHZ occurred. This is used to position the zoom traces at the location of the “worst case results”.

tRPRE and tRPST

The purpose of these tests is to characterize the Preamble and Postamble times for all Read bursts detected in the acquisition. Both tests use an interpolation algorithm to determine the point where the signal begins, which depending upon the signal shape can lead to some inaccuracies. Only tRPRE is shown below.

- tRPRE measures the time between the preamble start (DQS comes out of idle) and end (DQS at Vref).
- tRPST measures the time between the postamble starts (DQS at Vref) and end (DQS begins return to idle).

At the completion of the tRPRE test, the oscilloscope is in the following state:

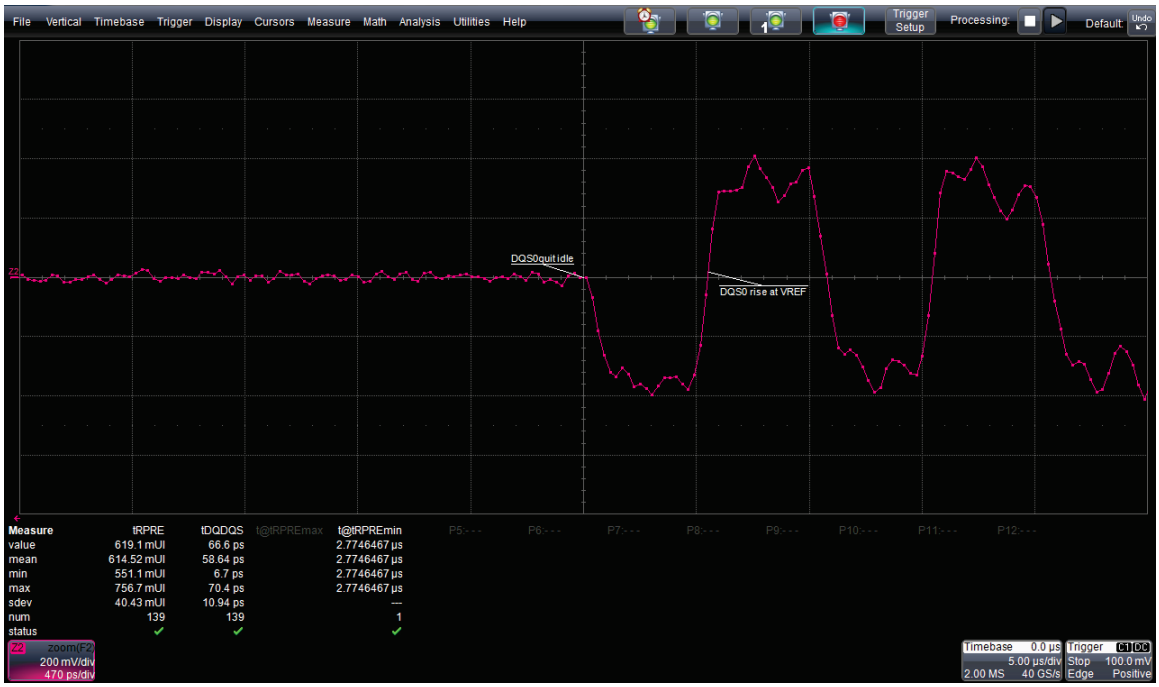


Figure 30. Oscilloscope configuration after the tRPRE test.

Shown on the screen: Z2 is a zoom of F2, the acquired DQS signal after any probe deskew has been applied. The zoom is positioned at the location of the "worst case" tRPRE measurement indicated by t@tRPREmin. A trace label is applied on this trace according to the signal name assigned to DQS to indicate where the interpolation algorithm has determined where the device is no longer idle and Vref.

In the Measure table:

- tRPRE (P1) is measuring the time from when time DQS quits driving to the next rising edge on DQS at Vref. The idle quit time is indicated by the trace label which is found through interpolation. Essentially the time between the two trace labels is measured. The minimum value is the measured value for tRPRE min reported in mtCK(avg). This test is considered informational only since the limit is undefined.
- tDQDQS (P2) is measuring the skew between DQ and DQS. Since this measurement is performed once per burst, this shows how many Read bursts were in the acquired waveform.
- t@tRPREmin (P4) displays the location of where the minimum value of tRPRE occurred. This is used to position the zoom traces at the location of the "worst case results".

DDR4 and LPDDR4/4X Variables

Main Settings

Speed Grade
Sets which DDR4 or LPDDR4 speed grade to use for testing. Default is DDR4-1600 and LPDDR4-1600. If Custom is selected, enter the speed in Custom Speed Grade.

Custom Speed Grade
This variable allows you to define a custom speed grade to be used. Enter a string in the format DDR4-*NNNN* or LPDDR4-*NNNN*, where NNNN is the custom speed grade.

Operating Mode
Select the probe configuration in use, Differential or Single-ended Differential.

Script Execution Variables

Read/Write Postamble
For each type of burst, select whether the burst contains postamble of 0.5 tCK or 1.5 tCK length.

Read/Write Burst Separation Method
Specifies whether to use the phase difference between DQ and DQS analog signals or HDA125 digital signals to identify and separate read and write bursts. Default is DQ/DQS.

Use previously saved deskew values?
When set to Yes, QualiPHY will use deskew values previously saved during the manual channel deskew procedure. When No, users are prompted to repeat the deskew procedure as part of the test. Default is No.

Pause after tests to review results?
When set to Yes, the script stops after each test allowing you to view the results. The setup is saved so the oscilloscope settings can be modified to allow for further debug results. Upon completion of debugging, testing can be seamlessly resumed with one click of a button. Default is No.

Prompt before signal acquisition?
Enables/disables a prompt at the beginning of the signal acquisition sequence. This will allow generation of read/write bursts at the start of the acquisition or modify the trigger conditions before signal acquisition. The default value for this variable is No.

Disable connection diagrams?
Disables/enables the display of connection diagrams when probe/cable setups require a change. When No, tests are stopped while the diagrams are displayed; when Yes, diagrams are disabled. Default is No.

Signal Settings

These variables give you control over the signals included in the tests.

CK(diff)?

Select "Yes" to include a CK(diff) signal in the set of signals to test.

DQ and DQS(diff)?

Select "Yes" to include DQ and DQS(diff) signals in the set of signals to test.

CA/ADDR?

Select "Yes" to include a Command/Address line in the set of signals to test.

DQS_t and DQS_c (single-ended)?

Select "Yes" to include single-ended DQS signals in the set of signals to test.

CK_t and CK_c (single-ended)?

Select "Yes" to include single-ended clock signals (CK_t, CK_c) in the set of signals to test.

Analog Signal Channel Assignments

<Signal> Input Channel

For each analog signal (CK_c, CK_t, CK(differential), etc.), select the input channel, C1-C4, to which it is connected.

HDA125 Digital Signal Assignments

These variables assign different signals and properties to the digital lines.

<Signal> Line

For each digital signal (CS_n, WE_n, RAS_n, etc.), select the HDA125 line over which it is input, or select Not Connected if it is not in use.

HDA Read Latency

Enter the number of bits from the Read Command to the start of the Read burst. This variable, along with the HDA Write Latency setting, determines what horizontal offsets to apply in order to get the correct decoding from the acquired Command Bus signals.

HDA Write Latency

Enter the number of bits from the Write Command to the start of the Write burst. This variable, along with the HDA Write Latency setting, determines what horizontal offsets to apply in order to get the correct decoding from the acquired Command Bus signals.

Default Threshold (volts)

Default logic threshold for all lines.

Individual Thresholds (volts)

For digital lines that are not using the default threshold level, enter individual thresholds in comma-delimited pairs (e.g., D0:0.5,D1:0.2,D3:-0.2).

Analog Signal Names

CMD/ADDR
Enter a name for the Command Address signals to distinguish between different pinouts. The suffix will be included in saved waveform files and in the report. Default is A0.

CK
Enter a name for the Clock signal to distinguish between different pairs. The suffix will be included in saved waveform files and in the report. Default is CK.

DQ
Enter a name for the Data signal to distinguish between different signals. The suffix will be included in saved waveform files and in the report. Default is DQ0.

DQS
Enter a name for the Strobe signal to distinguish between different signals. The suffix will be included in saved waveform files and in the report. Default is DQS0.

Analog Probe Settings
These variables allow you to specify the probe tip use for each input.

Probe Tip, <Channel *N*>
Tip installed on the probe connected to the respective channel number, C1-C4. Default is SI.

Analog Probe Location Corrections

<Channel> Probe Location Correction (ps)
Time in picoseconds to shift the waveform on the respective channel, C1-C4, *in addition to* the deskew value.

Analog Signal Channel Inversion

Invert <channel> signal?
Select "Yes" to invert the waveform on the respective channel, C1-C4. Default is No.

Digital Signal Inversion

Invert <signal>?
Select "Yes" to invert the respective digital signal (CS, WE, RAS, etc.). Default is No.

Save/Recall Waveforms

Use stored waveforms?
Select "Yes" to use previously stored waveform in the Waveform Path folder will be used.

Waveform Path
Full path to the folder in which to save waveform files, or from which to recall files when Use stored waveforms? is "Yes". When running normally, Waveform Path is the root path, with subfolders defined by the DUT name entered on the Operator dialog and the incrementing Run number. When running on stored waveforms ("Demo Mode"), waveform files are recalled from this folder.

Recalled Waveform File Index
5-digit index number of the waveform file to recall when running the script on previously stored waveforms.

Virtual Probe Setup
This group of variables enables you to apply virtual probing to the acquired signals and conduct the DDR measurements on the compensated waveforms.

Virtual Probe Control
Select the type of bursts (Read, Write or Both) to which to apply virtual probe compensation. Select Off to turn off VP compensation.

Virtual Probe Tool Selection
Select the Virtual Probe tool to use.

VP@Receiver math functions simulate the waveform at termination. Use this tool if you are seeing reflections that are too large to get good measurements. When creating the math functions, use F9-F12 for sources C1-C4, in order. Place the saved setup files in the VirtualProbe Path folder.

VirtualProbe utilizes the Virtual Probe toolkit. Use this tool if you have good models of the circuit in .s2p (single-ended) or .s4p (differential) touchstone files. When creating VP setups, use SetupA-SetupD for sources C1-C4, in order. Place the saved setup file in the VirtualProbe Path folder.

Advanced uses custom panel setups saved from a WebEditor processor to apply virtual probing to the acquired signals. When creating the processing web, output math functions F9-F12 for sources C1-C4, in order. Place the saved setup file in the VirtualProbe Path folder.

VP@Receiver Settings
These settings are applied when the Virtual Probe Tool Selection is VP@Receiver.

VP@Receiver Path
Full path to the location of the setup files for channels with VP@Receiver functions.

<channel> VP@Receiver Setup File Name
Enter the name of the setup file to be used when applying VP@Receiver to the respective channel, C1-C4. The setup file name should include the .lss extension.

VirtualProbe Settings
These settings are applied when the Virtual Probe Tool Selection is VirtualProbe or Advanced.

VirtualProbe Setup Path
Full path to the location the setup file.

VirtualProbe Setup File Name
Name of the setup file that will be used to generate all signals under test. The setup file name should include the .lss extension.

Advanced Settings

These variables are designed to give advanced users more control over the QualiPHY script.

Time per division for Acquisition

Enter the Time/div in exponential notation (e.g., 5e-3 for 5 ms/div).

Jitter BER Level

Enter the BER level used to calculate total and deterministic tJIT(per)/tJIT(cc) in SDA, this is setup as the power of 10. Default is -12.

Timing Reference Horizontal Shift (DDR4 only)

Override horizontal shift value that will shift all signals relative to the timing reference in DDR Debug Toolkit views. Enter value in seconds.

Custom Level Settings

Auto, Standard or Custom Levels

Select the type of levels to apply:

- Auto uses levels QualiPHY calculates from the top and base of the acquired waveform.
- Standard uses the levels defined by the JEDEC specification.
- Custom uses the VIH/VIL AC/DC levels defined by the custom level variables.

VDD and VDDQ Level

Enter a custom voltage level for VDD and VDDQ.

VOH(AC) Level for DQ, DQS(se)

Enter a custom voltage level for VOH(AC).

VOL(AC) Level for DQ, DQS(se)

Enter a custom voltage level for VOL(AC).

VREF.CA Level

Enter a custom voltage level for VREF.CA.

VREF.DQ Level for Writes (Inputs)

Enter a custom voltage level for VREF.DQ, Writes (Inputs).

AC Threshold

Select an AC threshold for DQ and single-ended DQS signals. This value sets the delta from VREF.DQ for many measurements.

Input DC Threshold

Enter a custom DC threshold voltage.

AC Threshold (CA)

Select an AC threshold for control, clock and address signals. This value sets the delta from VREF.CA for many measurements.

High/Low Levels Delta
Used to assist with preamble identification, it sets thesholds at + and - the selected value in the DQS signal.

DQS Read/Write Threshold (%)
Enter the hysteresis threshold for DQS read/write signals. Value is the % of the DQS peak-peak voltage.

Speed Bin Settings (DDR4 only)
Setting the correct DRAM configuration for CL, CWL and Speed Bin will allow the QPHY-DDR4 scripts to more closely alter the limits for certain measurements as outlined in the JEDEC spec. One example is tCK(avg), which derates as you change these three variables.

CL
Select a CAS Latency (CL) value (number of bits).

CWL
Select a CAS Write Latency (CWL) value (number of bits).

Speed Bin
Select the speed and memory letter associated with your DRAM. (ie. DDR4-2666T, DDR4-2666U, DDR4-2666V, DDR4-2666W)

DDR4 and LPDDR4/4X Limit Sets
The limits in use by the DDR4 tests are defined in the JEDEC DDR4 specification, JESD79-4D. The software includes limit sets for DDR4-1600, DDR4-1866, DDR4-2133, DDR4-2400, DDR4-2666, DDR4-2933 and DDR4-3200. DDR4-1600 is used by default.

The limits in use by the LPDDR4 and LPDDR4X tests are defined in the JEDEC JESD208-4D and JESD209-4-1A specifications. The software includes limit sets for LPDDR4-1600, LPDDR4-1866, LPDDR4-2133, LPDDR4-2400, LPDDR4-2666, LPDDR4-2933 and LPDDR4-3200. LPDDR4-1600 is used by default.

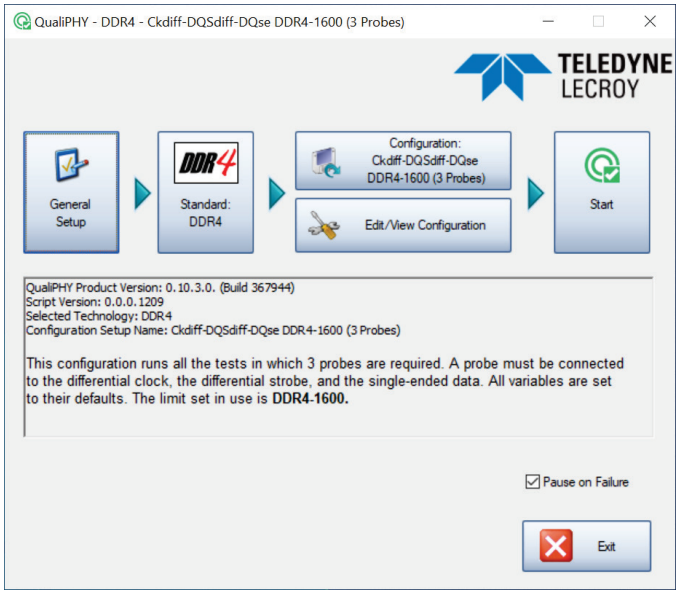
For those testing LPDDR4X, the limit sets are defined with a -D for differential or -S for single-ended configuration. It's important to know that the specification allows the signal to run only with the DQS and CK True, not the Complement portion of the signal, to conserve power when running at speeds <1600 MT/s. Configuring QualiPHY to match this is important for measurement limits.

Using QualiPHY

This section provides an overview of the QualiPHY user interface and general procedures.

QualiPHY Test Process

1. Before beginning any test or data acquisition, warm the oscilloscope for at least 20 minutes and perform any other required set up.
2. Launch the QualiPHY wizard and working from left to right, select your Standard, technology Component and test Configuration.



3. May any required settings on the Setup tab, then click Start.
4. Follow the connection diagrams/dialog prompts to connect the oscilloscope to the DUT and other test equipment. As you work, continue to follow the software prompts to change cabling, DUT output test patterns, etc. and continue.

   When all tests are successfully completed, both progress bars on the wizard dialog are completely green and the message “All tests completed successfully” appears.
5. If you have Pause on Failure checked, you’ll be prompted to restart failed tests after correcting errors.

   If problems are encountered, choose to:

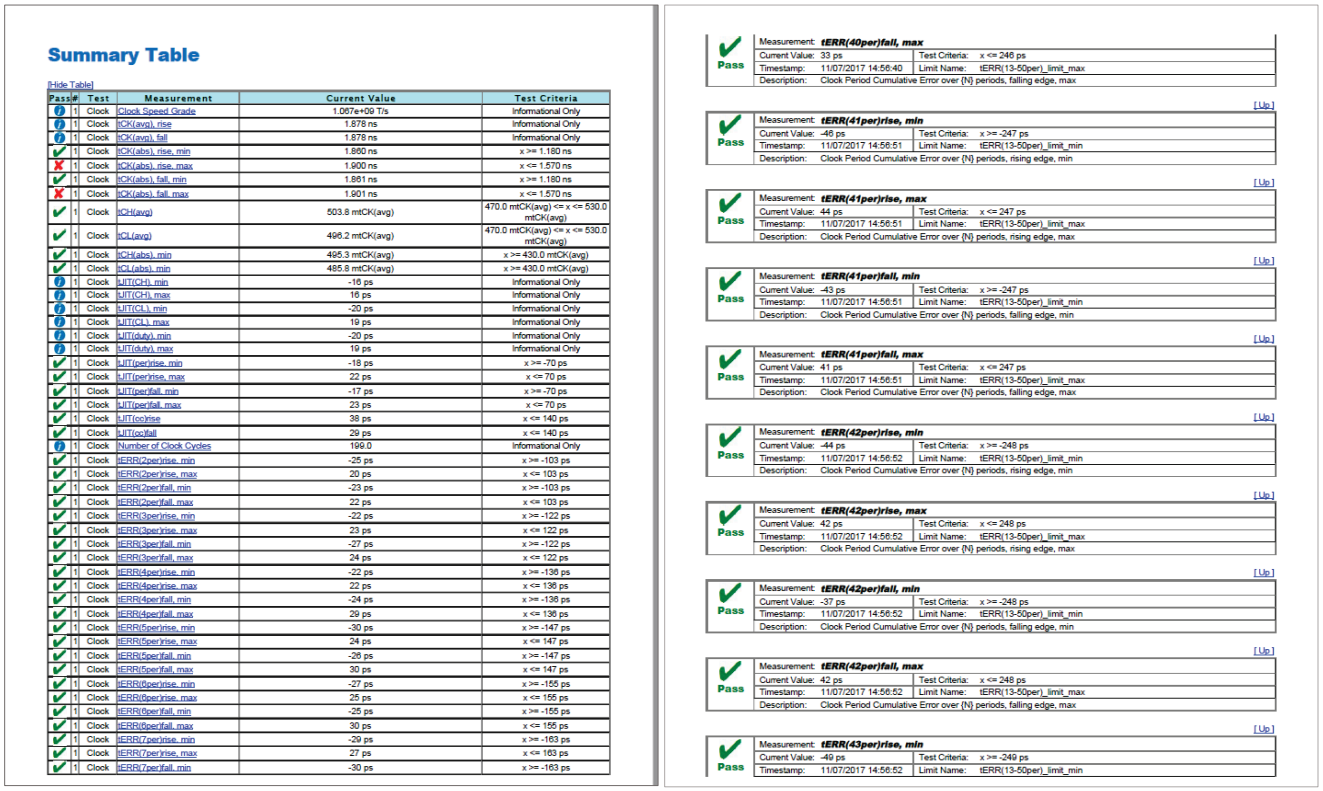
   - Retry the test from the latest established point defined in the script
   - Ignore and Continue with the next test
   - Abort Session

Generating Reports

The QualiPHY software automates report generation. On the wizard dialog, go to General Setup > Report to pre-configure reporting behavior. You can also manually launch the Report Generator from the wizard dialog after a test is completed.

The Report Generator offers the same selections as the Report tab, only applied to each report individually, rather than as a system setting. There are also options to link a custom style sheet (.xslt) to the report, or to Exclude Informative Results.

The Test Report includes a summary table with links to the detailed test result pages.



Summary Table

[Hide Table]

Pass	#	Test	Measurement	Current Value	Test Criteria
ℹ	1	Clock	Clock Speed Grade	1.067e+09 T/s	Informational Only
ℹ	1	Clock	tCK(avg), rise	1.878 ns	Informational Only
ℹ	1	Clock	tCK(avg), fall	1.878 ns	Informational Only
✔	1	Clock	tCK(abs), rise, min	1.860 ns	x >= 1.180 ns
✘	1	Clock	tCK(abs), rise, max	1.900 ns	x <= 1.570 ns
✔	1	Clock	tCK(abs), fall, min	1.861 ns	x >= 1.180 ns
✘	1	Clock	tCK(abs), fall, max	1.901 ns	x <= 1.570 ns
✔	1	Clock	tCH(avg)	503.8 mtCK(avg)	470.0 mtCK(avg) <= x <= 530.0 mtCK(avg)
✔	1	Clock	tCL(avg)	496.2 mtCK(avg)	470.0 mtCK(avg) <= x <= 530.0 mtCK(avg)
✔	1	Clock	tCH(abs), min	495.3 mtCK(avg)	x >= 430.0 mtCK(avg)
✔	1	Clock	tCL(abs), min	485.8 mtCK(avg)	x >= 430.0 mtCK(avg)
ℹ	1	Clock	tJIT(CH), min	-16 ps	Informational Only
ℹ	1	Clock	tJIT(CH), max	16 ps	Informational Only
ℹ	1	Clock	tJIT(CL), min	-20 ps	Informational Only
ℹ	1	Clock	tJIT(CL), max	19 ps	Informational Only
ℹ	1	Clock	tJIT(duty), min	-20 ps	Informational Only
ℹ	1	Clock	tJIT(duty), max	19 ps	Informational Only
✔	1	Clock	tJIT(per)rise, min	-18 ps	x >= -70 ps
✔	1	Clock	tJIT(per)rise, max	22 ps	x <= 70 ps
✔	1	Clock	tJIT(per)fall, min	-17 ps	x >= -70 ps
✔	1	Clock	tJIT(per)fall, max	23 ps	x <= 70 ps
✔	1	Clock	tJIT(cc)rise	38 ps	x <= 140 ps
✔	1	Clock	tJIT(cc)fall	29 ps	x <= 140 ps
ℹ	1	Clock	Number of Clock Cycles	199.0	Informational Only
✔	1	Clock	tERR(2per)rise, min	-25 ps	x >= -103 ps
✔	1	Clock	tERR(2per)rise, max	20 ps	x <= 103 ps
✔	1	Clock	tERR(2per)fall, min	-23 ps	x >= -103 ps
✔	1	Clock	tERR(2per)fall, max	22 ps	x <= 103 ps
✔	1	Clock	tERR(3per)rise, min	-22 ps	x >= -122 ps
✔	1	Clock	tERR(3per)rise, max	23 ps	x <= 122 ps
✔	1	Clock	tERR(3per)fall, min	-27 ps	x >= -122 ps
✔	1	Clock	tERR(3per)fall, max	24 ps	x <= 122 ps
✔	1	Clock	tERR(4per)rise, min	-22 ps	x >= -136 ps
✔	1	Clock	tERR(4per)rise, max	22 ps	x <= 136 ps
✔	1	Clock	tERR(4per)fall, min	-24 ps	x >= -136 ps
✔	1	Clock	tERR(4per)fall, max	29 ps	x <= 136 ps
✔	1	Clock	tERR(5per)rise, min	-30 ps	x >= -147 ps
✔	1	Clock	tERR(5per)rise, max	24 ps	x <= 147 ps
✔	1	Clock	tERR(5per)fall, min	-26 ps	x >= -147 ps
✔	1	Clock	tERR(5per)fall, max	30 ps	x <= 147 ps
✔	1	Clock	tERR(6per)rise, min	-27 ps	x >= -155 ps
✔	1	Clock	tERR(6per)rise, max	25 ps	x <= 155 ps
✔	1	Clock	tERR(6per)fall, min	-25 ps	x >= -155 ps
✔	1	Clock	tERR(6per)fall, max	30 ps	x <= 155 ps
✔	1	Clock	tERR(7per)rise, min	-29 ps	x >= -163 ps
✔	1	Clock	tERR(7per)rise, max	27 ps	x <= 163 ps
✔	1	Clock	tERR(7per)fall, min	-30 ps	x >= -163 ps

Pass — Measurement: **tERR(40per)fall, max** — Current Value: 33 ps — Test Criteria: x <= 246 ps — Timestamp: 11/07/2017 14:56:40 — Limit Name: tERR(13-50per)_limit_max — Description: Clock Period Cumulative Error over {N} periods, falling edge, max

[Up]

Pass — Measurement: **tERR(41per)rise, min** — Current Value: -46 ps — Test Criteria: x >= -247 ps — Timestamp: 11/07/2017 14:56:51 — Limit Name: tERR(13-50per)_limit_min — Description: Clock Period Cumulative Error over {N} periods, rising edge, min

[Up]

Pass — Measurement: **tERR(41per)rise, max** — Current Value: 44 ps — Test Criteria: x <= 247 ps — Timestamp: 11/07/2017 14:56:51 — Limit Name: tERR(13-50per)_limit_max — Description: Clock Period Cumulative Error over {N} periods, rising edge, max

[Up]

Pass — Measurement: **tERR(41per)fall, min** — Current Value: -43 ps — Test Criteria: x >= -247 ps — Timestamp: 11/07/2017 14:56:51 — Limit Name: tERR(13-50per)_limit_min — Description: Clock Period Cumulative Error over {N} periods, falling edge, min

[Up]

Pass — Measurement: **tERR(41per)fall, max** — Current Value: 41 ps — Test Criteria: x <= 247 ps — Timestamp: 11/07/2017 14:56:51 — Limit Name: tERR(13-50per)_limit_max — Description: Clock Period Cumulative Error over {N} periods, falling edge, max

[Up]

Pass — Measurement: **tERR(42per)rise, min** — Current Value: -44 ps — Test Criteria: x >= -248 ps — Timestamp: 11/07/2017 14:56:52 — Limit Name: tERR(13-50per)_limit_min — Description: Clock Period Cumulative Error over {N} periods, rising edge, min

[Up]

Pass — Measurement: **tERR(42per)rise, max** — Current Value: 42 ps — Test Criteria: x <= 248 ps — Timestamp: 11/07/2017 14:56:52 — Limit Name: tERR(13-50per)_limit_max — Description: Clock Period Cumulative Error over {N} periods, rising edge, max

[Up]

Pass — Measurement: **tERR(42per)fall, min** — Current Value: -37 ps — Test Criteria: x >= -248 ps — Timestamp: 11/07/2017 14:56:52 — Limit Name: tERR(13-50per)_limit_min — Description: Clock Period Cumulative Error over {N} periods, falling edge, min

[Up]

Pass — Measurement: **tERR(42per)fall, max** — Current Value: 42 ps — Test Criteria: x <= 248 ps — Timestamp: 11/07/2017 14:56:52 — Limit Name: tERR(13-50per)_limit_max — Description: Clock Period Cumulative Error over {N} periods, falling edge, max

[Up]

Pass — Measurement: **tERR(43per)rise, min** — Current Value: -49 ps — Test Criteria: x >= -249 ps — Timestamp: 11/07/2017 14:56:52 — Limit Name: tERR(13-50per)_limit_min

Reports are output to the folder D:\QPHY\Reports, or C:\LeCroy\QPHY\Reports if QualiPHY is installed on a remote PC.

You can add your own logo to the report by replacing the file *\QPHY\StyleSheets\CustomerLogo.jpg.

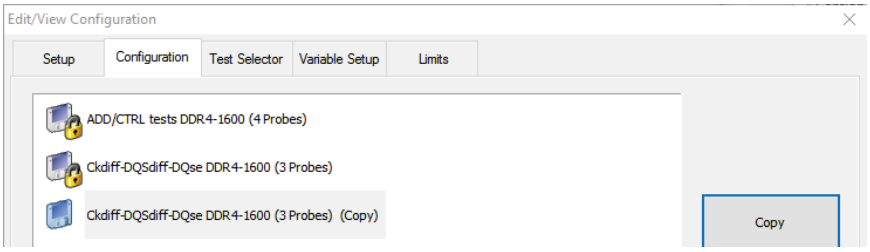
The recommended maximum size is 250x100 pixels at 72 ppi, 16.7 million colors, 24 bits. Use the same file name and format.

Customizing QualiPHY

The pre-loaded configurations cannot be modified. However, you can create your own test configurations by copying one of the pre-loaded configurations and modifying it.

Copy Configuration

1. Access the QualiPHY wizard dialog and select a **Standard**.
2. Click **Edit/View Configuration** and select the configuration upon which to base the new configuration. This can be a pre-loaded configuration or another copy.
3. Click **Copy** and enter a name and description. Once a custom configuration is defined, it appears on the Configuration tab followed by "(Copy)."

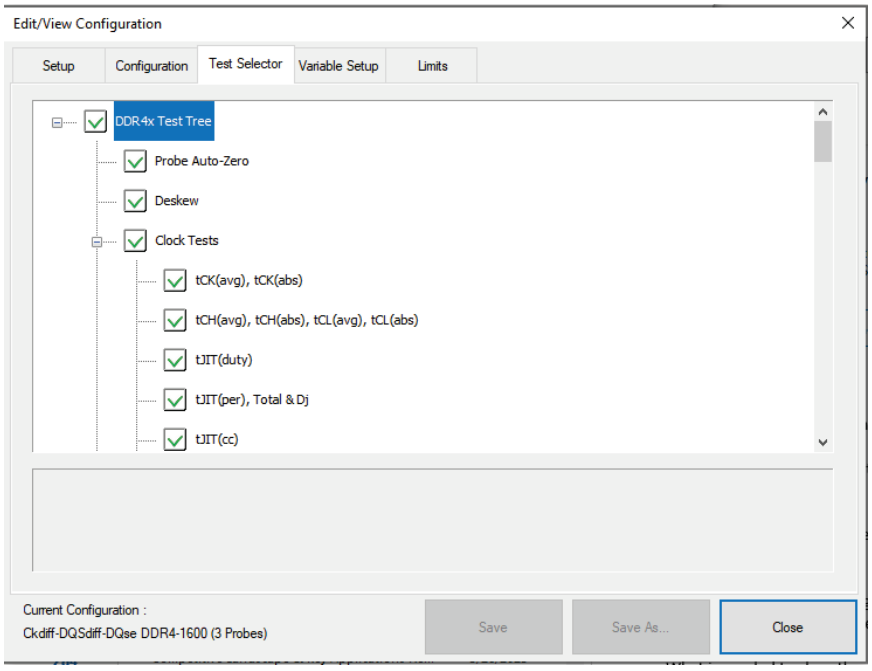


4. Select the new, custom configuration and follow the procedures below to continue making changes.

Note: If any part of a configuration is changed, the Save As button becomes active on the bottom of the dialog. If a custom configuration is changed, the Save button will also become active to apply the changes to the existing configuration, rather than create a new one.

Select Tests

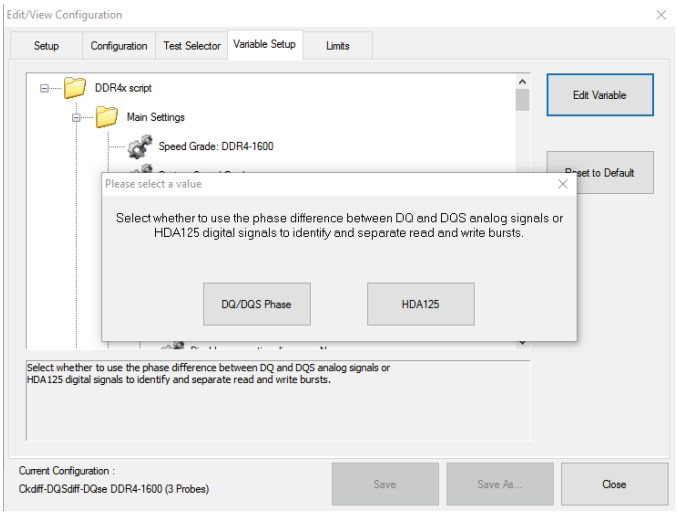
On the **Test Selector** tab, check the tests that make up the configuration. Each test is defined by the JEDEC standard. A description of each test is displayed when it is selected.



Edit Variables

The Variable Setup tab contains a list of test variables. To modify a variable:

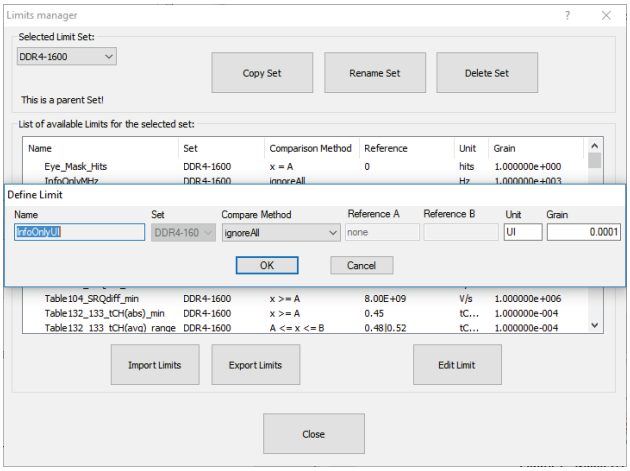
1. Select the variable on the Variable Setup tab, then click **Edit Variable**. (You can also choose to Reset to Default at any time.)
2. The conditions of this variable appear on a pop-up. Select or enter the new condition to apply.



Edit Test Limits

The Limits Manager shows the settings for every test limit in a limit set. Those in the default set are the limits defined by the standard. To create a custom limit set:

1. On the Limits tab, click **Limits Manager**.
2. With the default set selected, click **Copy Set** and enter a name for the new limit set.
3. Double click the limit to be modified, and in the pop-up enter the new values.



You can also Import Limits from a .csv file. Navigate to the file location after clicking the Import Limits button.

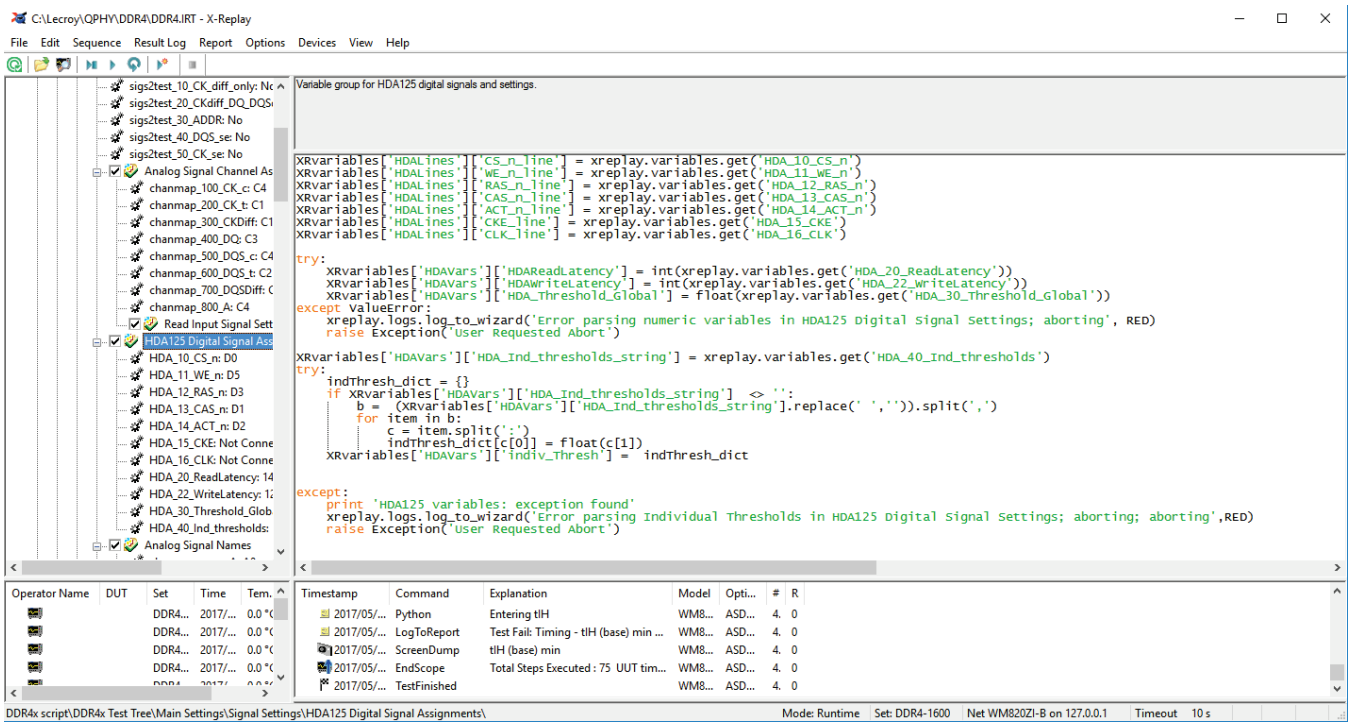
Tip: Likewise, Export Limits creates a .csv file from the current limit set. You may wish to do this and copy it to format the input .csv file.

X-Replay Mode

The X-Replay mode window is an advanced ("developer") view of QualiPHY. The tree in the upper-left frame enables you to navigate to processes in the test script, in case you need to review the code, which appears in the upper-right frame.

Two other particularly useful features are:

- A list of recent test sessions in the lower-left frame. While you can only generate a report of the current test session in the QualiPHY wizard, in X-Replay Mode you can generate a report for any of these recent sessions. Right-click on the session and choose Create Report from context menu.
- The QualiPHY log in the bottom-right frame. The frame can be split by dragging up the lower edge. The bottom half of this split frame now shows the raw Python output, which can be useful if ever the script needs debugging.



Appendix A: Virtual Probing Setup and Dependencies

Because the JEDEC electrical specifications are defined at the balls of the DDR DRAM, it is often necessary to use the virtual probing capabilities of the oscilloscope to get the best representations of the signals to be analyzed with DDR Debug Toolkit.

Also, if DDR Debug Toolkit and QPHY-DDR* are used together on the same device, it is good practice to ensure your DDR Debug virtual probing setup can also be used when you perform compliance testing using QualiPHY. QualiPHY has specific requirements for virtual probing that you will want to observe in the setup files you save and the selections you make in DDR Debug Toolkit.

The virtual probing capabilities described here become available with the installation of the SDAIII-CompleteLinQ or VirtualProbe software options.

Virtual Probing Methods

There are three methods for using virtual probing in DDR Debug Toolkit:

Method 1–Apply the VirtualProbe@Rcvr math processor to the input signals, then use the resulting math functions as inputs for DDR Debug. This math processor will apply the termination network parameters to the acquired signals.

Method 2–Use Virtual Probe software to apply S-parameter models to the input signals, then use the resulting VPOut* waveforms as inputs for DDR Debug. This method is good for using .s2p and .s4p files to deembed effects.

Method 3–Use WebEditor to apply the VirtualProbe math processor to the input signals, then use the resulting math functions as inputs for DDR Debug. This is an advanced approach that may be used to represent more complex S-parameters, such as interposer models.

Method 1–VirtualProbe@Rcvr Math Functions

The VirtualProbe@Rcvr math processor is recommended if the difference between the signal being probed and the desired signal can be defined as a simple RLC termination model with some transmission line delay, as shown in the following figure. Here, the probe point is the input (In) of the termination model and the desired signal is the output (Out) of the model.

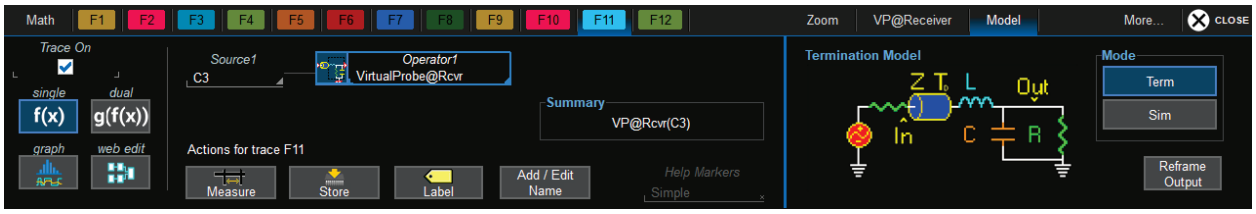
Create Math Functions

For each signal that you will analyze in DDR Debug Toolkit, apply the VirtualProbe@Rcv math processor to the acquired signals. For interoperability of DDR Debug Toolkit and QualiPHY, best practice is to use:

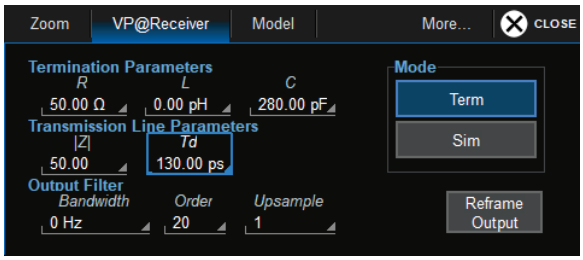
- CLK on C1 = source for F9
- DQS on C2 = source for F10
- DQ on C3 = source for F11
- Other (e.g., ADDR) on C4 = source for F12

For example, to apply the VirtualProbe@Rcv math function to DQ on C3:

1. Open the oscilloscope F11 setup dialog and choose C3 as Source1 and VirtualProbe@Rcvr as Operator1. On the Model subdialog, choose Term(ination) mode.



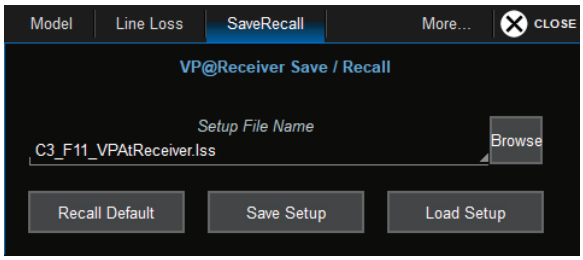
2. Open the VP@Receiver subdialog and input the termination network parameters:



For more information on using the VirtualProbe@Rcvr math processor, see the white paper.

Using the Virtual Probe at Receiver Math Operator to Eliminate Reflections

3. As you create each math function, go to the SaveRecall subdialog and Save Setup to an .lss file for each input signal.



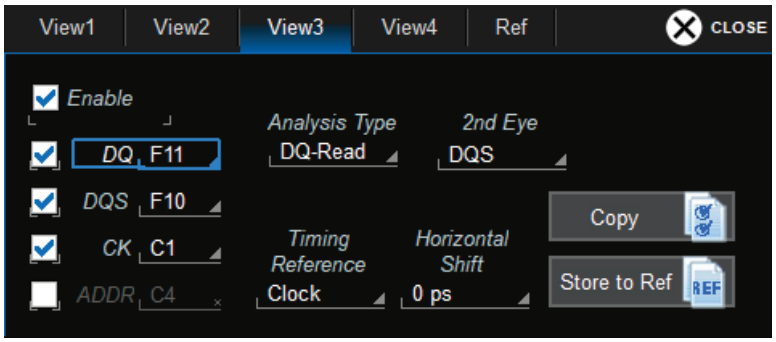
Tip: It will be easier to select files in QualiPHY if you include the input channel in the filename, for example, C3_F11_VPAtReceiver.lss.

4. Copy all files to an oscilloscope folder that QualiPHY can access. The default is D:\Applications\VPAtReceiver.

Configure DDR Debug Toolkit

When setting up your DDR Debug Toolkit Views, select the VirtualProbe@Rcvr math functions you created as the inputs for the signals, rather than the channels.

In this example, DQ is probed on C3 and DQS is probed on C2 of the oscilloscope. F11 and F10 are the VirtualProbe@Rcv math functions that were applied to the probed signals, respectively.

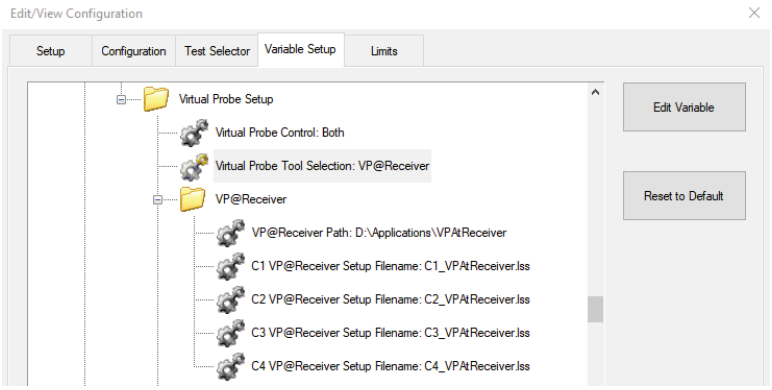


Using VirtualProbe@Rcvr with QualiPHY

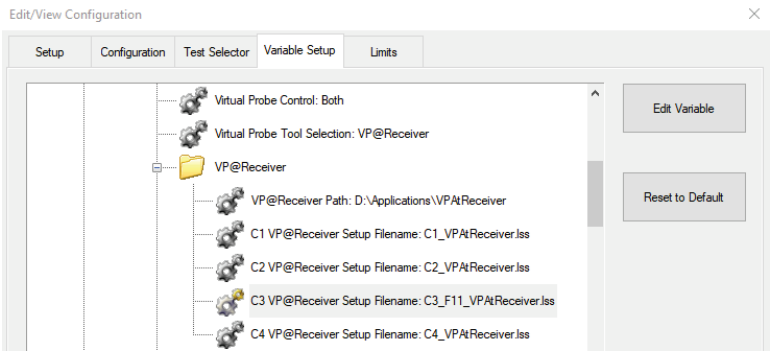
QualiPHY expects specific math functions to represent specific inputs when using the VirtualProbe@Rcvr method. When creating your math functions, use:

- C1 = Source for F9
- C2 = Source for F10
- C3 = Source for F11
- C4 = Source for F12

1. On the QualiPHY wizard, after selecting the configuration to use, choose View/Edit Configuration, then open the Variable Setup tab and:
2. Turn “Virtual Probe Control” to “Read”, “Write” or “Both” types of bursts (it is Off by default)
3. Choose “VP@Receiver” as the “Virtual Probe Tool Selection”:



4. In the VP@Receiver variable group, change:
   - "VP@Receiver Path" to the folder containing the saved setup files
   - "C*n* VP@Receiver Setup File" to the names of the files representing compensated input channels



Note: You will need to save these changes to a new configuration, which will then be ready for selection whenever you wish to apply VirtualProbe@Rcvr to this setup.

Method 2–Virtual Probe Software

The Virtual Probe method can be used if the difference between the signal being probed and the desired signal can be defined by one or more S-parameter touchstone files (.s2p for single-ended and .s4p for differential).

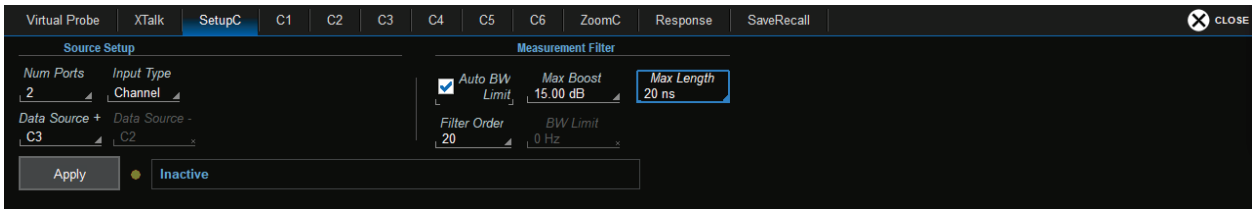
Configure Virtual Probe Setups

In the Virtual Probe software, S-parameters can be used to define multiple stages of the input/output signal flow. For interoperability of DDR Debug Toolkit and QualiPHY, best practice is to use:

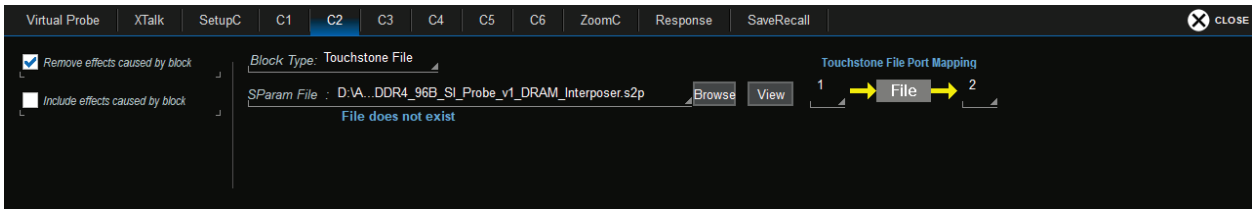
- CLK on C1 = source for SetupA
- DQS on C2 = source for SetupB
- DQ on C3 = source for SetupC
- Other (e.g., ADDR) on C4= source for SetupD

For example, to apply Virtual Probe Setup C to the DQ signal on C3:

1. Open the SetupC dialog and choose C3 as the Data Source.

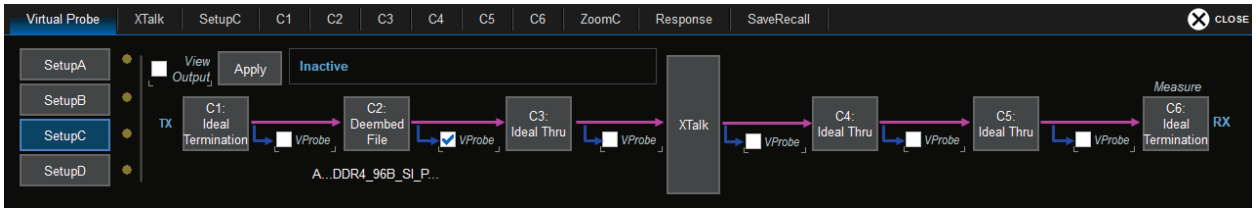


2. On the C2 dialog (or at whichever block of the circuit you wish to deembed), select "Remove effects caused by clock" and import the .s2p file representing the fixture you want deembedded (here, the interposer):

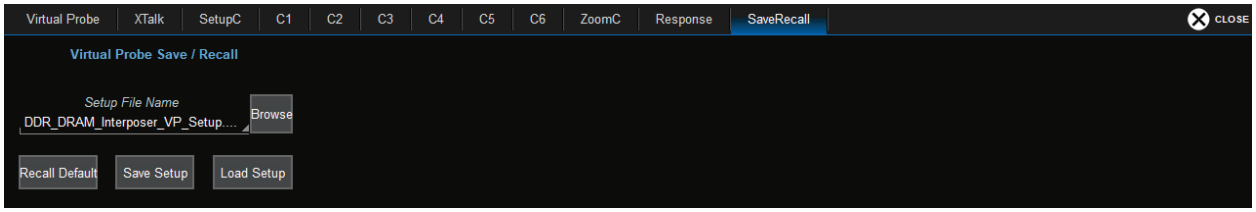


Note: In this example, C2 has nothing to do with the signal input channel, but represents the order of processing in the Virtual Probe "circuit". Setups A, B and D have similar blocks A2, B2 and D2.

3. On the Virtual Probe dialog, select block C2 (Deembed File):



4. Do the same for the other inputs that require virtual probing, following the conventions as to which Virtual Probe Setup to use for which input.
5. Open the SaveRecall dialog and save the Virtual Probe setup to an .lss file in an oscilloscope folder that QualiPHY can access. The default folder is oscilloscope D:\Applications\VirtualProbe.

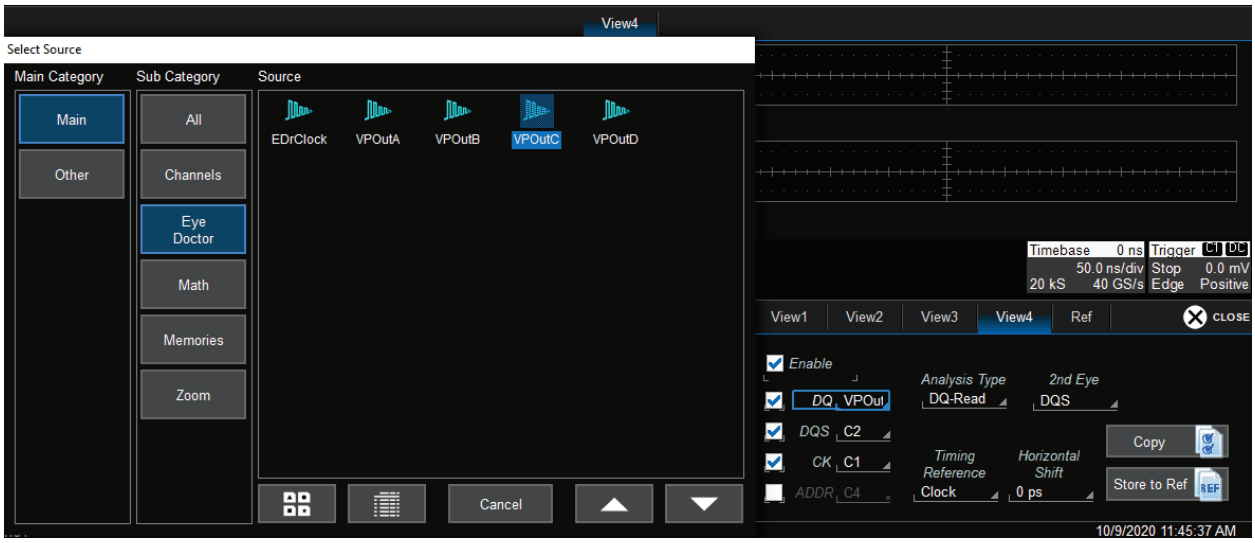


Note: With this method, there is only one setup file, vs. four setup files for the VirtualProbe@Rcvr method.

Configure DDR Debug Toolkit

Select the VPOut* waveforms corresponding to each Virtual Probe Setup you created as the inputs for DDR Debug Toolkit views. Setup A will output VPOutA, and so forth.

In the example below, the DQ signal with the interposer deembedded is represented by VPOutC, so that waveform is selected as the DQ input in DDR Debug Toolkit, rather than the probed input C3:



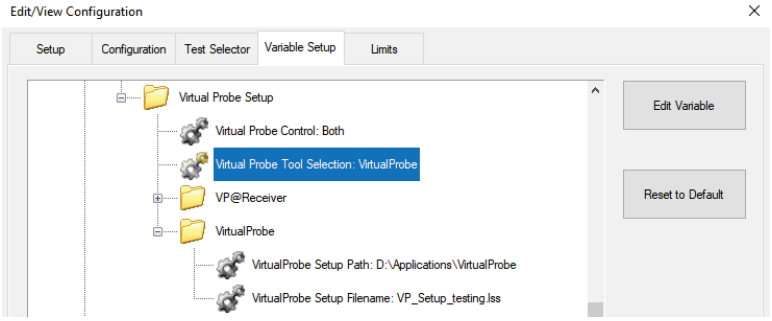
Note: VPOut* waveforms are in the Eye Doctor selector menu.

When Using Virtual Probe with QualiPHY

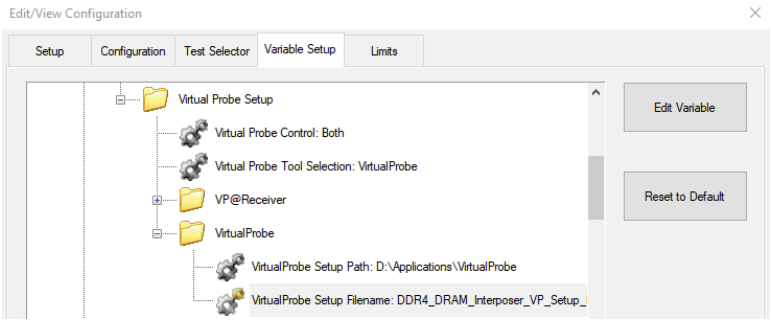
The Virtual Probe setups should correspond to the oscilloscope input channels as follows:

- C1 = Source for SetupA (VPOutA)
- C2 = Source for SetupB (VPOutB)
- C3 = Source for SetupC (VPOutC)
- C4 = Source for SetupD (VPOutD)

1. On the QualiPHY wizard, after selecting the configuration to use, choose View/Edit Configuration, then open the Variable Setup tab and:
2. Turn “Virtual Probe Control” to “Read”, “Write” or “Both” types of bursts (it is Off by default)
3. Choose “VirtualProbe” as the “Virtual Probe Tool Selection”:



4. In the VirtualProbe variable group, change:
   - “VirtualProbe Setup Path” to the full path to your setup file folder
   - “VirtualProbe Setup Filename” to the saved .lss file



Note: You will need to save these changes to a new configuration, which will then be ready for selection whenever you wish to apply Virtual Probe to this setup.

Method 3–WebEditor

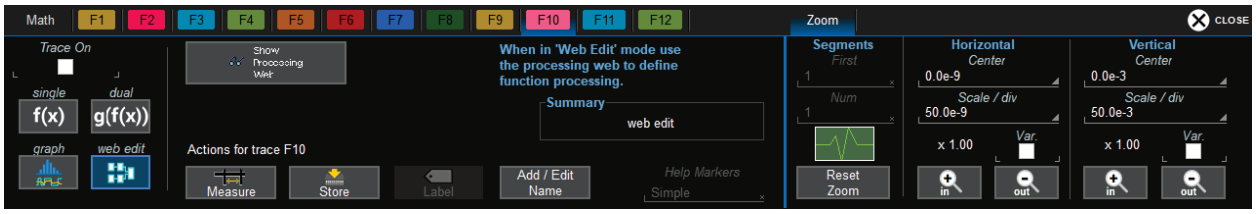
Some interposers use more sophisticated S-parameters than the 2- or 4-port models, such as .s3p and .s6p. For these cases, the netlist of the interposer can be defined using the oscilloscope WebEditor tool. The WebEditor will output math functions corresponding to the compensated channels, which will be used as inputs in DDR Debug Toolkit, similar to the VirtualProbe@Rcvr method. For interoperability of DDR Debug Toolkit and QualiPHY, best practice is to use:

- CLK on C1 = source for F9
- DQS on C2 = source for F10
- DQ on C3 = source for F11
- Other (e.g., ADDR) on C4 = source for F12

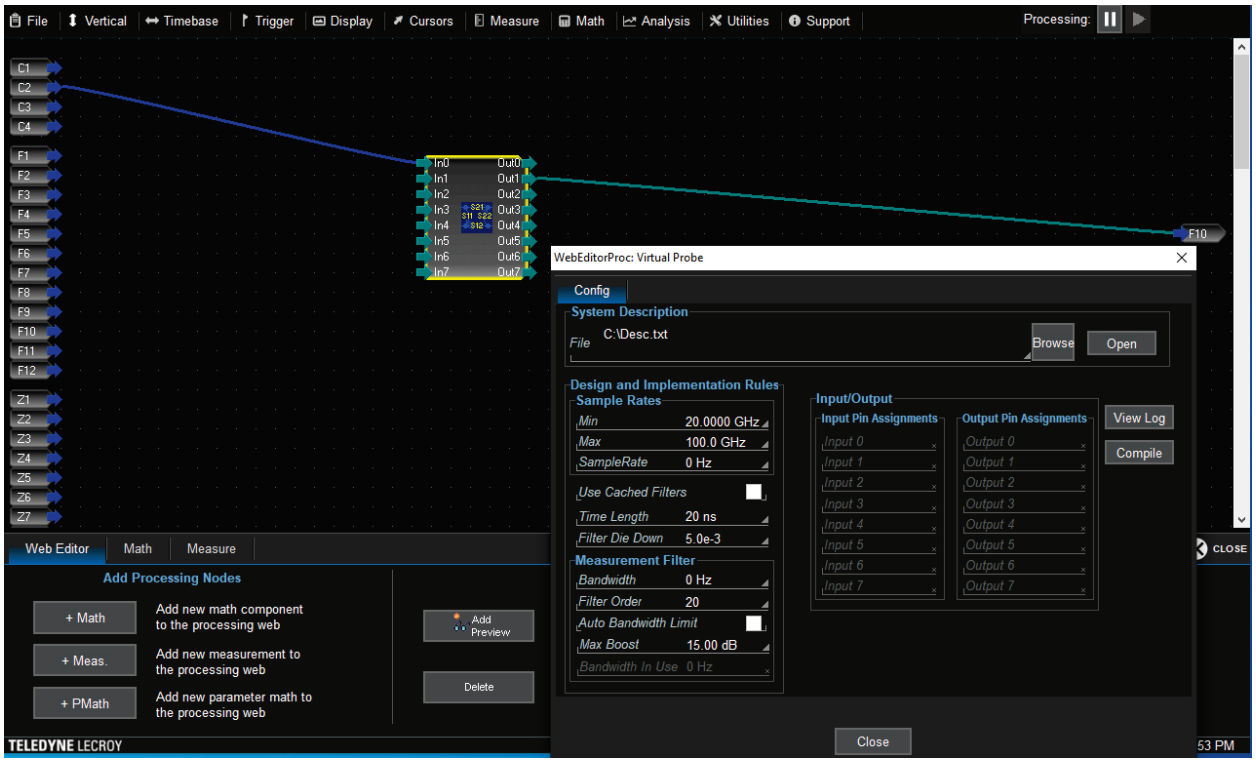
Define Netlist in WebEditor

In this example, the probed DQS and DQ signals are input on C2 and C3. These inputs will undergo the processing web to deembed the interposer from the signal.

1. To begin, open the F10 dialog and select web edit, then Show Processing Web.



This will take you to a screen like that below where you create a processing web that inputs C2 and C3, passes them through the VirtualProbe math processor, and outputs F10 and F11. The VirtualProbe processor allows you to configure the characteristics of the interposer, including applying signal filters and manually mapping input to output pins.



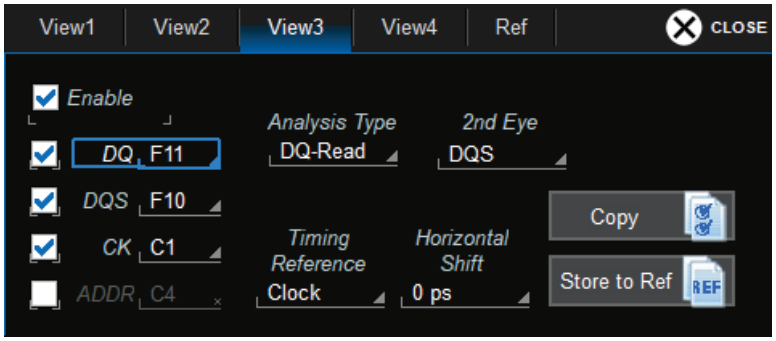
2. Do the same for C3-F11 and other inputs that require virtual probing, following the conventions below as to which math functions to use for which channels. Both F10 and F11, and any other math functions needed, can be placed on the same processing web.
3. Save the configuration to an .lss file in an oscilloscope folder where QualiPHY can access it.

Note: With this method, there is only one setup file, vs. the four setup files for VirtualProbe@Rcvr math functions.

Contact Teledyne LeCroy support for more information about creating and saving your processing web.

Configure DDR Debug Toolkit

Choose the math functions resulting from the processing web as the inputs for the DDR Debug Toolkit views:

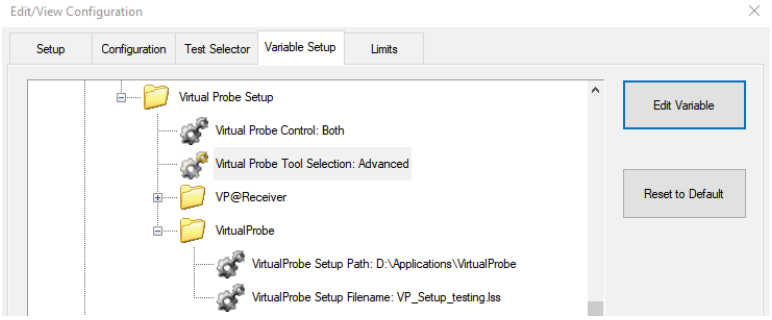


Using WebEditor with QualiPHY

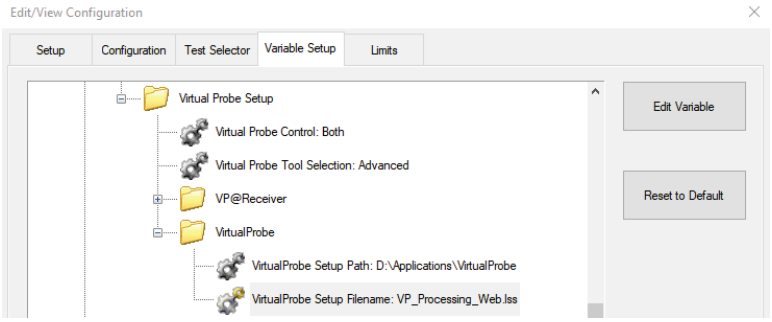
The math functions output by the WebEditor processing web should correspond to the following oscilloscope input channels:

- C1 = Source for F9
- C2 = Source for F10
- C3 = Source for F11
- C4 = Source for F12

1. On the QualiPHY wizard, after selecting the configuration to use, choose View/Edit Configuration, then open the Variable Setup tab and:
2. Turn “Virtual Probe Control” to “Read”, “Write” or “Both” types of bursts (it is Off by default)
3. Choose “Advanced” as the “Virtual Probe Tool Selection”:



4. In the Virtual Probe variable group, change:
   - “VirtualProbe Setup Path” to the full path to your setup file folder
   - “VirtualProbe Setup Filename” to the saved .lss file.



Note: You will need to save these changes to a new configuration, which will then be ready for selection whenever you wish to apply the processing web to this setup.

Appendix B: File Name Conventions for Saved Waveforms

QPHY-DDR4 saves the waveforms from each acquisition using a specific file name convention. This specific waveform name definition allows you to re-run any acquisition to recreate specific test results. When running QPHY-DDR4 in demo mode, the variables need to be set up appropriately to let QPHY know which waveform should be recalled.

Here is a typical QPHY-DDR4 waveform name: C2_CKDQ0DQS3_DQS3 _00014.trc

C2: This is the channel used to acquire the signal. In this case C2 was used. When running in Demo mode this portion of the waveform must match the **<Signal> Input Channel** variable. Possible values: C1, C2, C3, C4

CKDQ0DQS3: This is the probe setup used during the acquisition. When running in Demo mode this portion of the waveform must match the probe setup for the test group being run. Possible Values: CK (CK diff probe Setup), CKDQxDQSx (CK-DQ-DQS 3 probe setup), CKDQxDQSxAx (CK-DQ-DQS-Add 4 probe setup), etc.

DQS3: This is the signal name for this trace as it was set using the Analog Signal Name variable. When running in Demo mode this portion of the waveform must match the Signal Name variable. Possible values: DQ0-63, DQS0-15, etc.

00014: This is the file index. QPHY will automatically increment this by one on each run. When running in Demo mode this portion of the waveform must match the Recalled Waveform File Index variable. Possible values: Any five digit number.

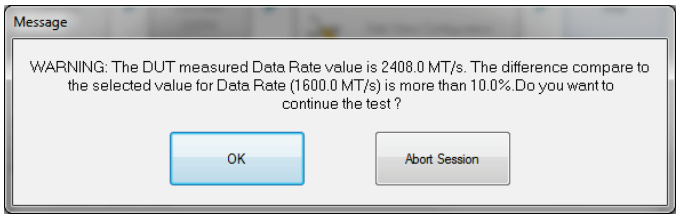
Portion of Trace Name	Meaning
C2	Channel Index
CKDQ0DQS3	Probe Setup
DQS3	Signal Name
00014	File Index

Appendix C: Common Warning Messages

Clock Speed Grade

At the beginning of each run, QualiPHY measures the clock speed to verify that the appropriate limit set is used.

This warning message occurs when the measured speed grade is greater than 10% different than the selected speed grade. When attempting to run on saved waveforms, if the displayed data rate is zero, this is an indication that the waveforms were not properly loaded by QualiPHY.

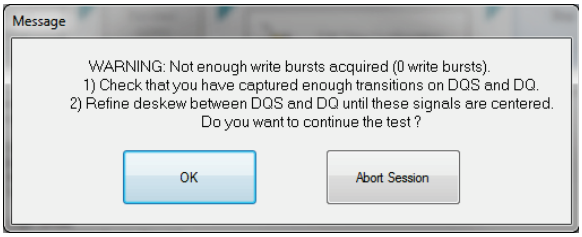


Solution: Check to make sure the appropriate limit set has been selected, or if using a custom speed grade, set the *Custom Speed Grade* variable.

Read/Write Burst

At the beginning of each run, QualiPHY checks if enough Read or Write bursts are captured in the acquisition.

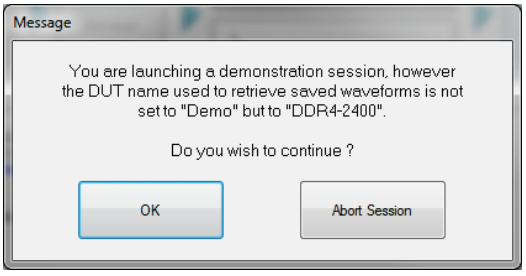
This warning appears when less than 10 R or W bursts are detected. When there are fewer than 10 bursts, the measurements will not have much statistical significance. If only R burst tests are selected, the script will only check for R bursts, and likewise with W bursts.



Solution: Verify that the device has enough DQ and DQS transitions. Either the acquisition length or the burst density can be increased. To increase the acquisition length, adjust the *Time per division for Acquisition* variable.

DUT Name

When running in Demo mode, QualiPHY warns if the DUT name is not “Demo”. The DUT name entered should match the name of the folder containing the saved waveforms.



Solution: Ensure the DUT name matches the folder in which you have saved waveforms. If it does, press “OK”.

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