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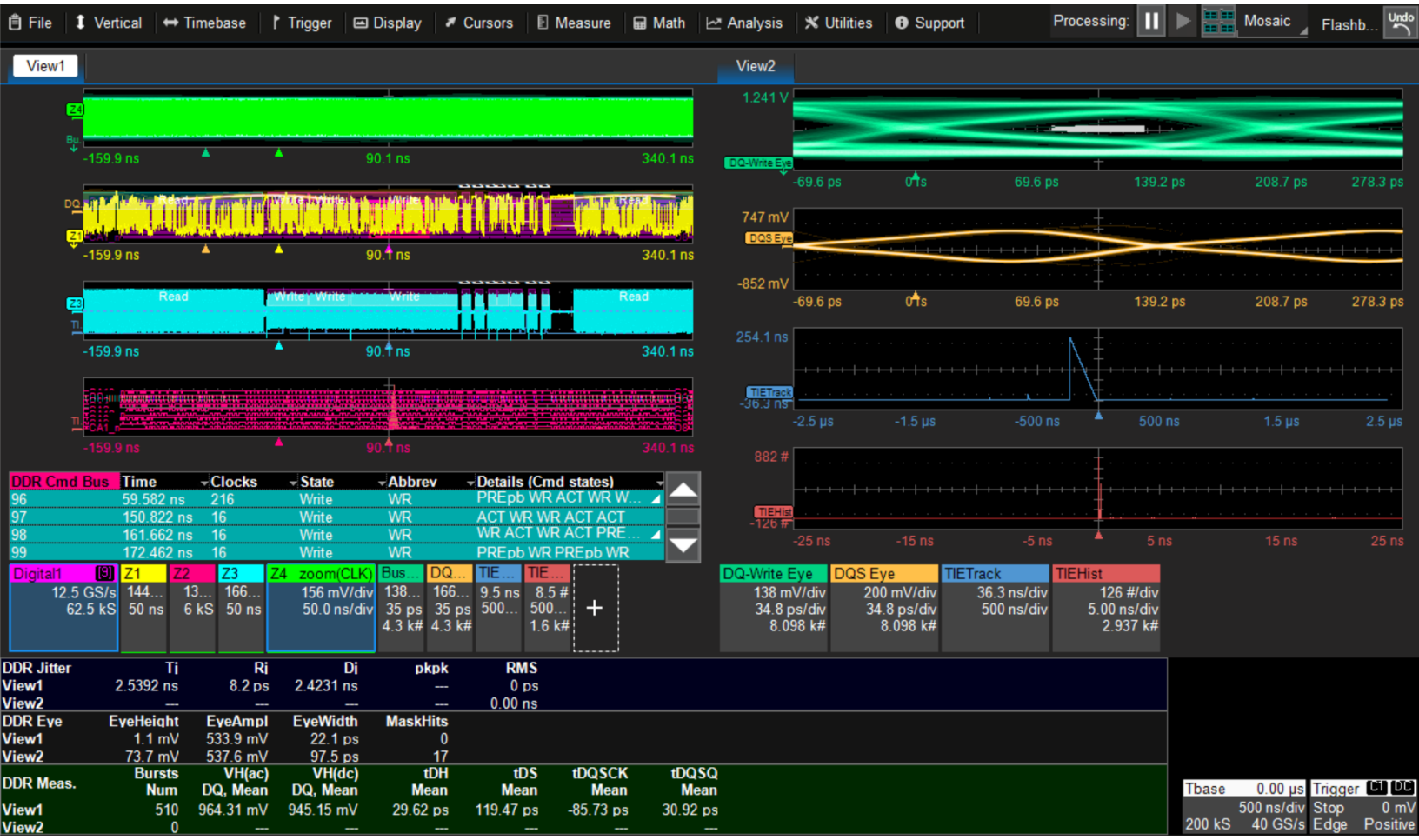

Instruction Manual

DDR Debug Toolkit

DDR Debug Toolkit Instruction Manual

April, 2023
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Contents

Introduction to DDR Debug Toolkit

Built on the specific recommendations of engineers and technicians, DDR Debug Toolkit provides debug and analysis tools for the *entire DDR design cycle*, unlike most oscilloscope-based DDR physical layer test tools targeted exclusively at JEDEC conformance testing. DDR Debug Toolkit helps you tackle unexpected failures at initial turn on, validate the effect of crosstalk on electrical and signal quality, perform burst separation and dive to the root cause of compliance failures.

With DDR Debug Toolkit, Teledyne LeCroy introduces numerous, time-saving industry firsts to simplify and enhance validation testing:

- Quickly create and measure eye diagrams, and perform eye mask testing to JEDEC standards.
- Use the Command Address Bus to extrapolate exactly where and when Read and Write commands are transferred. This enables the highest accuracy packet separation when used with the HDA125 High-speed Digital Analyzer.
- Identify the root cause of problems with jitter analysis specifically designed for bursted DDR signals that conventional serial data tools cannot analyze.
- Apply JEDEC DDR-specific measurement parameters, enabling easy quantitative analysis of system performance.

All this DDR analysis can be performed simultaneously on four different "Views" of the input, allowing for a deep understanding of system performance and dramatically improving DDR testing efficiency.

What's New

Teledyne LeCroy is always innovating to provide you with the latest standards and features. Following are some new additions to the DDR Debug Toolkit following release of the 10.2 and 10.3 versions of the MAUI software:

- LPDDR4X mask testing
- Faster Custom Protocol speeds—DDR5 up to 8400 MT/s
- New user interface for CMD Bus Decoding—now perform 90% of the command bus setup right in the DDR Debug Toolkit application
- Better threshold Autoset and Mask centering
- New user interface for R/W separation
- Support for DDR4/LPDDR4/LPDDR4X debug on WavePro HD Oscilloscopes

DDR Analysis Process

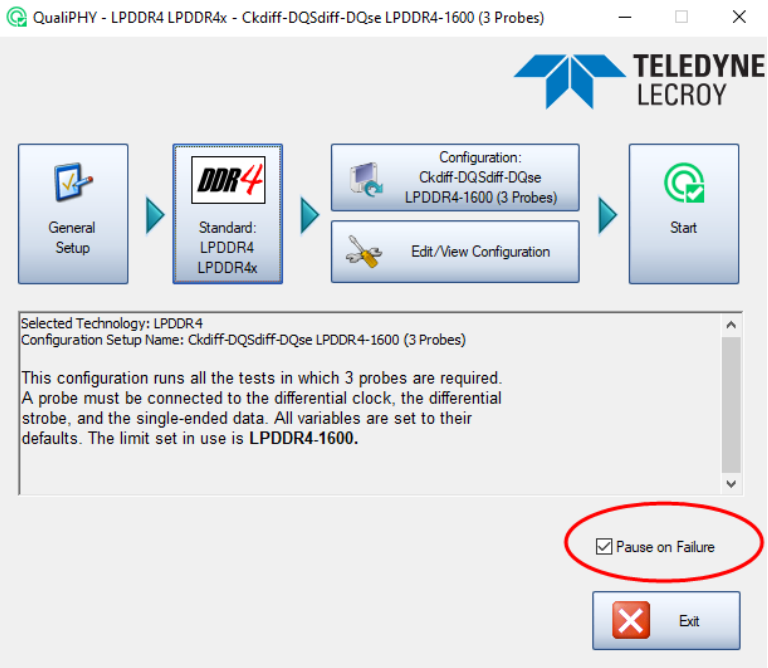
The recommended process for using DDR Debug Toolkit is:

1. Perform deskew, signal check and any other required preliminary procedures, such as virtual probing set up.
2. Configure properties of the input signals used.
3. Set up individual Views of the DDR signals.
4. If using digital R/W separation, configure the command bus.
5. If desired, add qualifications to target analysis to regions of bursts.
6. Select Eye, Jitter, or DDR measurements from the respective dialogs to begin analysis.

Using DDR Debug with QualiPHY

QualiPHY is Teledyne LeCroy's automated compliance test software. The QualiPHY DDR options autorun tests of JEDEC DDR- or LPDDR- specific measurements to the latest DRAM memory standard and autogenerate a PDF Pass/Fail report at the end, reducing test time and setup error.

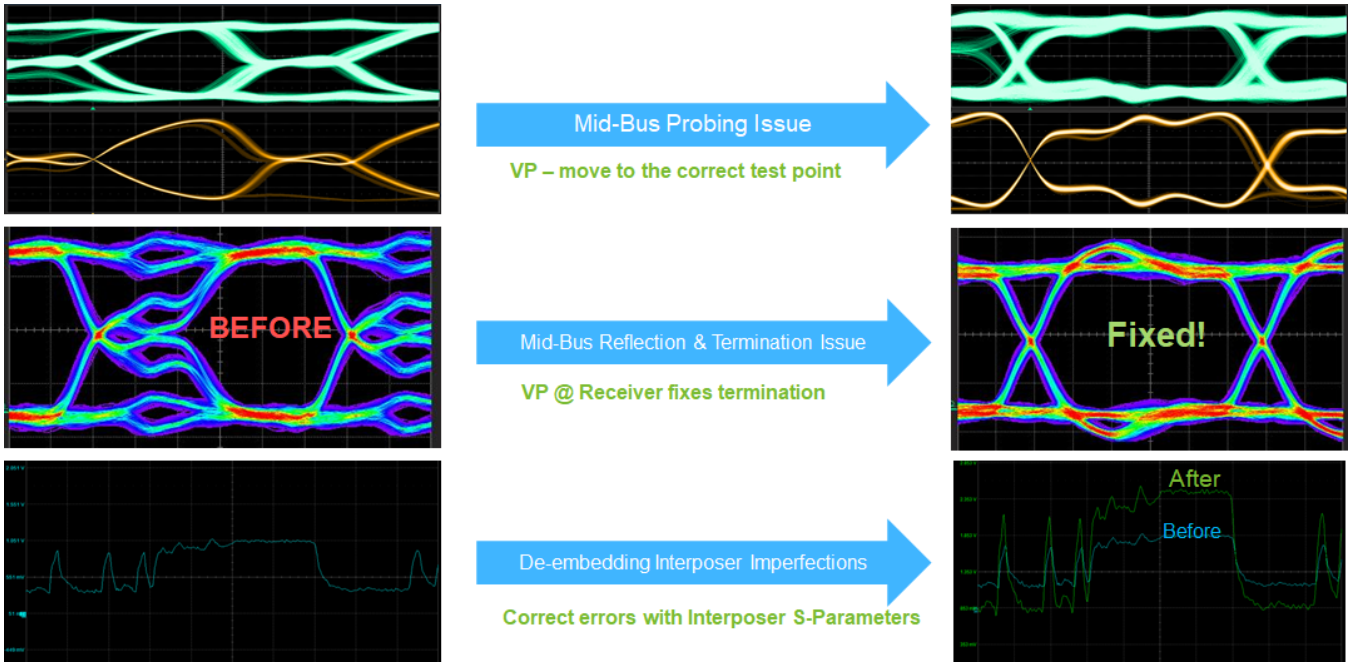
When devices unexpectedly fail, users need to know where and why this occurred. Sometimes, the problem can easily be traced to the need to correct for mid-bus reflections or improve thresholds. Worse, a design issue may be at fault. DDR Debug Toolkit was built for these exact use cases. Whenever using QuailiPHY, simply check the box labeled "Pause on Failure".



If a failure occurs, QualiPHY will pause to allow you open the MAUI oscilloscope application. Choose **Analysis > DDR Debug** to open the DDR Debug Toolkit to view the current setup, add new measurements and investigate the failure.

Using DDR Debug with VirtualProbe

VirtualProbe is an oscilloscope option enabling you to de-embed interposers, virtually "move" undesirable probing locations, and correct for mid-bus reflections and termination issues. After inputting the probed channel to the VirtualProbe application or math function, the post-processed output waveform is then input to DDR Debug Toolkit for actual analysis. For full, step-by-step procedures, see the Virtual Probing Set Up section of this manual.



Many signal quality problems can be corrected by first processing the inputs through VirtualProbe functions.

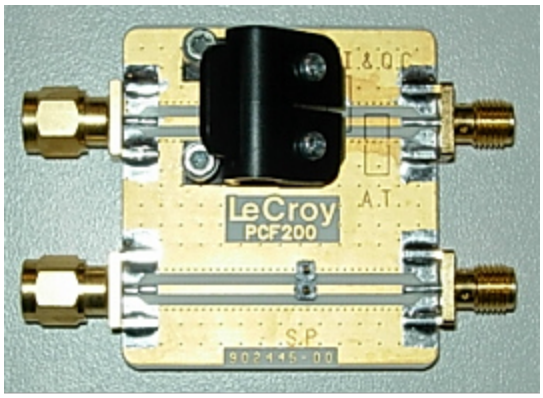
Signal Integrity Check & Probing Setup

Deskewing Probes

Before using the DDR Debug Toolkit, it is crucial to deskew probes to ensure proper signal timing.

Required Equipment

- PCF200 (included with WaveLink “-PS” probe systems)



- Square-Pin (SP) tip or additional Solder-In (SI) lead (included with "-PS" probe systems)
- 50 Ω terminator

Note: Alternatively, an LPA-K-A adapter and an SMA cable can be used.

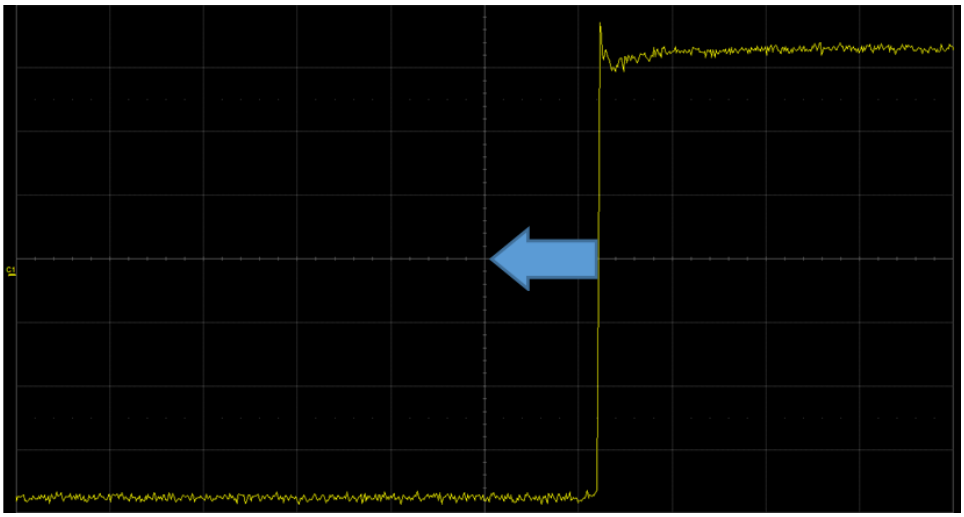
Procedure

1. Turn on the oscilloscope for at least 20 minutes and perform a self-calibration, if needed.
2. Connect the PCF200 to the oscilloscope’s Fast Edge output using the signal path indicated by the type of probe tip being used for the measurement:
    - The upper path (with the black clip) is for Solder-In (SI), QuickLink Solder-In (QL-SI), Quick-Connect (QC) and Adjustable Tip (AT) probe tips.
    - The lower circuit is for Square-Pin (SP) probe tips.

Tip: For ease of connectivity, we recommend using the SP tip. However, the tip does not matter as long as you use the *same* tip to deskew each probe. On some oscilloscope models, the Fast Edge signal is output over the Aux Out interface. Go to Utilities > Utilities Setup > Aux Output to configure the output for Fast Edge.

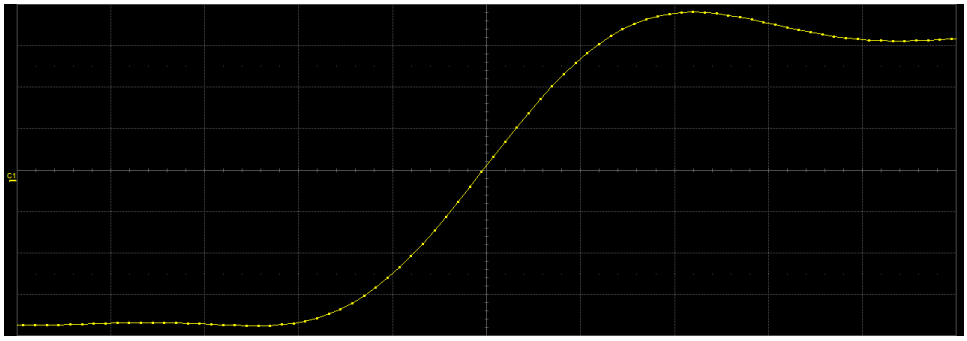
3. Connect probes electrically in a single-ended arrangement using their designated area on the fixture:
    - Connect the positive side, indicated by a plus sign on the probe tip, to the signal trace (between the two white strips).
    - Connect the negative side to the ground plane (outside the white strips).
4. In order to minimize reflection, apply a 50 Ω terminator to the end of the signal path in use. If a 50 Ω terminator is not available, an SMA cable can be used to terminate the PCF200 to one of the oscilloscope's outputs.
5. Connect the probe cable to C1.
6. Set the oscilloscope trigger type to "Edge", trigger source to "Fast Edge", timebase to 10 ns/div, and delay to zero. Start acquisition.

    Once everything is properly set up, the oscilloscope display should look similar to the figure below. If there is no propagation delay due to the probe, and no internal oscilloscope channel propagation delay, the 50% trigger level will appear exactly centered on the oscilloscope grid. Any visible delay represents the amount of skew to be corrected.



Initial view of trace before adjustment. Enter deskew value to move rising edge to center.

7. Adjust the C1 Deskew value so that the 50% rising edge point is centered on the grid, as shown in the image below:
    - From the C1 setup dialog, enable Sinx/x Interpolation and set Averaging to 50 sweeps.
    - Adjust the Deskew value to move the rising edge of the trace toward the center of the display.
    - Decrease the timebase to around 20 ps/div, and adjust the Deskew value so that the 50% rising edge point is centered on the grid.



After adjustment, trace should cross at exactly 50% level at center.

8. Repeat this procedure for each probe using the same probe tip.

Note: Before moving on to the next probe, reset Averaging to 1 sweep and turn off Sinx/x Interpolation.

Initial Signal Checking

Before using the DDR Debug Toolkit, perform these key quality checks of your data, strobe and clock signals to avoid potential setbacks.

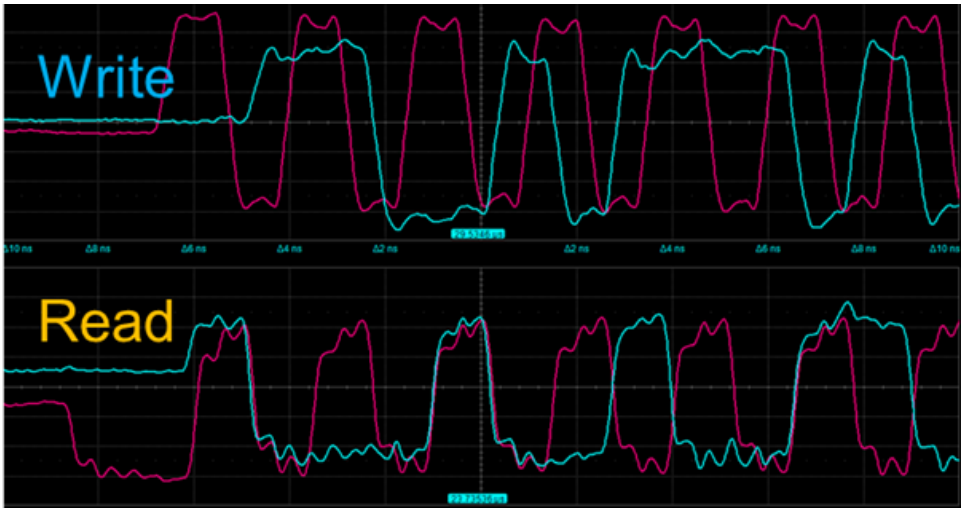
Signal Amplitude

For best results, it is recommended that signals cover at least 80% of the vertical grid. Use the channel Vertical Scale (V/Div) control to adjust the amplitude of each signal.

Presence of R/W Burst

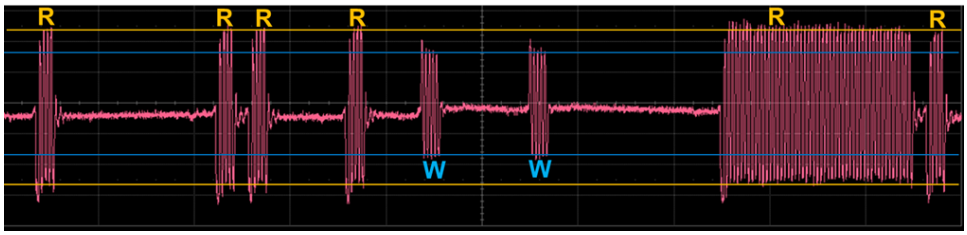
Check that the device is outputting the expected bursts. As a general rule of thumb:

- During an R burst, DQ and DQS should be in phase
- During a W burst, DQ and DQS should be a quarter cycle out of phase



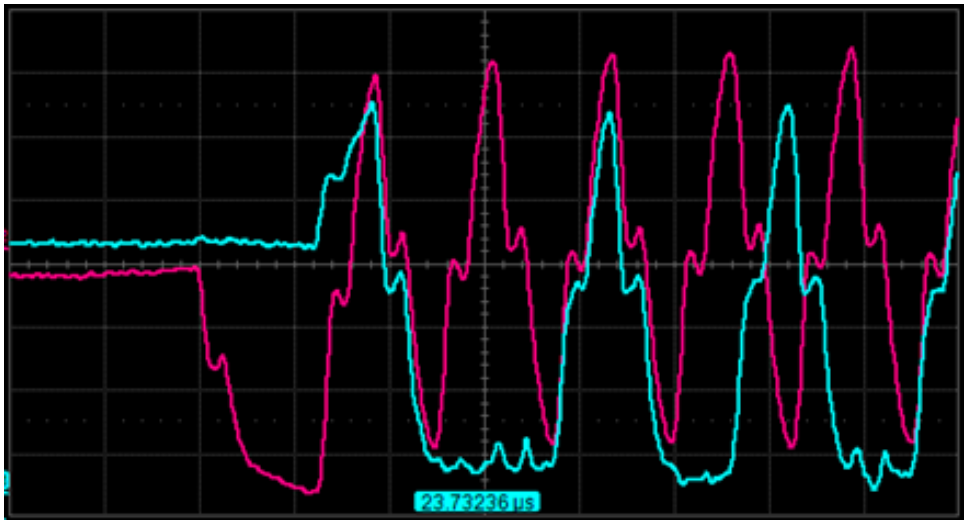
Note: The general rule of phase difference does not apply to LPDDR4 due to the DQS-DQ training process.

Additionally, use the signal amplitude to determine the presence of R and W bursts. When probing at the memory, R bursts will have a larger amplitude than W bursts.



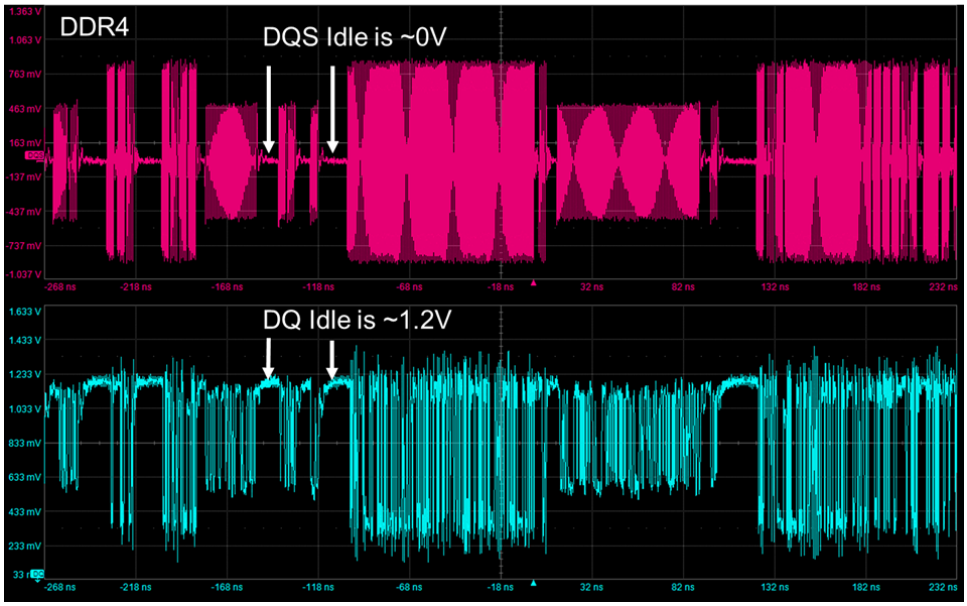
Signal Quality

Evaluate if there are signal reflections within the burst packets, as this can complicate the accuracy of the packet separation and electrical and timing measurements. If you see problems as in the image below, see the section on VirtualProbe@Rcvr Math Functions later in this document for ways to adjust for unwanted reflections.



Idle Levels

Validate the signal idle levels. Incorrect signal idle levels will negatively impact the R/W burst detection, electrical, and timing measurements. For example in DDR4, DQS should have an idle level of ~ 0 mV, while DQ should have an idle level slightly less than 1.2 V. In other standards, like LPDDR4, this idle level may differ vastly.



Correct DQS/CK Differential Probing (True *and* Complement)

It’s important that the Strobe (DQS) and Clock (CLK) are properly set up for differential probing. One common mistake is using a differential probe across just the DQS_t (True) and Ground. This causes undesired leveling problems, making it extremely hard to perform R/W separation. The proper setup should have the differential probe across both the DQS_t (true) and DQS_c (complement), or else across the CK_t (true) and CK_c (complement). It's important that the idle stage be in the middle of the packets.

Virtual Probing Set Up

Because the JEDEC electrical specifications are defined at the balls of the DDR DRAM, it is often necessary to use the virtual probing capabilities of the oscilloscope to get the best representations of the signals to be analyzed with DDR Debug Toolkit.

Because DDR Debug Toolkit and QPHY-DDR* are often used together on the same device, it is good practice to ensure your DDR Debug virtual probing setup can also be used when you perform compliance testing using QualiPHY. QualiPHY has specific requirements for virtual probing that you will want to observe in the setup files you save and the selections you make in DDR Debug Toolkit.

The virtual probing capabilities described here become available with the installation of the SDAIII-CompleteLinQ or VirtualProbe software options.

Virtual Probing Solutions

There are three approaches to using virtual probing in DDR Debug Toolkit, each of which solves different DDR probing problems.

VirtualProbe@Recvr Functions

Problem: Mid-bus reflections and termination issues. In DRAM setups, sometimes the probe location adds timing delay and mixed with incorrect terminations can cause a supper effect of bounding reflections.

Solution: Apply the VirtualProbe@Rcvr math processor to the input signals, then use the resulting math functions as inputs to DDR Debug Tookit. This math processor will apply the termination network parameters to the acquired signals, helping you to account for an correct the problem of mid-bus reflections.

VirtualProbe Software De-embedding

Problem: Mid-bus probing location issues. At times the PCB via is in an unintended location. This location causes the actual measurement location to not be at it's idea Ball of the DRAM, as called out by the JEDEC.

Solution: Use VirtualProbe software to apply S-parameter models to the input signals, then use the resulting VPOut* waveforms as inputs for DDR Debug. By De-embedding using .s2p (single-ended) or .s4p (differential) setups, you can remove the trace length to achieve the expected test point location at the Ball of the DRAM. Likewise, if you wish to analyze READ packets at the controller, you can move the location of the probe point using a simulated Virtual Probe to effectively see how strained the READ packet eye looks.

WebEditor Netlist with VirtualProbe Functions

Problem: Interposer integration. Installing a Nexus or EKH style interposer can sometimes come with challenges. The fact the interposers provide a T-Setup means the S-Parameter files are in a configuration not typically supported by oscilloscopes.

Solution: Use WebEditor to apply the VirtualProbe math processor to the input signals, then use the resulting math functions as inputs for DDR Debug. In this unique Netlist configuration, you'll be able to de-embed an interposer with .s3p or .s6p S-parameters.

VirtualProbe@Rcvr Math Functions

The VirtualProbe@Rcvr math processor is recommended if the difference between the signal being probed and the desired signal can be defined as a simple RLC termination model with some transmission line delay, as shown in the following figure. Here, the probe point is the input (In) of the termination model and the desired signal is the output (Out) of the model.

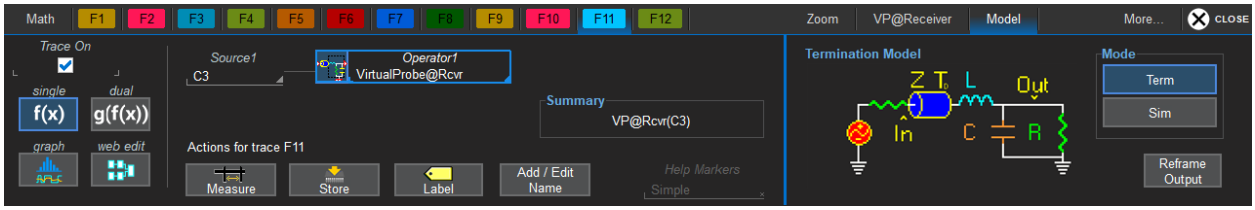
Create Math Functions

For each signal that you will analyze in DDR Debug Toolkit, apply the VirtualProbe@Rcvr math processor to the acquired signals. For interoperability of DDR Debug Toolkit and QualiPHY, best practice is to use:

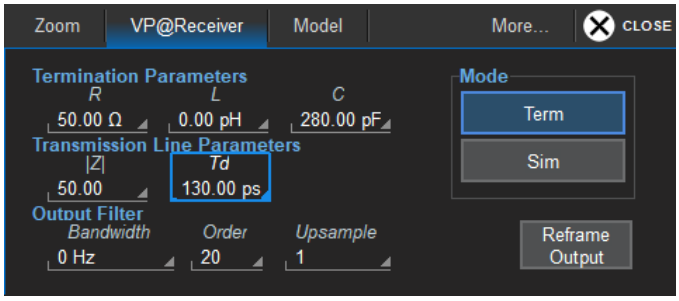
- CLK on C1 = source for F9
- DQS on C2 = source for F10
- DQ on C3 = source for F11
- Other (e.g., ADDR) on C4 = source for F12

For example, to apply VirtualProbe@Rcvr to the DQ signal on C3:

1. Open the oscilloscope F11 setup dialog and choose C3 as Source1 and VirtualProbe@Rcvr as Operator1.
2. On the Model subdialog, choose Term(ination) mode.



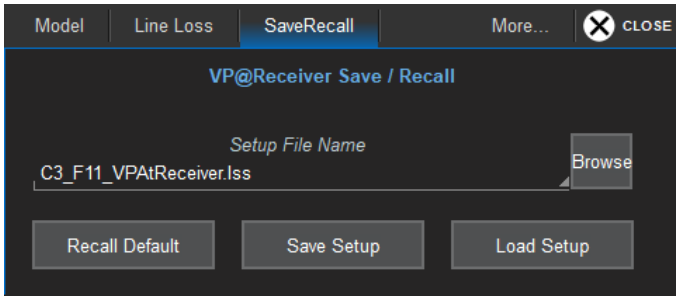
3. Open the VP@Receiver subdialog and input the termination network parameters.



   For more information on using the VirtualProbe@Rcvr math processor, see the white paper, *Using the Virtual Probe Receiver Math Operator to Eliminate Reflections*.

4. As you create each math function, go to the SaveRecall subdialog and Save Setup to an .lss file for each input signal.

   It will be easier to select files in QualiPHY if you include the input channel in the filename, for example, C3_F11_VPAtReceiver.lss.

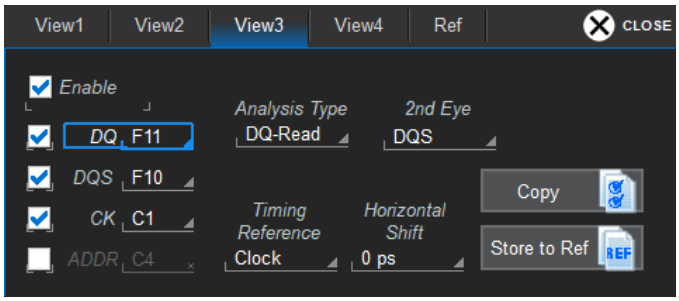


5. Copy all files to an oscilloscope folder that QualiPHY can access. The default is D:\Applications\VPAtReceiver.

Configure DDR Debug Toolkit

When setting up your DDR Debug Toolkit Views, select the VirtualProbe@Rcvr math functions you created as the inputs for the signals, rather than the oscilloscope channels.

In this example, DQ is probed on C3 and DQS is probed on C2 of the oscilloscope. F11 and F10 are the VirtualProbe@Rcvr math functions that were applied to the probed signals, respectively.



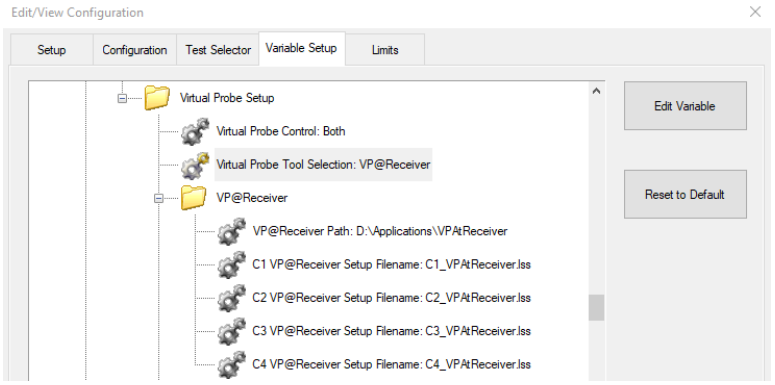
Using VirtualProbe@Rcvr with QualiPHY

QualiPHY expects specific math functions to represent specific inputs when using the VirtualProbe@Rcvr method. When creating your math functions, use:

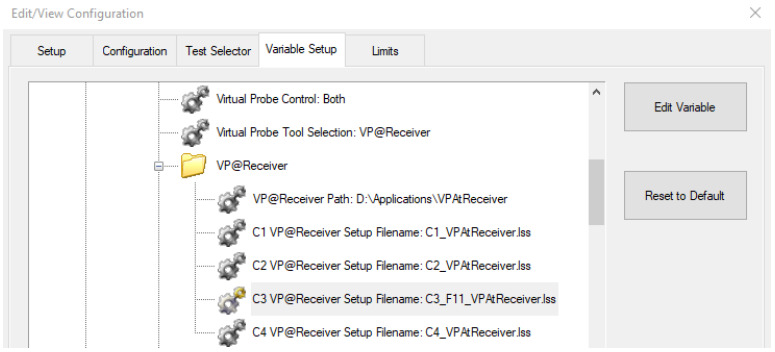
- C1 = Source for F9
- C2 = Source for F10
- C3 = Source for F11
- C4 = Source for F12

On the QualiPHY wizard, after selecting the configuration to use:

1. Choose View/Edit Configuration, open the Variable Setup tab and:
    - Turn “Virtual Probe Control” to “Read”, “Write” or “Both” types of bursts (it is Off by default)
    - Choose “VP@Receiver” as the “Virtual Probe Tool Selection”



2. In the VP@Receiver variable group, change:
    - "VP@Receiver Path" to the folder containing the saved setup files
    - "Cn VP@Receiver Setup File" to the names of the files representing compensated input channels



Note: You will need to save these changes to a new configuration, which will then be ready for selection whenever you wish to apply VirtualProbe@Rcvr.

Virtual Probe Software De-embedding

The Virtual Probe method can be used if the difference between the signal being probed and the desired signal can be defined by one or more S-parameter touchstone files (.s2p for single-ended and .s4p for differential).

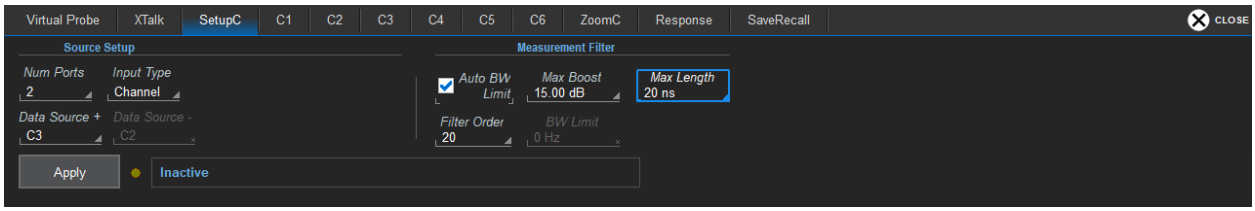
Configure Virtual Probe Setups

In the Virtual Probe software, S-parameters can be used to define multiple stages of the input/output signal flow. For interoperability of DDR Debug Toolkit and QualiPHY, best practice is to use:

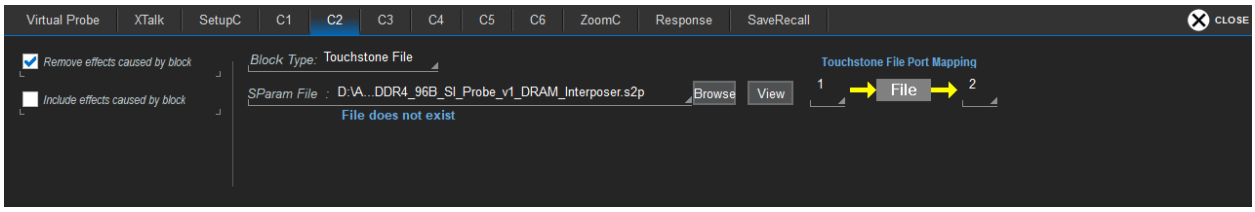
- CLK on C1 = source for SetupA
- DQS on C2 = source for SetupB
- DQ on C3 = source for SetupC
- Other (e.g., ADDR) on C4 = source for SetupD

For example, to apply Virtual Probe Setup C to the DQ signal on C3:

1. Open the SetupC dialog and choose C3 as the Data Source.

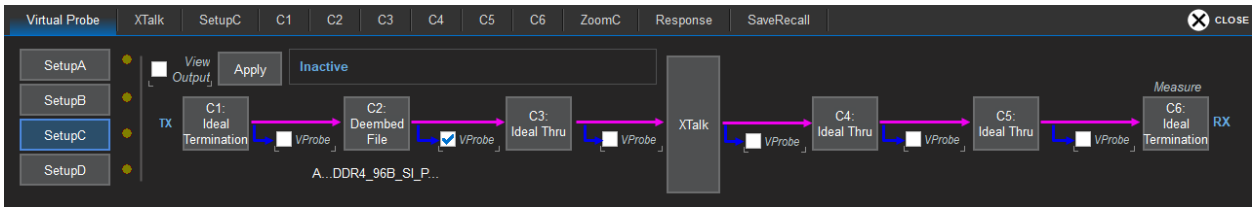


2. On the C2 dialog (or at whichever block of the circuit you wish to deembed), select “Remove effects caused by block” and import the .s2p file representing the fixture you want deembedded (here, the interposer).



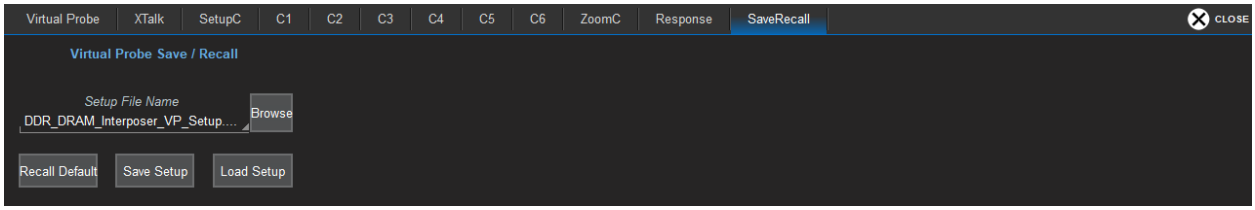
Note: In this example, C2 has nothing to do with the signal input channel, but represents the order of processing in the Virtual Probe "circuit." Setups A, B and D have similar blocks A2, B2, and D2.

3. On the Virtual Probe dialog, select block C2 (Deembed File).



4. Do the same for the other inputs that require virtual probing, following the conventions as to which Virtual Probe Setup to use for which input.

5. Open the SaveRecall dialog and save the Virtual Probe setup to an .lss file in an oscilloscope folder that QualiPHY can access. The default folder is oscilloscope D:\Applications\VirtualProbe.

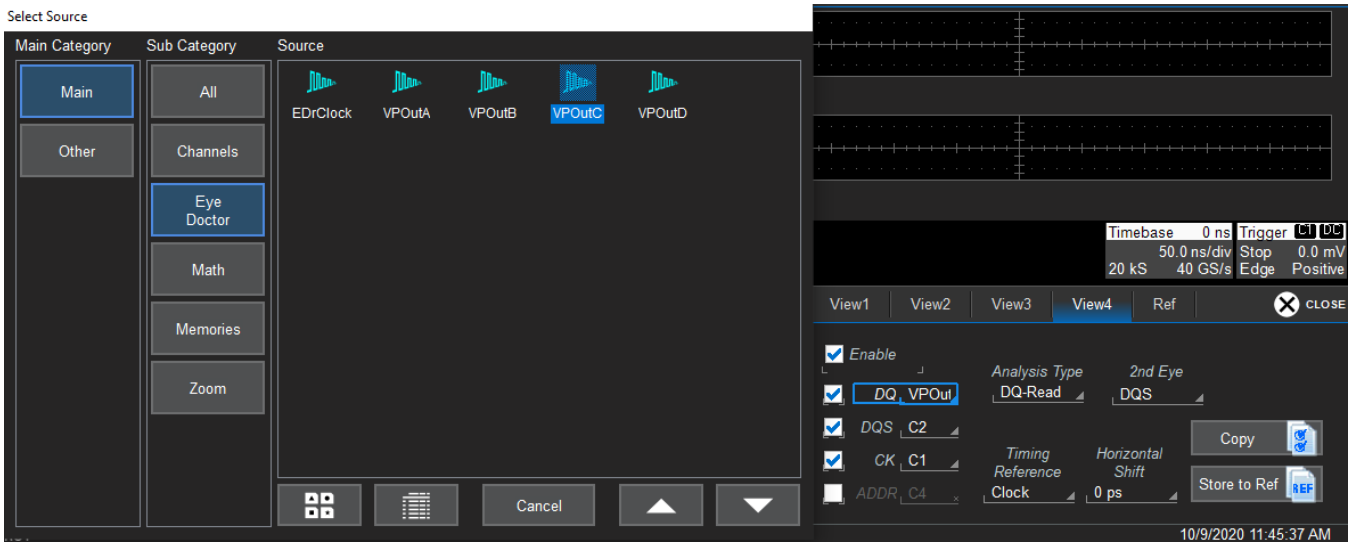


Note: With this method, there is only one setup file, vs. four setup files for VirtualProbe@Rcvr.

Configure DDR Debug Toolkit

Select the VPOut* waveforms corresponding to each Virtual Probe Setup you created as the sources for DDR Debug Toolkit Views. SetupA will output VPOutA, and so forth.

In this example, SetupC is the DQ signal with the interposer deembedded, represented by VPOutC, so that waveform is selected as the DQ input in DDR Debug Toolkit, rather than the probed input C3.



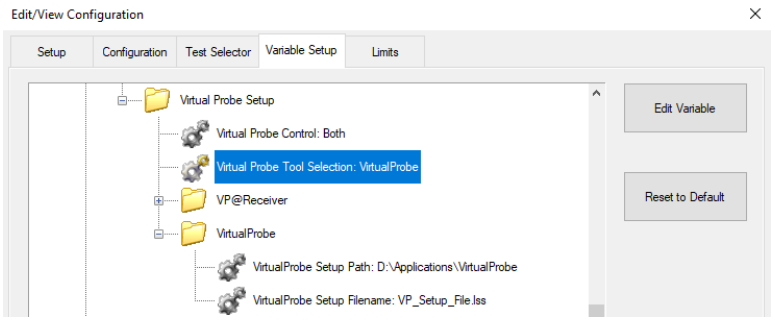
Note: VPOut* waveforms are in the Eye Doctor selector menu.

Using Virtual Probe with QualiPHY

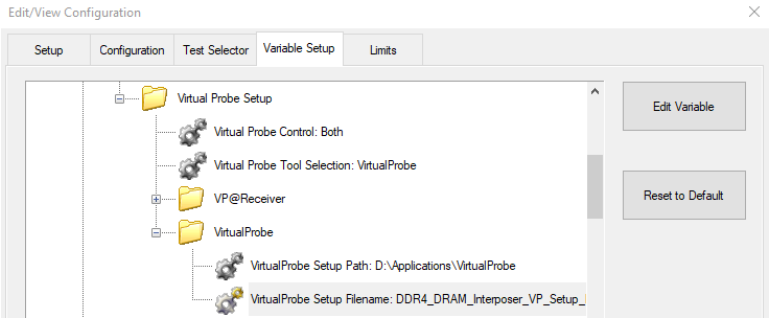
The Virtual Probe setups should correspond to the oscilloscope input channels as follows:

- C1 = Source for SetupA (VPOutA)
- C2 = Source for SetupB (VPOutB)
- C3 = Source for SetupC (VPOutC)
- C4 = Source for SetupD (VPOutD)

1. On the QualiPHY wizard, after selecting the configuration to use, choose View/Edit Configuration, then open the Variable Setup tab and:
    - Turn “Virtual Probe Control” to “Read”, “Write” or “Both” types of bursts (it is Off by default)
    - Choose “VirtualProbe” as the “Virtual Probe Tool Selection”



2. In the VirtualProbe variable group, change:
    - "VirtualProbe Setup Path" to the full path to your setup file folder
    - "VirtualProbe Setup Filename" to the saved .lss file



Note: You will need to save these changes to a new configuration, which will then be ready for selection whenever you wish to apply Virtual Probe to this setup.

WebEditor Netlist with VirtualProbe Functions

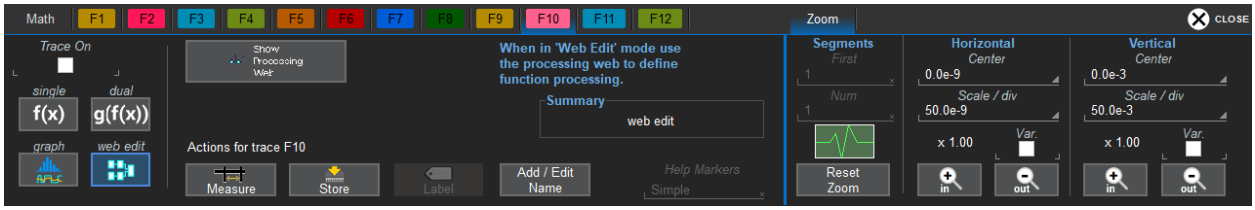
Some interposers use more sophisticated S-parameters than the 2- or 4-port models, such as .s3p and .s6p. For these cases, the netlist of the interposer can be defined using the oscilloscope WebEditor tool. The WebEditor will output math functions corresponding to the compensated channels, which will be used as inputs in DDR Debug Toolkit, similar to the VirtualProbe@Rcvr method. For interoperability of DDR Debug Toolkit and QualiPHY, best practice is to use:

- CLK on C1 = source for F9
- DQS on C2 = source for F10
- DQ on C3 = source for F11
- Other (e.g., ADDR) on C4 = source for F12

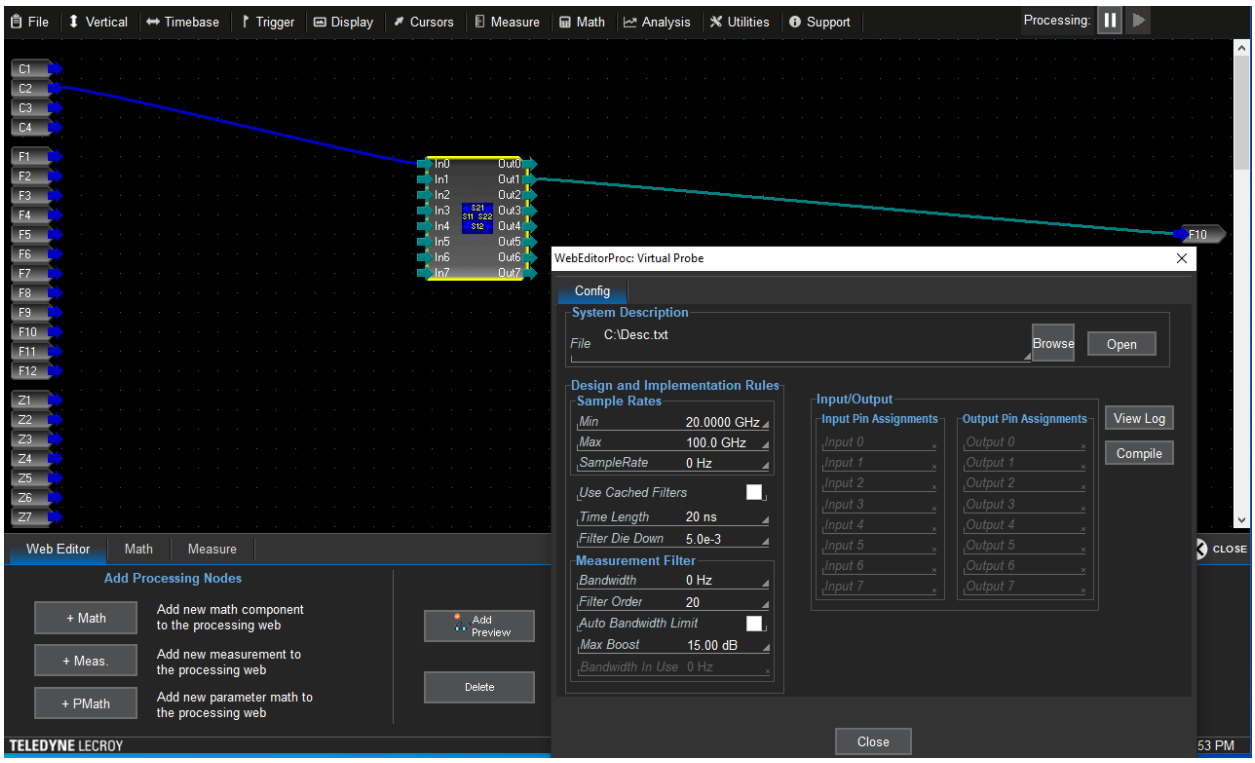
Define Netlist in WebEditor

In this example, the probed DQS and DQ signals are input on C2 and C3. These inputs will undergo the processing web to deembed the interposer from the signal.

1. To begin, open the F10 dialog and select web edit, then Show Processing Web.



This will take you to a screen like that below where you create a processing web that inputs C2 and C3, passes them through the VirtualProbe math processor, and outputs F10 and F11. The VirtualProbe processor allows you to configure the characteristics of the interposer, including applying signal filters and manually mapping input to output pins.



2. Do the same for C3-F11 and other inputs that require virtual probing, following the conventions below as to which math functions to use for which channels. Both F10 and F11, and any other math functions needed, can be placed on the same processing web.

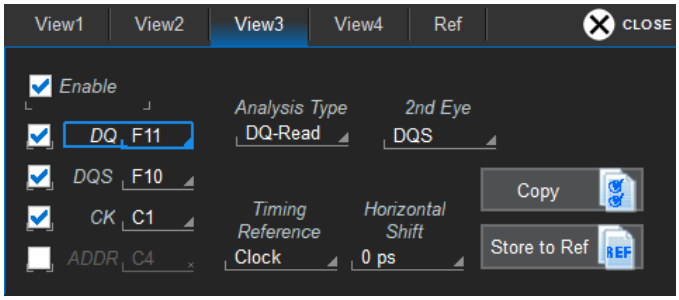
3. Save the configuration to an .lss file in an oscilloscope folder where QualiPHY can access it.

Note: With this method, there is only one setup file, vs. the four setup files for VirtualProbe@Rcvr.

Contact Teledyne LeCroy support for more information about creating and saving your processing web.

Configure DDR Debug Toolkit

Choose the math functions resulting from the processing web as the inputs for DDR Debug Toolkit Views:

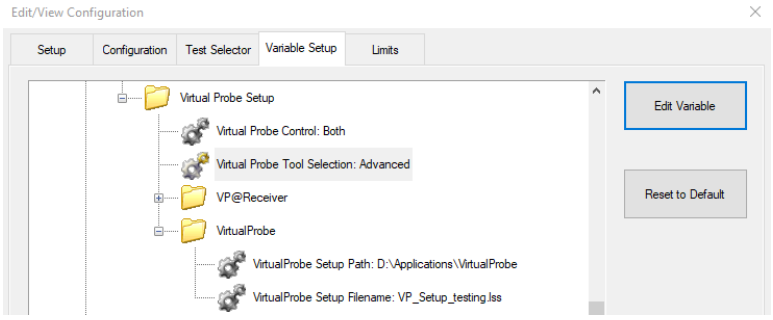


Using WebEditor with QualiPHY

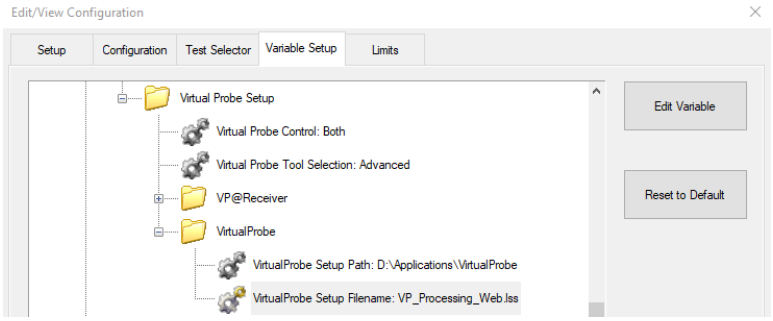
The math functions output by the WebEditor processing web should correspond to the following oscilloscope input channels:

- C1 = Source for F9
- C2 = Source for F10
- C3 = Source for F11
- C4 = Source for F12

1. On the QualiPHY wizard, after selecting the configuration to use, choose View/Edit Configuration, then open the Variable Setup tab and:
    - Turn “Virtual Probe Control” to “Read”, “Write” or “Both” types of bursts (it is Off by default)
    - Choose “Advanced” as the “Virtual Probe Tool Selection”



2. In the Virtual Probe variable group, change:
    - “VirtualProbe Setup Path” to the full path to your setup file folder
    - “VirtualProbe Setup Filename” to the saved .lss file



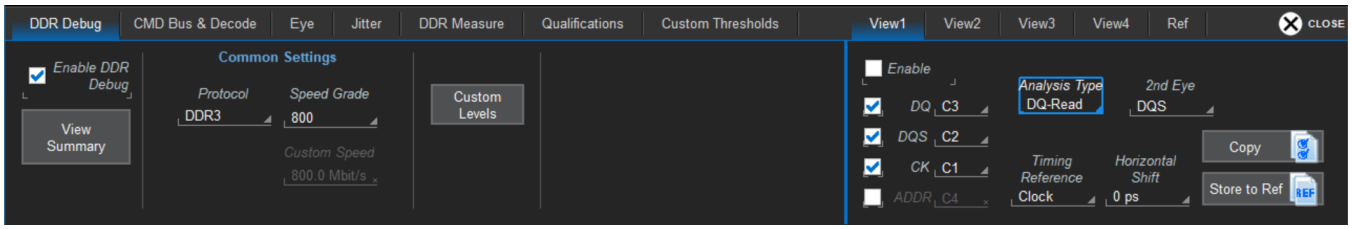
Note: You will need to save these changes to a new configuration, which will then be ready for selection whenever you wish to apply the processing web to this setup.

DDR Debug Set Up

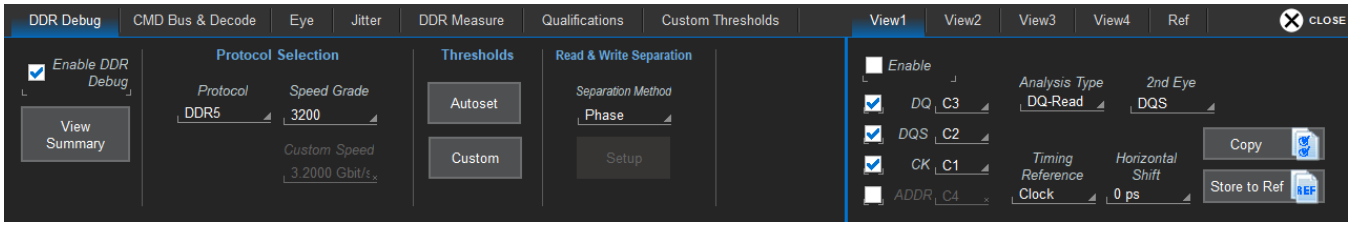
To turn on the DDR Debug Toolkit functionality:

1. From the menu bar, choose **Analysis > DDR Debug**.
2. Select the **Enable DDR Debug** checkbox in the top left corner of the main DDR Debug dialog. Deselecting this box will turn off all DDR views and measurements, although your configurations will remain in place.

Caution: Before enabling DDR Debug, *disable* SDAIII, PAM4 or VectorLinQ by clearing the Enable checkboxes within these applications. The applications cannot run concurrently.



Legacy DDR Debug setup dialog.



New DDR Debug setup dialog used for DDR4, LPDDR4, LPDDR4X, and DDR5 .

There are two types of settings on this dialog:

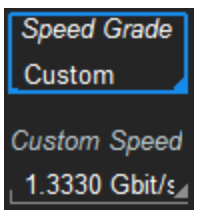
- Settings used to characterize the DDR signal inputs. These apply to all views.
- View-specific settings that appear on the subdialogs to the right of the main dialog. There is one tab for each analysis view, plus a Ref(erence) view which may be copied from any other view and stored for future comparison.

Protocol Selection

In **Protocol**, choose the DDR JEDEC standard used by the signals under test.

The **Speed Grade** setting will adjust to what is defined by the standard for the selected protocol. If using a non-standard speed, choose Custom and enter the system transfer rate.

For example, DDR3-1333 should be entered as 1.3330 Gbit/s.



Thresholds

The protocol selection defaults Vref, VOH, VOL, VDD threshold values as designated by the JEDEC Standard. By pressing the **Autoset** button, DDR Debug measures the Vref for the Write DQ packet. Typically, Vref is calculated as VDD (supply voltage) /2 of the current acquisition.

To use other thresholds, enter them on the Custom Thresholds dialog. Enter custom Vref values in mV.

Tip: You can use the Custom or Custom Levels button to open the Custom Thresholds dialog.

Read & Write Separation

DDR Debug Toolkit offers two options for Read/Write separation:

- Analog approach, which looks only at the DQ and DQS signals and separates Reads and Writes accordingly. This involves analyzing the Preamble or Phase relationship to make the best prediction of where a Read or Write packet occurs. For example, in DDR4 the DQ/DQS signals in a Read packet are in phase, while in a Write packet they are out of phase.
- Digital approach, which looks at the DDR command bus (input using an HDA125) to determine when a Read or Write command was sent and uses the latency periods to calculate the start of a Read or Write burst.

The following table shows the Read/Write separation methods by standard supported by Teledyne LeCroy products. If you are using DDR Debug Toolkit with QualiPHY, we recommend that you choose a Read/Write separation method supported by both.

	Analog				Digital	
	DQ/DQS Phase		Preamble		Command Bus (HDA125)	
Standard	QualiPHY	DDR Debug	QualiPHY	DDR Debug	QualiPHY	DDR Debug
DDR3	Yes	Yes	No	No	Yes	Yes
DDR3L/LPDDR3	Yes	Yes	No	No	No	Yes
DDR4	Yes	Yes	No	No	Yes	Yes
LPDDR4/LPDDR4X	No	No	Yes	Yes	Yes	Yes
DDR5	N/A*	Yes	N/A	No	N/A	Yes

* N/A indicates software not yet available.

On the DDR Debug dialog, in **Separation Method**, choose to use Phase, Preamble or CMD Bus.

Note: For DDR2, LPDDR2, DDR3, DDR3L and LPDDR3, this selection is made on the CMD Bus & Decode dialog. Check **Enable R/W Separation using CMD Bus** to use digital R/W separation. If the command bus is not selected, the software will default to using the supported analog method.

If using the command bus, you will need to connect the HDA125 to the oscilloscope and DUT, then configure the command bus digital inputs on the CMD Bus & Decode dialog.

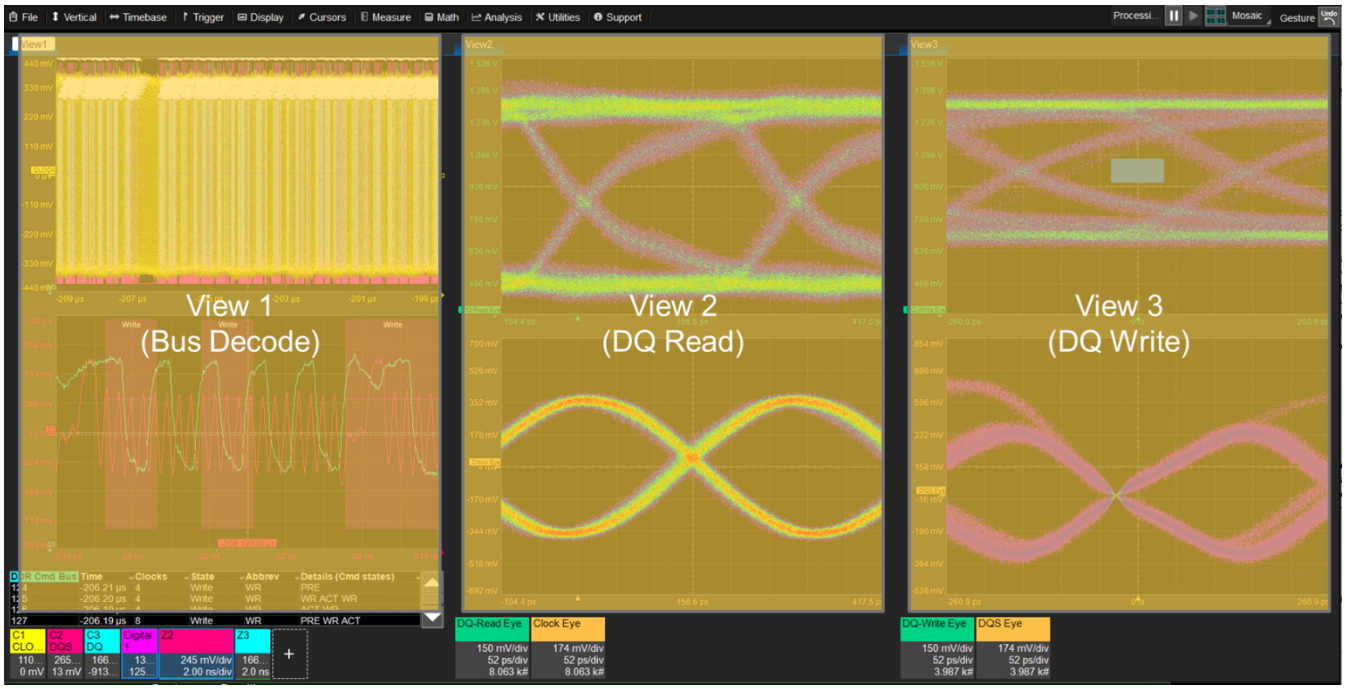
Tip: You can use the Setup button to open the CMD Bus & Decode dialog.

For instructions on connecting the HDA125, see the *HDA125 High Speed Digital Analyzer Operator's Manual*.

Setting Up Views

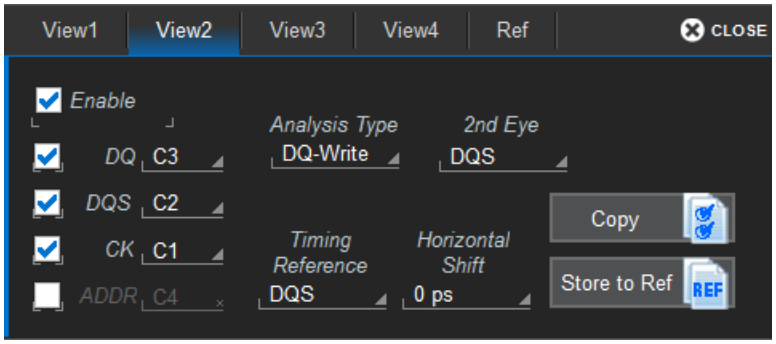
You can configure up-to-four primary Views plus a stored Reference View of the DDR signals. Eye parameters, jitter measurements and DDR measurements are calculated for each View.

A View constitutes a set of signals and the selection of an Analysis Type applied to them. Each View results in a unique eye diagram and jitter track, which may be displayed along side that of any other Views for easy comparison.



The three Views above show the Command Bus Decode, and a comparison of the DQ-Read and DQ-Write eye diagrams of the same signal.

Note: The inputs to Views can be live channels or calculated signals, such as math functions and Virtual Probe or Eye Doctor output waveforms. See Virtual Probing Set Up if you are using virtual probing to compensate the acquired DDR signals.



Signals Analyzed

On the desired View*n* subdialog, check **Enable** to turn on the View.

Select the checkbox for each **signal** (DQ, DQS, etc.) you wish to analyze in that View.

Using the field next to the signal checkbox, assign an **input** to each signal selected. Inputs can be any live channel, memories (stored waveforms), math functions or other waveforms.

Analysis Type

In **Analysis Type**, choose how to generate the primary eye diagram for this View.

- DQ-Read and DQS-Read build the eye diagram from only the Read bits in the respective signals.
- DQ-Write and DQS-Write build the eye diagram from only the Write bits in the respective signals.

The Analysis Type Bus does not generate an eye diagram but instead turns on the Command Bus Decode, placing colored overlays showing significant transitions of the command bus on the selected digital bus and analog signals. Decoded commands are also shown in a table below the input waveforms. You can modify decoder settings on the CMD Bus & Decode dialog.

2nd (Reference) Eye Signal

Choose the signal to be analyzed in a **2nd Eye** that can be displayed next to the main eye for reference. This 2nd Eye correlates to the first eye setup under Analysis Type. If the Analysis Type is DQ-Write or DQS-Write, then the 2nd Eye will be peformed on a Write burst packet. Likewise if DQ-Read or DQS-Read is selected, the 2nd Eye will be performed ona Read burst packet.

Timing Reference

The **Timing Reference** helps to diagnose timing inconsistencies between the clock, strobe and data.

Defaulted to Clock, if you have problematic signals try changing the reference timing to DQS Strobe. This typically shifts the crossing point to be in phase if the 2nd Eye is Clock and out of phase if it is DQS.

The Timing Reference field is disabled if the primary Analysis Type is DQS (Read or Write), as that signal's only reference has to be the clock.

Horizontal Shift

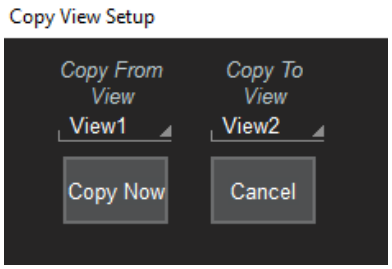
To horizontally shift all signals with respect to the Timing Reference, enter the amount of delay in **Horizontal Shift**. This capability allows you to center a mask inside the eye diagram. The shift applies only to the View in which it is set.

Note: The Center DQ Write Eyes function on the Eye dialog calculates the Horizontal Shift required to center the eye around a mask. This value will propagate to the Horizontal Shift field.

Copying Views

Quickly set up new Views by copying from an existing view.

1. Touch the Copy button on any View subdialog.
2. Choose the View to Copy From and the View to Copy To, then touch Copy Now.



3. On the DDR Debug dialog, modify those settings that differ between these Views.

Storing Views to Reference

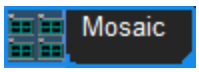
The Reference View allows you to easily conduct performance tuning or optimization tests. You may store any view into the reference slot, then change its setup to observe the change in performance characteristics. Measurements can be added or removed from the reference at any time, so there is no need to worry about having all analysis parameters defined at the beginning of testing.

To store a view to reference, open the View*n* subdialog, then touch Store to Ref.

Arranging Views

Views support different grid styles, allowing you to arrange multiple eye diagrams and traces any way you like on the display. All Views will take whatever grid mode you select from the Display Setup dialog. Drag-and-drop descriptor boxes to move traces between grids.

As in other Serial Data Analysis software, you can change the placement of Views on the display by using the LandScape control on the menu bar.



- Single uses the entire display area for a single View. Views are arranged one behind the other on separate tabs.
- Dual places two sets of enabled Views side by side. Use the tabs to select which View is displayed on top in each group.
- Mosaic arranges all enabled Views around the display, where they can be seen simultaneously.

The LandScape selection will be limited by the number of Views enabled.

Summary

Select View Summary at the far left of the main DDR Debug dialog for an overview of all View configurations.

Using Custom Thresholds

Measurements and R/W separation are performed with reference to the thresholds set on the Custom Thresholds dialog. For the best accuracy, it's important to have good thresholds that represent your unique DDR or LPDDR signals. The Autoset feature does a good job of analyzing the signals to determine the Vref.DQ level, but further fine-tuning can increase measurement accuracy and improve packet separation. Many things can degrade the signal quality, but correcting for signal quality and carefully setting the thresholds goes a long way in DDR/LPDDR testing.

It is important to ascertain which packet is a Read (Output data from DRAM) and which is a Write (Input Data to DRAM). To set up the measurement system for Eye Diagram Analysis and measurements:

- The Vref. DQ level should be centered in the Write packet.
- The VOH(AC) and VOL(AC) levels should be around the 20-80% levels of the Read packet.

You may need to fine tune this if there are monotonic edges or termination reflections showing up on your signals.

Tip: Change the logic thresholds for the digital command bus on the CMD Bus & Decode dialog.

Command Bus Set Up and Decode

The DDR command bus can be input over an HDA125 High Speed Digital Analyzer and used to:

- Separate Read and Write bursts
- Trigger acquisition based on the occurrence of a particular command (e.g., trigger on Read command)
- Decode the command state, then generate a colored overlay to mark significant transitions on the digital bus trace and analog traces.

It is not necessary to apply the command bus to all these functions simultaneously, you can choose how it is to be used in DDR Debug Toolkit.

Tip: See the *HDA125 High Speed Digital Analyzer Operator's Manual* for instructions on connecting and deskewing the HDA125.

Supported Digital Signals

The digital signals to be probed when using the HDA125 depend on the Command Truth Table, which is unique to each JEDEC specification. Below are the Command Bus signals required for decoding by DDR Debug Toolkit. Signals marked with an asterisk (*) are the minimum required for R/W separation.

Memory Standard	JEDEC CMD Truth Table
DDR4	CS_n*, WE_n*, RAS_n*, CAS_n*, ACT*
DDR5	CS_n, CA0*, CA1*, CA3*, CA4*, CA9, CA10, CA12
LPDDR4 / LPDDR4X	CS_n, CA0, CA1*, CA2*, CA3*, CA4*

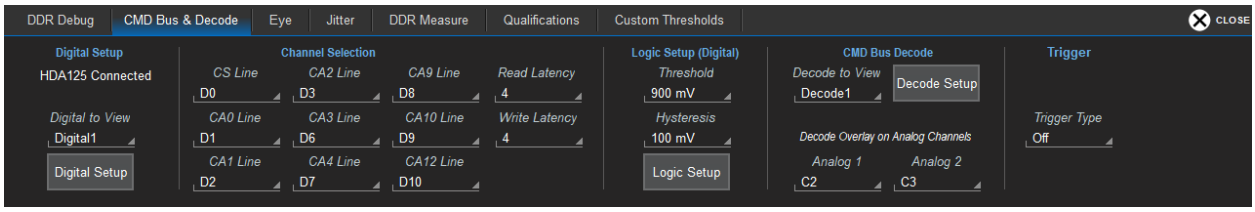
* Minimum required for R/W separation.

Read/Write Separation

Digital Read/Write Separation for DDR4, LPDDR4, LPDDR4X, DDR5

1. Following instructions in the HDA125 manual, configure any Digital*n* group to represent the DDR command bus.
2. On the DDR Debug dialog, choose to use the CMD Bus as the Read & Write **Separation Method**.
3. On the CMD Bus & Decode dialog, in **Digital to View**, select the Digital*n* (group) that represents the DDR Command Bus. This will populate the Channel and Logic fields with the settings configured for that group.

   Otherwise, use the Channel Selection fields to specify which digital lines make up the bus, and set the **Threshold** and **Hysteresis** for logic determination.



> Note: The dialogs are linked. Any changes made here will override the settings on the Digital*n* dialog and the Decode*n* dialog. If making a new setup, be careful to select a Digital group that can be overwritten.

4. Enter the **Read Latency** and **Write Latency**. The latency is the number of clock cycles that will lapse between the Read or Write command appearing on the bus and the beginning of the burst. These latency values are provided in the DRAM manufacturer's datasheet.
5. To change any of the digital thresholds, hysteresis, or inversion settings for individual lines, select the **Logic Setup** button.

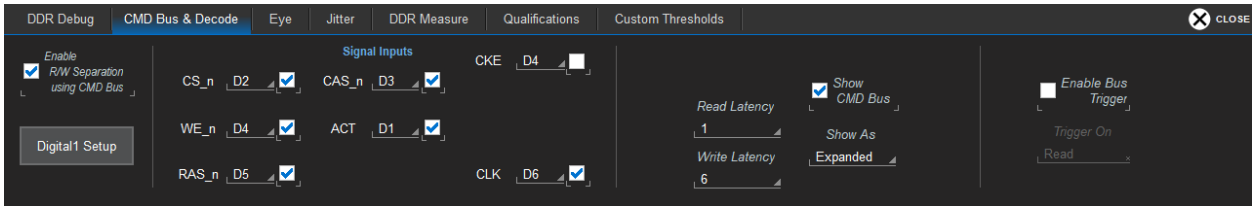
   This can be helpful in cases where input leads were accidentally reversed, or you find you get a better decoding with different levels or hysteresis.

   For example, when you reconnect tips to the HDA125 after having connected them to a DH Series probe, you may find the thresholds need to be reset, or that the signal needs inverting.

> Tip: To return to the DDR Debug dialogs, you can touch any open Eye descriptor boxes, or choose Analysis > DDR Debug.

Digital Read/Write Separation for All Other Standards

1. Following instructions in the HDA125 manual, configure Digital1 to represent the DDR Command Bus.
2. On the CMD Bus & Decode dialog, check **Enable Read/Write Separation using CMD Bus**. This will populate the Signal Input fields with the settings from the Digital1 dialog.



Note: The dialogs are linked, so any settings you change here will also affect the Digital1 group.

3. To change any of the line thresholds, hysteresis, or inversion settings, select the **Digital1 Setup** button to go to the digital dialogs, then open the **Logic Setup** tab. This can be helpful in cases where input leads were accidentally reversed, or you find you get a better decoding with different levels or hysteresis.
4. Enter the **Read Latency** and **Write Latency**. The latency is the number of clock cycles that will lapse between the Read or Write command appearing on the bus and the beginning of the burst. Thesse latency values are provided in the DRAM manufacturer's datasheet.
5. Check **Show CMD Bus** to turn on the display of the Digital1 bus. Choose to show the **Expanded** view of individual lines or the collapsed **Bus** trace.

Note: It is not necessary to view the bus to use it for R/W separation.

Bus Trigger

The Bus trigger helps with debug by allowing you to isolate problematic parts of the DDR signal. Using the HDA125 high-speed digital analyzer, you can probe the memory command bus to trigger acquisition on a variety of digital states. When Bus Trigger is enabled, the Trigger descriptor box shows the trigger type is DDR.

Bus Trigger for DDR4, LPDDR4, LPDDR4X, DDR5

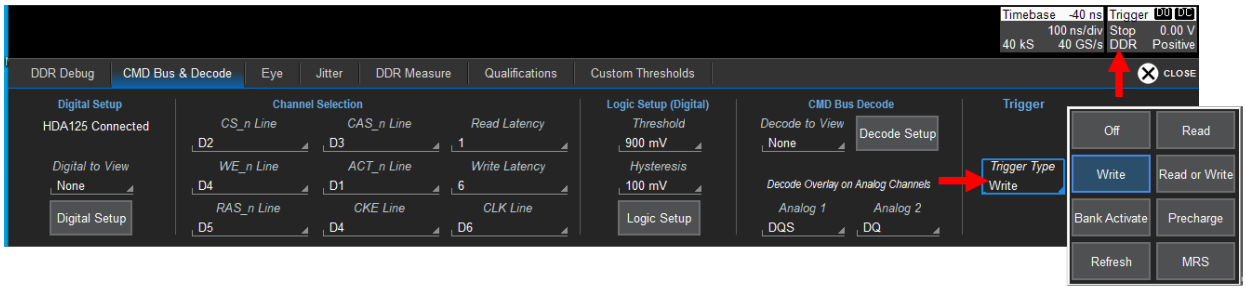
1. Following instructions in the HDA125 manual, configure any Digital*n* group to represent the digital inputs.
2. On the CMD Bus & Decode dialog, in **Digital to View**, select the Digital*n* (group). This will populate the Channel and Logic fields with the settings configured for that group.

   Otherwise, use the Channel Selection fields to specify which digital lines make up the bus, and set the **Threshold** and **Hysteresis** for logic determination.

   Use the **Digital Setup** button to go to the Logic Setup dialog if inverting is needed.

   Note: The dialogs are linked. Changes made here will override the settings on the Digital*n* dialog and the Decode*n* dialog. If making a new setup, be careful to select a Digital group that can be overwritten.

3. In **Trigger Type**, choose the DDR command to trigger on.



4. Make an acquisition of your analog and digital signals.

Bus Trigger for All Other Standards

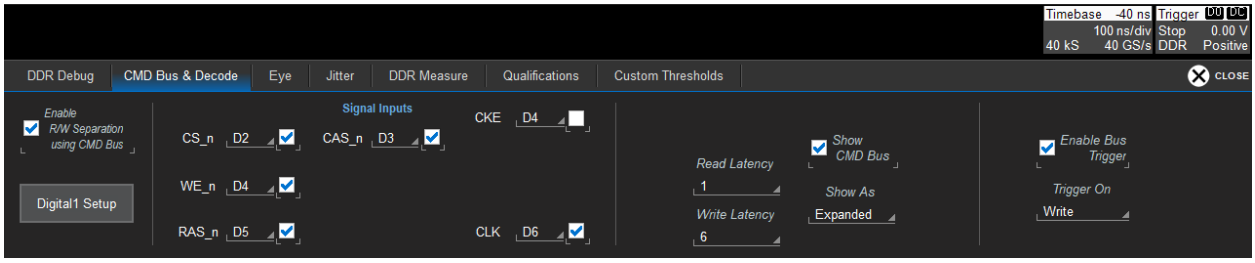
1. Following instructions in the HDA125 manual, configure the Digital1 group to represent the digital inputs and set the **Threshold** and **Hysteresis** for logic determination. You can use the **Digital1 Setup** button to open the Digital1 and Logic Setup dialogs.

   Otherwise, use the Channel Selection fields on the CMD Bus & Decode dialog to specify the inputs.

   Note: The dialogs are linked, so any settings you change here will also affect the Digital1 group.

2. On the CMD Bus & Decode dialog, check **Enable Bus Trigger**.

3. Choose the DDR command to **Trigger On**.



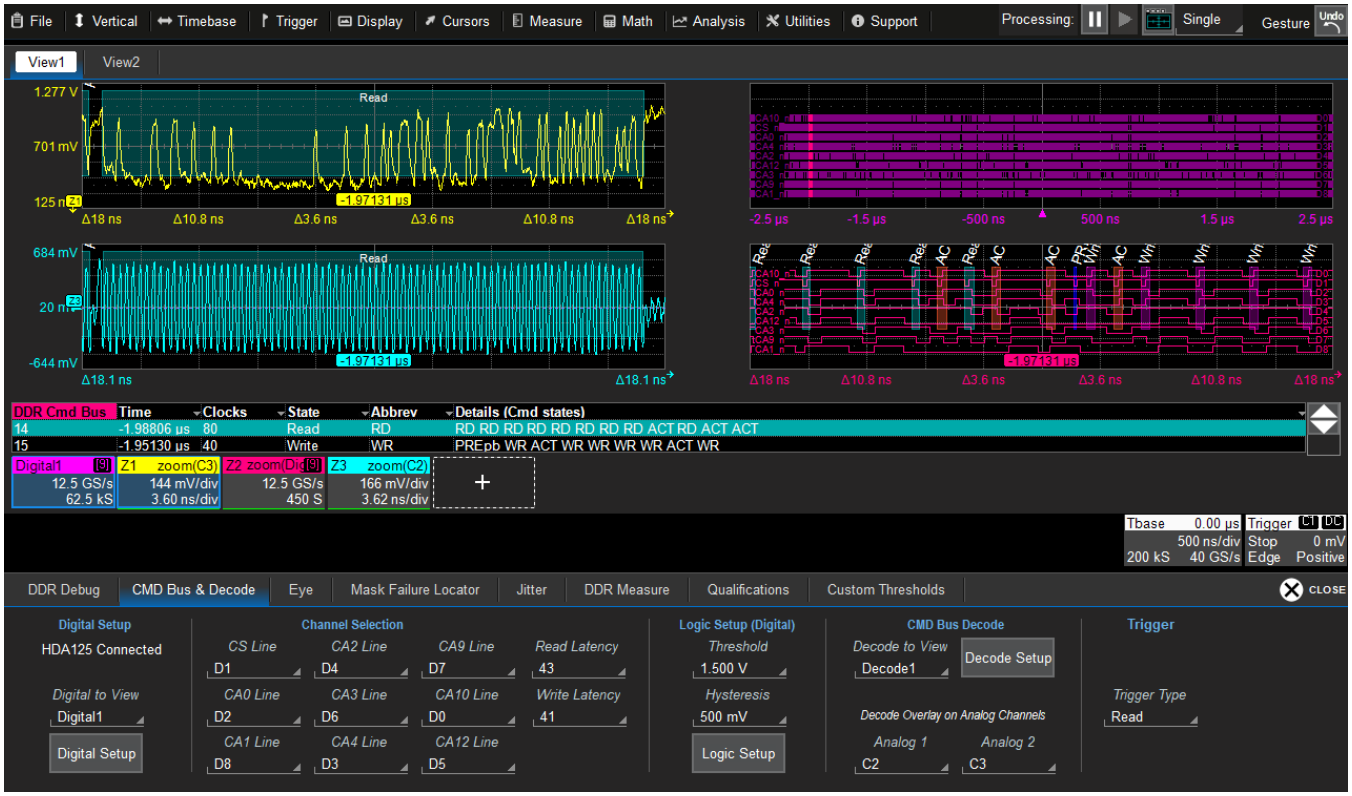
4. Make an acquisition of your analog and digital signals.

Bus Decode

Using Analysis Type Bus, DDR bus commands can be decoded and shown as time-aligned, color-coded overlays on zooms of both the digital and analog traces, helping you more easily view the relationship between the physical and protocol layers. A tabular readout shows the acquisition time, clock cycle, and command states.

Note: By default, Bus analysis sets up the DDR Command Bus Decode on Decode1 using the Digital1 group and the analog DQ and DQS signals as inputs. For DDR4, LPDDR4, LPDDR4x, and DDR5, the decoder, digital group and analog signals used can be changed. Only the digital command bus is decoded and used to derive an overlay that is placed on the digital and analog signals. Decoding is not available for all data types.

Bus Decode for DDR4, LPDDR4, LPDDR4X, DDR5



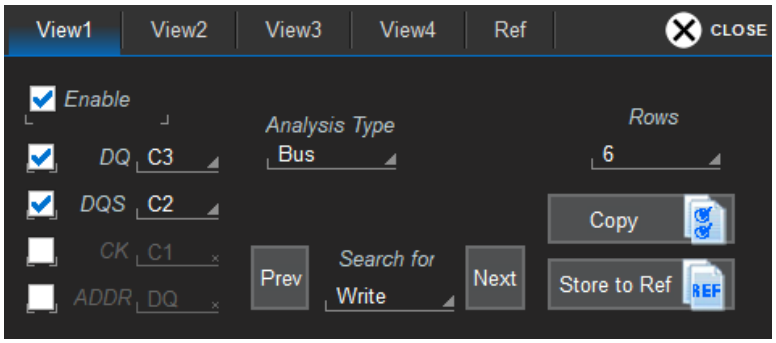
1. If you wish to change the Digital group or Decoder used, or to change the analog signals that receive the decoder overlay (e.g., "decode" a math function or Virtual Probe output signal), change the **Digital to View**, **Decode to View** or the **Analog 1/Analog 2** selections on the CMD Bus & Decode dialog *before* selecting Analysis Type Bus on the View subdialog.

   If you have not yet configured a Digital*n* group to match the HDA125 inputs, or you wish to change the digital lines displayed, do so on the CMD Bus & Decode dialog.

   Note: The dialogs are linked, and these settings will overwrite anything set up with the selected digital group or decoder.

2. Make at least one acquisition of your digital and analog signals.

3. On the View*n* subdialog, choose **Analysis Type Bus**.



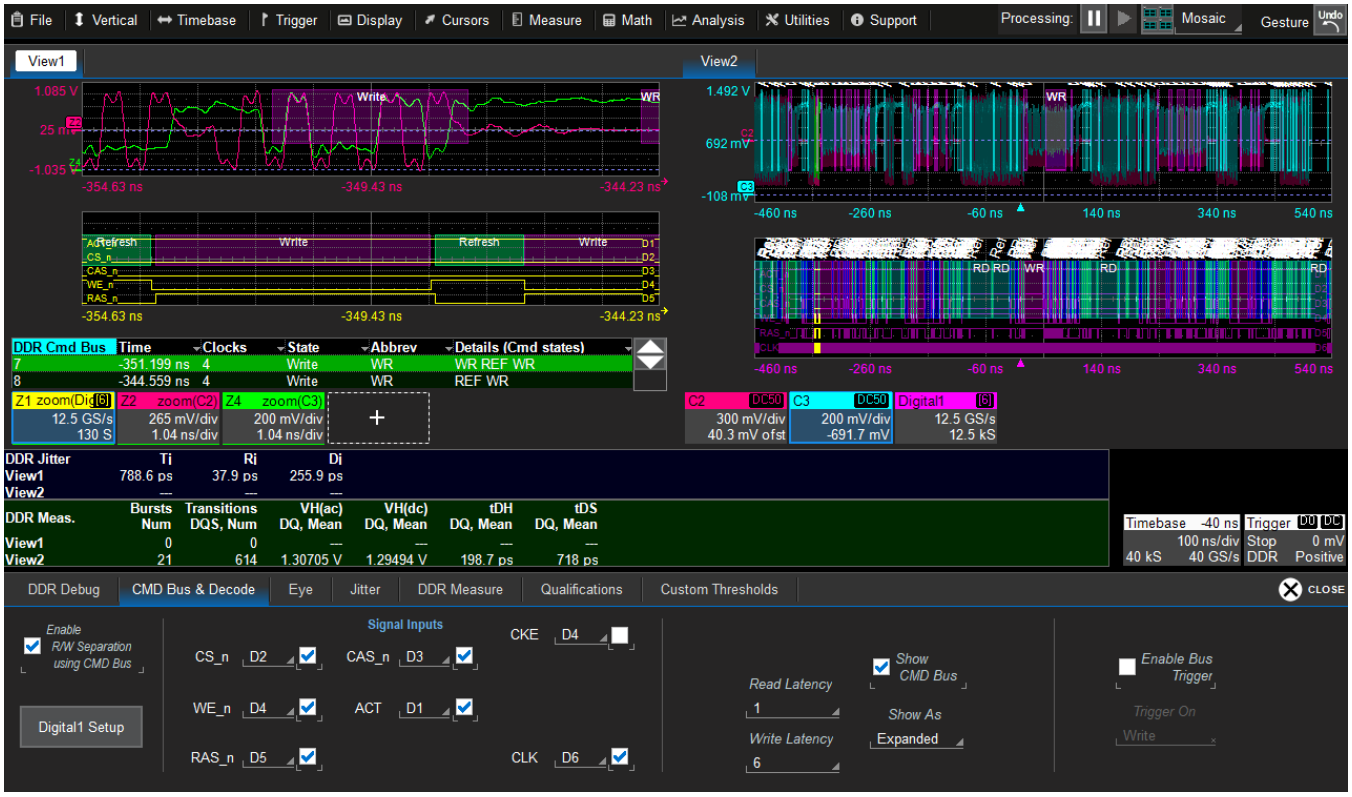
> **Note:** If you do not see a satisfactory decoding, you may need to modify the logic threshold/hysteresis of some digital lines. Return to the CMD Bus & Decode dialog and click the Logic Setup button to go to the digital setup dialogs. This is also helpful to invert lines that have accidentally been connected with reversed polarity.

4. Optionally, change the number of **Rows**shown in the decoder table.

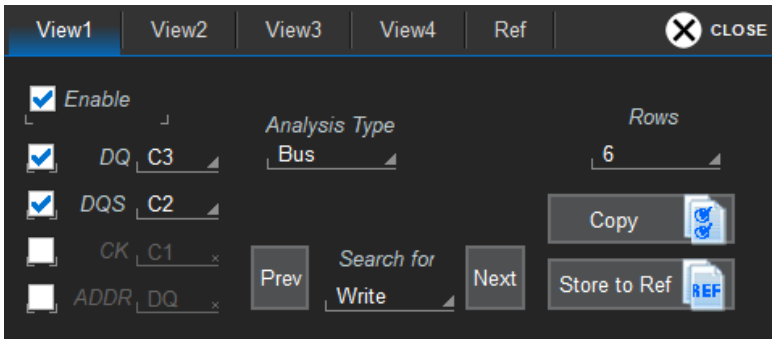
5. To nagivate the decoding, select the command to **Search for**, using the the **Prev** and **Next** buttons to show the previous or next occurrence of that command.

   Alternatively, select a row from the DDR CMD Bus decoder table. A zoom will be created and centered on the selected command.

Bus Decode for All Other Standards



1. If you have not yet configured Digital1 group to match the HDA125 inputs, or you wish to change the digital lines on display, change them on the CMD Bus & Decode dialog. Be sure to select Show CMD Bus if you wish to view the decoding over the digital lines as well as the DQ and DQS signals.
2. Make at least one acquisition of your digital and analog signals.
3. On the View*n* subdialog, select Analysis Type Bus.



Note: If you do not see a satisfactory decoding, you may need to modify the logic threshold/hysteresis of some digital lines. Return to the CMD Bus & Decode dialog and click the Digital1 button to go to the digital setup dialogs. This is also helpful to invert lines that have accidentally been connected with reversed polarity.

4. Optionally, change the number of Rows to show in the decode table.
5. To nagivate the decoding, on the View*n* subdialog, select the command to Search for, using the the Prev and Next buttons to show the previous or next occurrence of that command.

   Alternatively, select a row from the DDR CMD Bus decoder table. A zoom will be created and centered on the selected command.

Bus Commands Decoded

Below are the DDR commands by standard decoded and their abbreviations on the CMD Bus Decode overlay.

DDRx Commands Decoded	Abbreviation	DDR4	DDR5
Bank Activate	ACT	•	•
Device Deselected	DES	•	
Invalid, End Marker	end		•
Multi-Purpose Command	MPC		•
Mode Register Read	MRR		•
Mode Register Set	MRS	•	
Mode Register Write	MRW		•
No Operation	NOP	•	•
Power Down Entry	PDE	•	•
Power Down Exit	PDX	•	
Precharge	PRE / PREpb	•	
Precharge All	PREab		•
Precharge Same Bank	PREsb		•
Read	RD	• [1]	•
Refresh	REF	•	
Refresh Management Same Bank	RFMsb		•
Refresh Same Bank	REFsb		•
RFU	RFU		•
Self Refresh Entry	SRE	•	•
Self Refresh Entry with Freq Change	SREF		•
Self Refresh Exit	SRX		
VrefCA Command	VrefCA		•
VrefCS Command	VrefCS		•
Write	WR	• [1]	•
Write Pattern	WRP		•
ZQ Calibration	ZQC	•	

• Supported when all digital lines are probed on the Command Bus.

• [1]Cannot distinguish RDS4, RDS8, RDA, RDAS4, RDAS8, WRS4, WRS8, WRA, WRAS4, WRAS8.

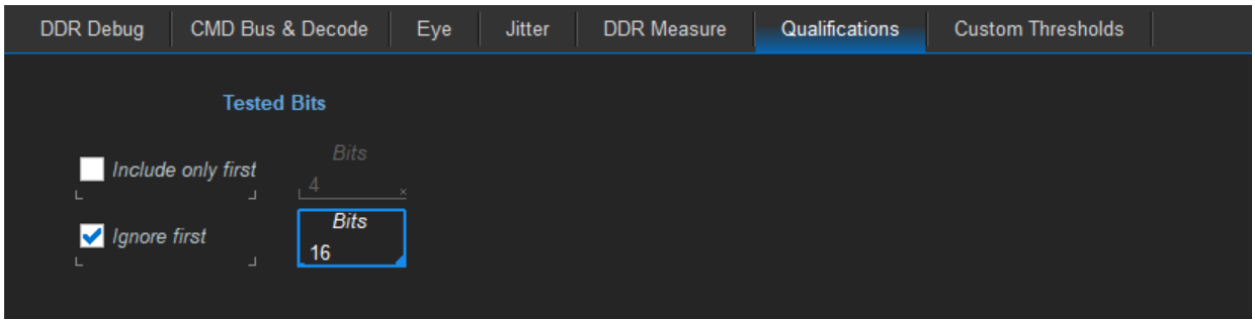
LPDDRx Commands Decoded	Abbreviation	LPDDR4 / 4X
Activate-1	ACT-1	
Activate-2	ACT-2	•
Bank Activate	ACT	•
CAS	CAS	
Deselect	DES	•
Invalid, End Marker	end	•
Mask Write	MWR	•
Mode Register Read	MRR	•
Mode Register Wr-1	MRW-1	
Mode Register Wr-2	MRW-2	•
Mode Register Write	MRW	•
Multi-Purpose Command	MPC	•
No Operation	NOP	
Power Down Entry	PDE	
Precharge	PRE	•
Read	RD	•
Read DQ Cal	RDC	
Read FIFO	RFF	
Read32	R32	
Refresh	REF	•
Reserved Future Use	RFU	•
Self Refresh Entry	SRE	•
Self Refresh Exit	SRX	•
Write	WR	•
Write FIFO	WFF	

• Supported when all digital lines are probed on the Command Bus.

Adding Qualifications

By using the built-in qualifiers, all the analyses in the DDR Debug Toolkit can be gated according to the specific qualifying conditions. This is a useful way to isolate specific areas of interest within a burst. Qualifications apply to all Views, including the Reference, and all measurements.

1. Open the **Qualifications** dialog.



2. Select the desired qualifiers:
   - **Include only first** "n" bits in the analysis
   - **Ignore first** "n" bits in the analysis
3. Enter the number of bits for each active qualifier.

Note: The qualifiers are additive. For example, if "Include only first" is set to 4 bits, and "Ignore first" is set to 1 bit, this would result in only the second and third bits in each burst being analyzed. If "Ignore first" is greater than or equal to "Include only first", all bits are filtered out of the analysis.

DDR Analysis

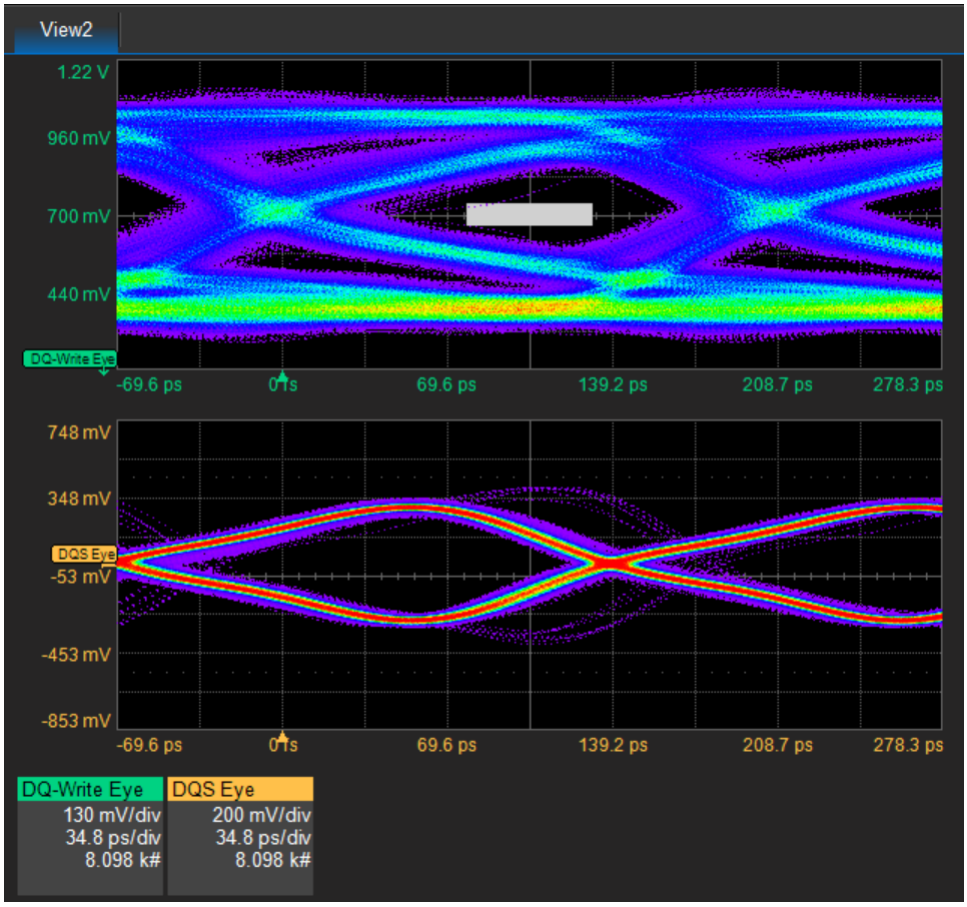
Eye Diagram Analysis

Primary eye diagrams based on the Analysis Type are displayed simultaneously for each enabled DDR View. An optional, reference 2nd Eye can be displayed with it. Eye appearance and scale are controlled from the Eye dialog.

Eye diagrams are built using either a single sweep or over multiple sweeps. Depending upon the Analysis Type selected for the View, they are filtered to display all acquired Read or Write unit intervals (UI). The eye diagram overlays every DQ or DQS bit in each detected burst and aligns them in time according to the timing reference.

Eye mask testing can be applied to the primary eye, with failure indicators showing where the signal violates the mask limits. Standard mask selections are available for all supported DDR standards, or you can upload custom mask files.

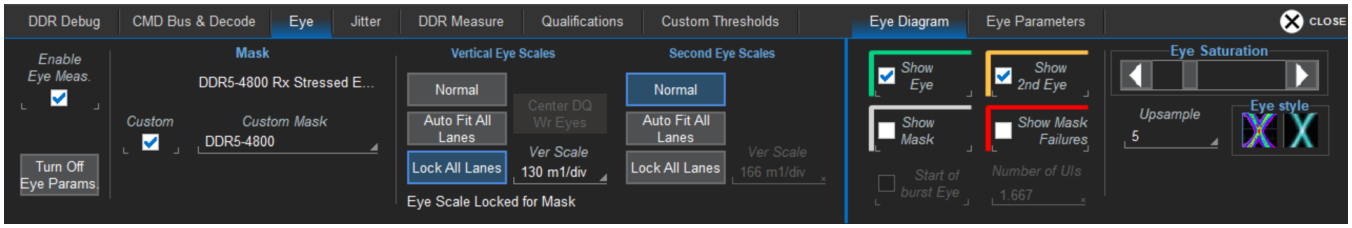
A selection of eye parameters is also available. All selected eye measurements are calculated for each enabled View.



Primary eye with mask test and reference 2nd Eye.

Creating Eye Diagrams

Touch the Eye tab to access the Eye dialog and its two sub-dialogs: Eye Diagram and Eye Parameter.



Select **Enable Eye Meas.** in the upper left corner of the Eye dialog to turn on eye measurements.

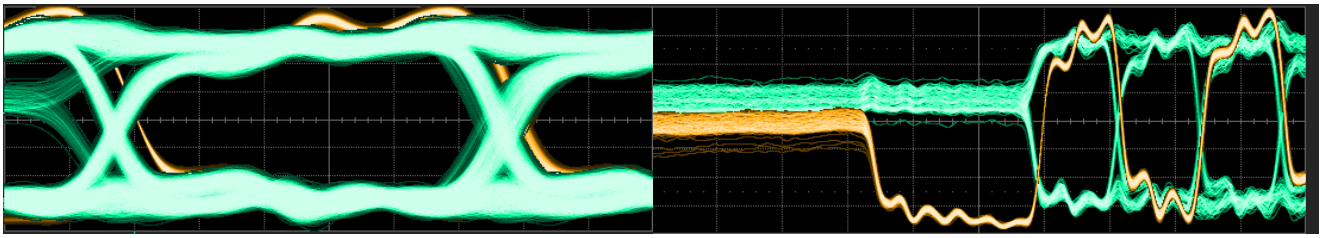
Use the Eye Diagram subdialog to select which eyes are displayed:

- **Show Eye** creates the eye for the primary signal (Analysis Type selection on the main DDR Debug Dialog).
- **Show 2nd Eye**creates the eye for the secondary signal (2nd Eye selection on the main DDR Debug Dialog).

Number of UIs allows you to specify the extent of the UI to display in each eye diagram. The default is 1.667, a full UI with about a third extended on each side.

While traditional eye diagrams overlay all acquired bursts into a single image, the **Start of Burst Eye** will display bursts sequentially, which is especially useful for understanding how a system transitions from an idle state to a burst. In this eye diagram, the first bit of each burst is horizontally aligned (preambles, first bits, second bits, etc.).

Tip: Increase the Number of UIs to see more of the signal when using the Start of Burst Eye.



Conventional eye and burst eye of same signal.

Eye Appearance

Eye Saturation adjusts the color grading or intensity. Use the slider to increase or decrease eye saturation. Slide to the left to reduce the threshold required to reach saturation.

The **Upsample** factor increases the number of sample points used to compose the eye diagram by interpolating points. Optionally, increase the value from 1 to a higher number (e.g., 5) to fill in gaps.

Note: Gaps can occur when the bitrate is extremely close to a submultiple of the sampling rate, such that the sampling of the waveform does not move throughout the entire unit interval. Gaps can also occur when using a record length that does not sample a sufficiently large number of unit intervals. Using record lengths of ≥ 1 million points is recommended in order to acquire tens of thousands, if not hundreds of thousands, of unit intervals.

Eye Style allows you to choose from color-graded or analog persistence styles.

With color-graded persistence  , pixels are given a color based on the pixel's relative population and the selected Eye Saturation. The color palette ranges from violet (lowest) to red (highest).

With analog persistence  , the color used mimicks the relative intensity that would be seen on an analog oscilloscope.In DDR Debug Toolkit, the secondary eye will be displayed in a dark orange color. Analog persistence is useful when the second eye is displayed.

Vertical Eye Scaling

The scale of the main Eye and 2nd Eye can be set separately.

- Normal uses the Volts/div of the eye diagram input trace.
- Auto Fit All Lanes sets the scaling of the eye pattern so that the one level is at the second vertical division above center, and the zero level is at the second division below center.
- Lock All Lanes sets the vertical scales to the value entered in the adjacent Ver Scale entry box.
- Center DQ Wr Eyes applies the required amount of horizontal shift to center DQ-Write eyes around the mask when one is enabled. Press it after turning on the mask test. The button is inactive for other types of eyes.

Note: If a mask is enabled, the controls for primary eye scaling are disabled. Only the 2nd Eye can be rescaled.

Eye Descriptor Box

The descriptor box for an Eye diagram includes following information:

- Top line: Volts/division of the eye
- Second line: Time/division of the eye
- Third line: the number of unit intervals (UI) displayed by the eye diagram

If cursors are enabled, cursor values appear in subsequent lines.

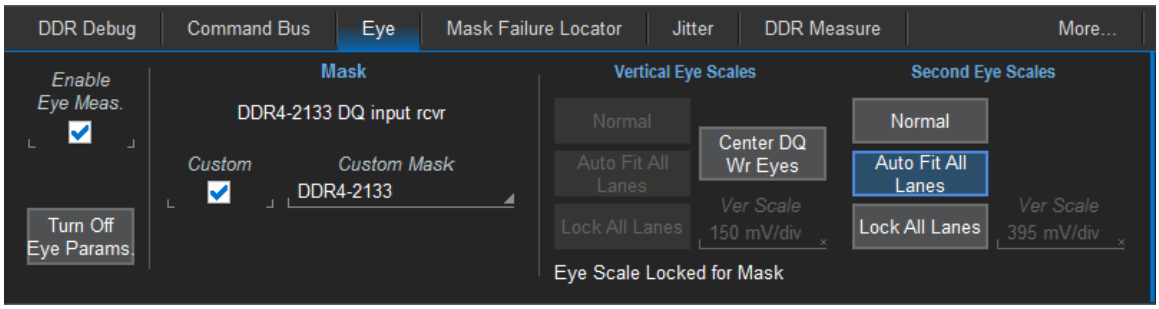
Eye Mask Testing

By showing where eyes violate mask limits, mask testing quickly shows where signals fail to conform to standard.

Selecting Masks

In the Mask section of the Eye dialog, select the mask to be used for eye diagram mask testing.

By default, the mask is configured to match the protocol and speed grade defined on the DDR Debug dialog. Alternatively, a custom mask can be entered by checking **Custom** and selecting the **Custom Mask** file.



Detail of eye mask test selections.

Note: Only masks containing "DDR" in the file name are visible from the Custom Mask field.

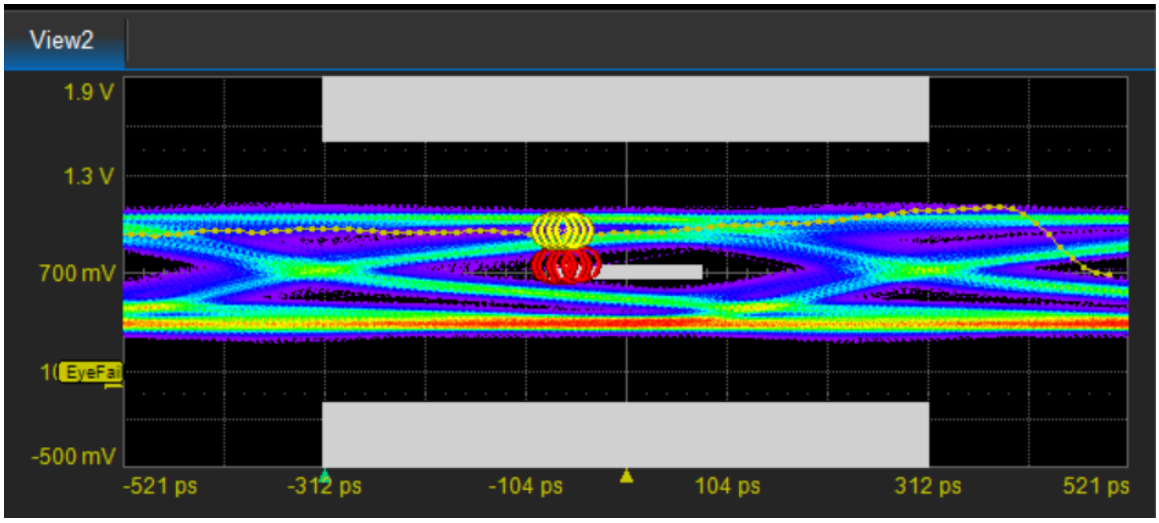
Display the mask over the eye by selecting the **Show Mask** and (optionally) **Show Mask Failures** boxes on the Eye Diagram subdialog.

Mask Failure Locator

The Mask Failure Locator dialog appears when Show Mask Failures is selected. Use it to quickly search for and take action upon finding mask test failures.

First, select the **View** to search for failures.

Check **Show Location** to mark the location of mask failures on the input trace.



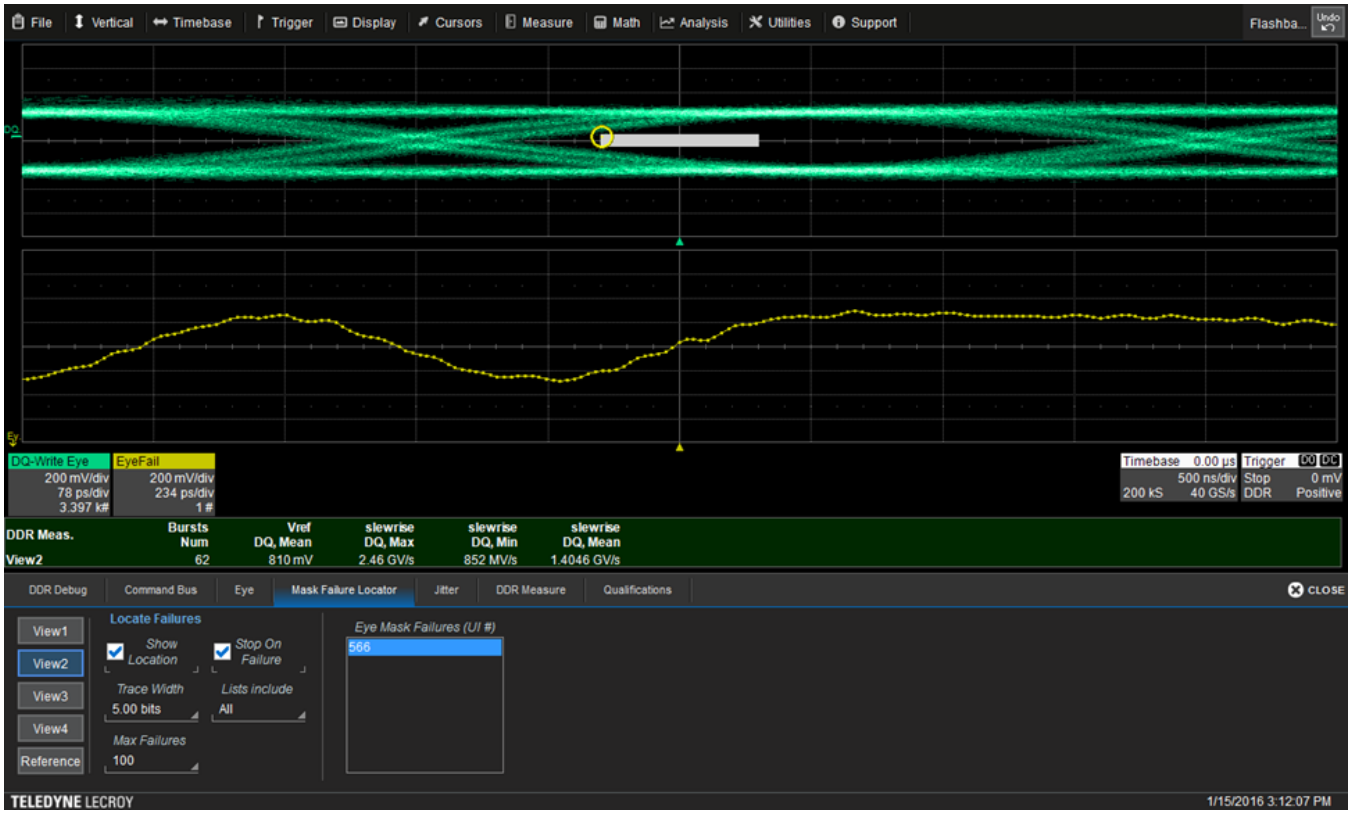
The red circles show all mask violations, while the yellow circles show the currently selected failure. The yellow dots shows the positions on the input trace where mask violations occurred over time.

Check Stop On Failure to stop acquisition whenever an eye mask failure occurs.

In Trace Width, enter the number of UIs surrounding the mask violation to display as "padding."

Enter the Max Failures to retain in the Eye Mask Failure list.

Select from the Eye Mask Failure list to mark and zoom to the location of that failure. Yellow circles appear on the eye diagram to show the location of the failure selected from the list.



Mask Failure Locator marks mask failures on original trace. Select a failure to create a zoom of that location.

Mask Definitions

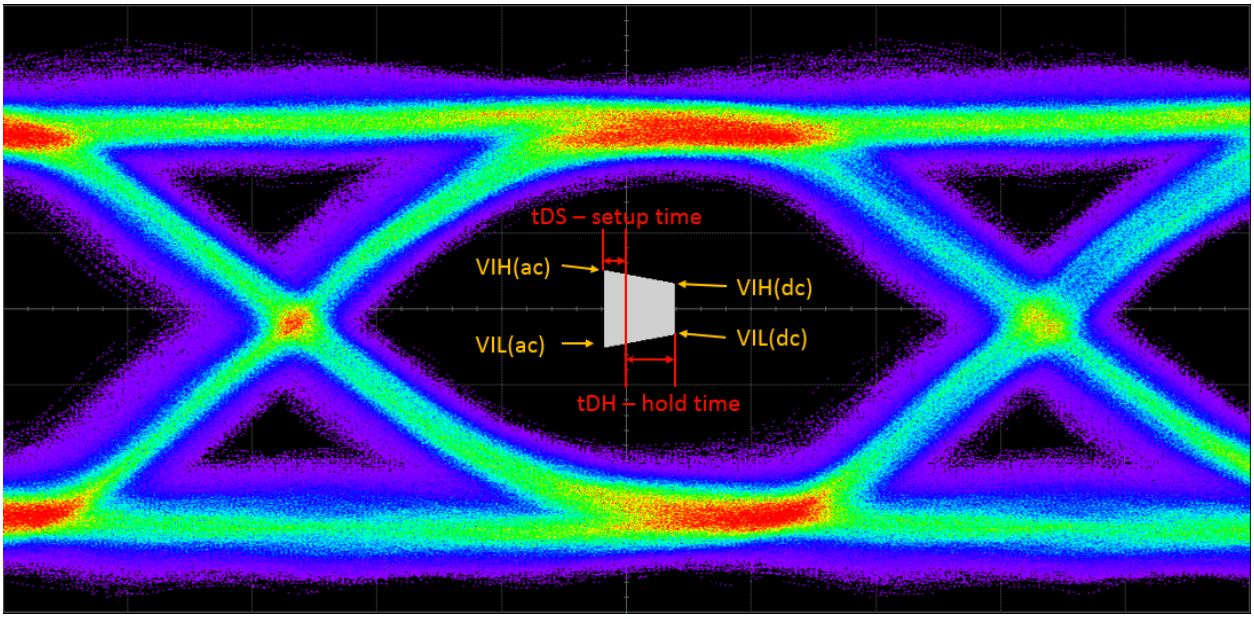
Masks are either "normalized" or "absolute":

- Normalized masks reference grid locations rather than absolute voltages.
- Absolute masks specify specific voltage and time values. When using absolute masks, the position of mask features will depend on the volts/div setting of the mask.

All of the default DDR masks are absolute. Following are the standard mask definitions included for selection in DDR Debug Toolkit.

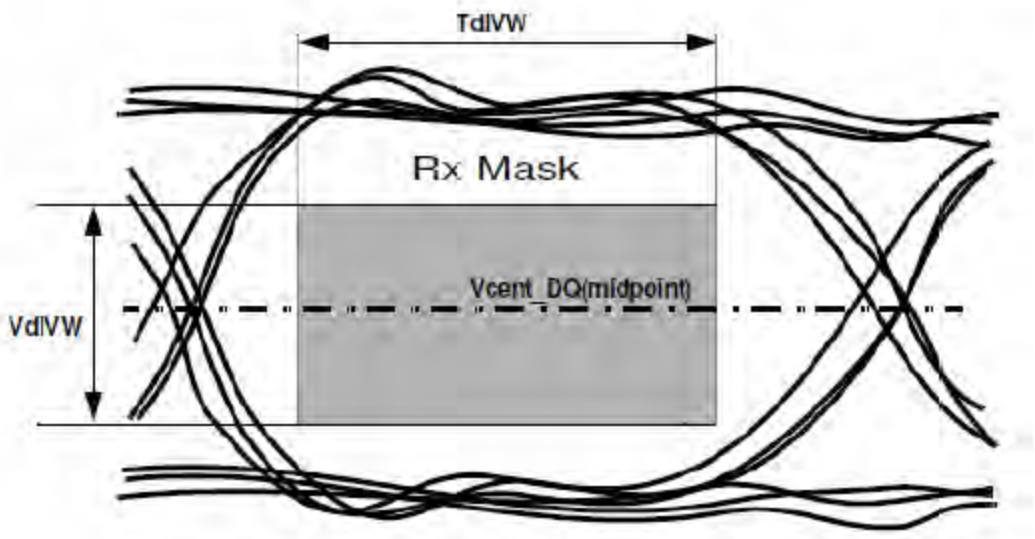
DDR2/3/3L and LPDDR2/3 Mask Definition

The DDR2, DDR3, LPDD2, and LPDDR3 specifications don't explicitly define a compliance mask. However, a mask for a valid data bit can be constructed using the setup and hold times. It is created as a normalized mask. The image below shows the definition for the mask.



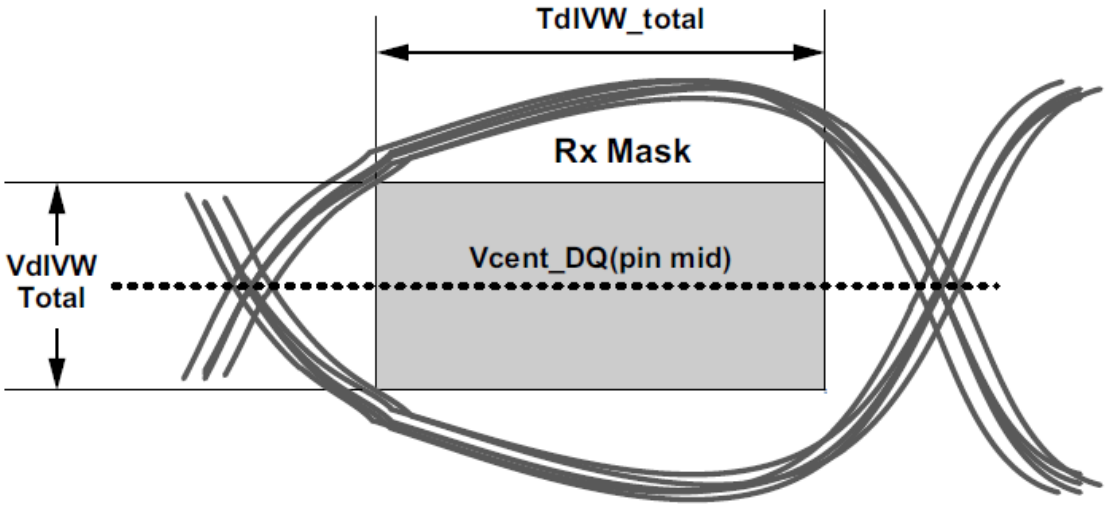
DDR4 Mask Definition

The DDR4 mask is defined by the JEDEC JESD79-4 specification. It is an absolute mask. The image below shows the definition for the mask.

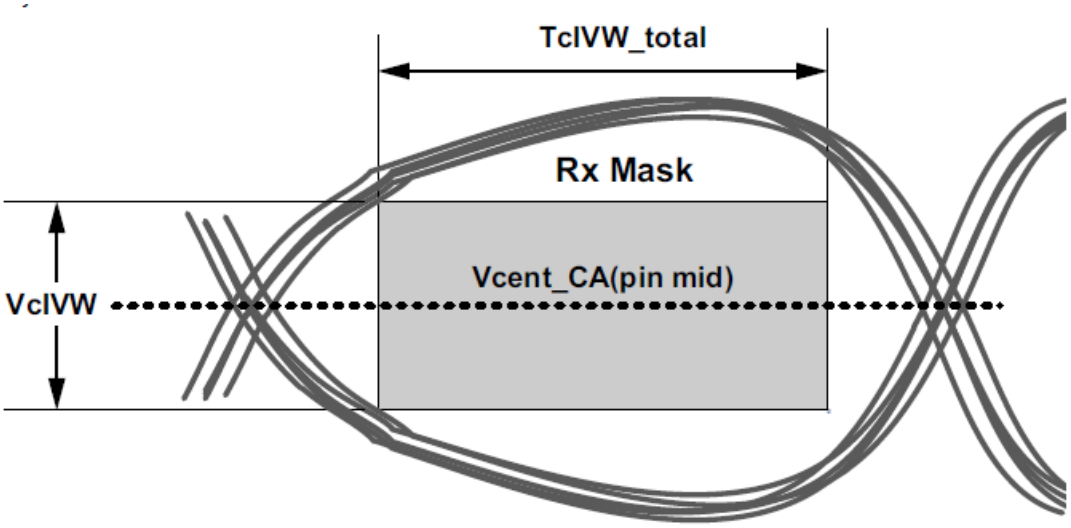


LPDDR4 and LPDDR4X Mask Definitions

The LPDDR4/LPDDR4X mask is defined by the JEDEC JESD209-B specification. There are two absolute masks, one each for the DQ and CA signals. The appropriate mask is automatically selected by the software. The images below show the definition of each mask.



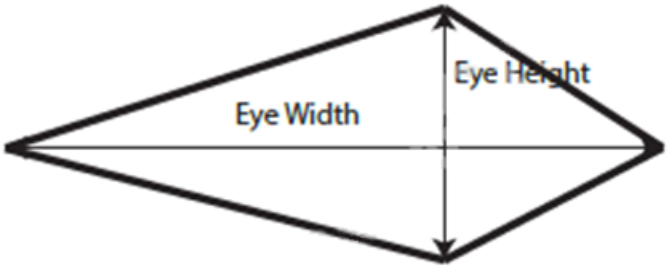
LPDDR4/LPDDR4X DQ mask.



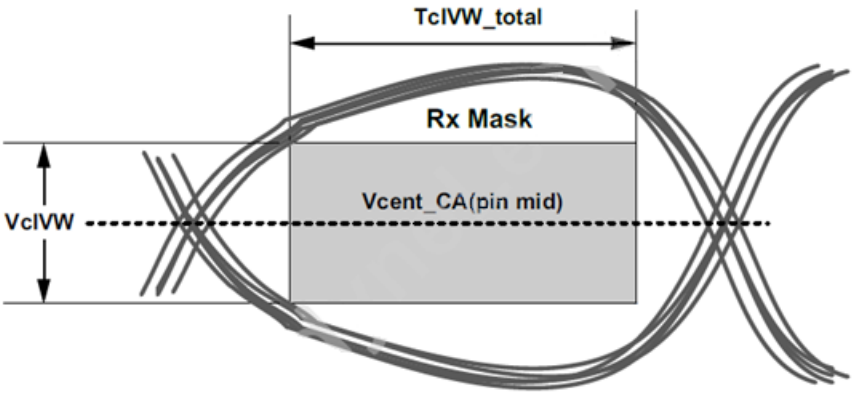
LPDDR4/LPDDR4X CA mask.

DDR5 Mask Definitions

The DDR5 masks are defined by the JEDEC JESD79-5 specification. There are two masks defined in the specification; a DQ Rx Stressed Eye Mask defined by Eye Height and Eye Width parameters and an absolute mask for CA signals.



DDR5 DQ Rx Stressed Eye mask.



DDR5 DQ CA mask.

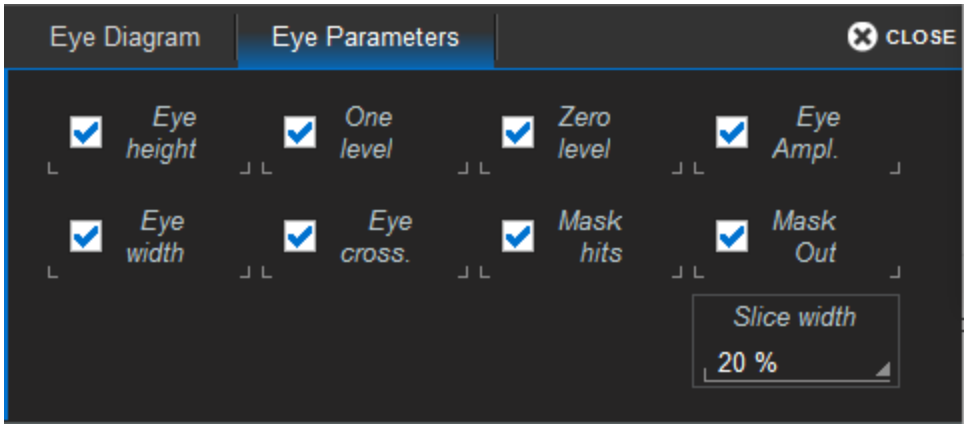
Eye Parameters

Up-to-eight standard eye measurements can be calculated simultaneously. All parameters are calculated across all enabled Views and displayed on the DDR Eye table. Measurements are made on the primary Eye in each view, the one resulting from the signal selected in the Analysis Type field.

DDR Eye	EyeHeight	EyeAmpl	EyeWidth	EyeCross	MaskHits
View1	510.4 mV	921.4 mV	546 ps	32.76 %	19.3005e+6
View2	584.3 mV	942.2 mV	579 ps	50.09 %	14.8613e+6
View3	1.168 V	1.573 V	585 ps	43.30 %	19.4384e+6
View4	1.547 V	1.849 V	611 ps	46.32 %	
Reference	---	---	---	---	---

Tip: To turn off all eye parameters (and hide the table), touch the Turn off Eye Params button located at the left side of the main Eye dialog.

Use the Eye Parameters subdialog to select the parameters to be displayed on the DDR Eye table.



Eye height is a measure of the signal-to-noise ratio of a signal. The measurement provides an indication of the eye opening and is made on the central region (normally 20%, user changeable) of the UI (bit period).

One level shows the simple mean of the 1 or high state of the eye within the selected slice width.

Zero level shows the simple mean of the 0 or low state of the eye within the selected slice width.

Eye Ampl.(itude) is a measure of the amplitude of the data signal. The measurement is made using the distribution of amplitude values in a region near the center of the eye (the "slice width") selected by the user (normally 20% of the distance between the zero crossing times). The simple mean of the distribution around the 0 level is subtracted from the mean of the distribution around the 1 level. This difference is expressed in units of the signal amplitude (normally voltage). This measurement algorithm is best suited to eye diagrams that are rendered from optical rather than electrical signals. In the presence of inter-symbol interference and/or equalization, it may not give reasonable results.

Eye width gives an indication of the total jitter in the signal. The time between the crossing points is computed by measuring the mean of the histograms at the two 0 crossings in the signal. Three times the standard deviation of each distribution is subtracted from the difference between these two means. This measurement algorithm is best suited to eye diagrams that are rendered from optical rather than electrical signals. In the presence of inter-symbol interference and/or equalization, it may not give reasonable results.

Eye cross.(ing) is the point where the transitions from 0 to 1 and from 1 to 0 reach the same amplitude. This is the point on the eye diagram where the rising and falling edges intersect. The eye crossing is expressed as a percentage of the total eye amplitude. The eye crossing level is measured by finding the minimum histogram width of a slice taken across the eye diagram in the horizontal direction (as the vertical displacement of this slice is varied).

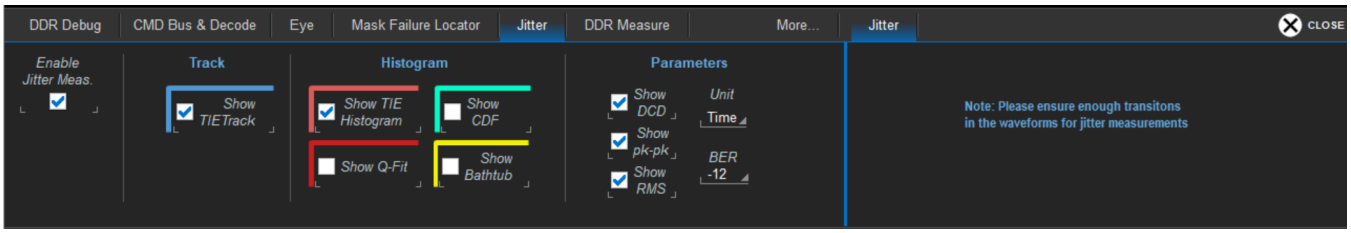
Mask hits is the number of samples where the signal impedes the mask.

Mask out is the number of samples where the signal does not impeded the mask.

You may also enter a Slice width. The slice width is a percentage of the duration of a single bit, indicating how much of the central portion of the bit width to use during vertical eye measurements.

Jitter Analysis

The Jitter dialog is the principal tool for setting up DDR jitter measurements.

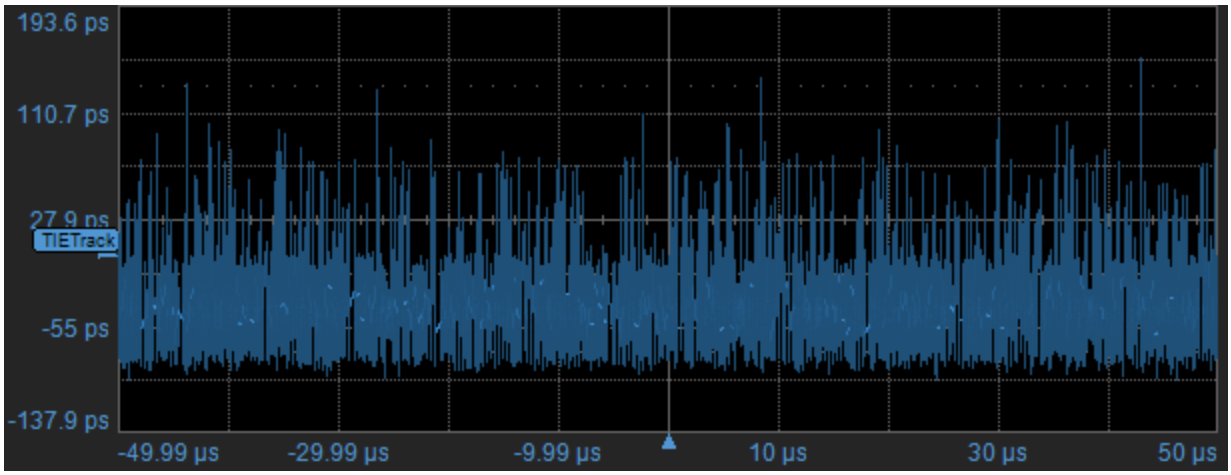


Select **Enable Jitter Measure** to turn on the jitter measurements. Deselecting this checkbox turns off the display of all jitter plots and parameters.

Jitter Track (TIE Track)

The TIE Trend, which only has a sample for each edge in the input waveform, is converted to what we call a track, or TIE Track, which is uniformly sampled at every UI, by interpolating samples for each UI where there was no edge (virtual edge). The TIE Track is also given a time axis.

Select **Show Tie Track** to plot the TIE results versus time.



TIE Track display.

Note: There is no control for TIE trend on the dialog. However, the TIE trend is calculated in the background and is used as an input for future calculations. TIE trend is calculated as the deviation of each edge from the ideal provided by the recovered clock (timing reference).

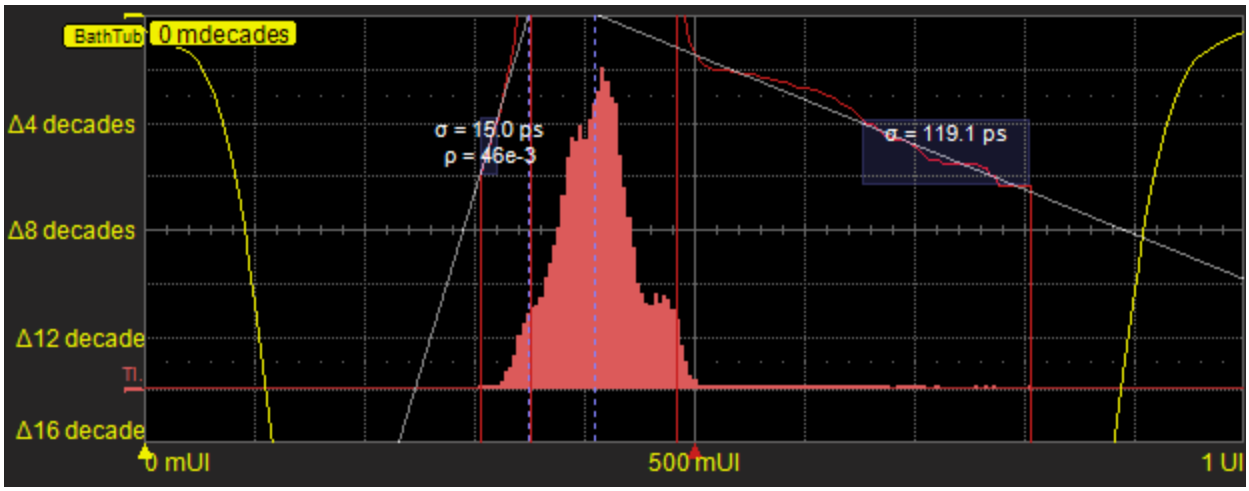
To zoom the TIE Track, select the TIE Track trace descriptor, then enter the new scale on the Zoom of Tie Track subdialog that appears next to the main Jitter dialog.

Select TIE Track descriptor rescale track.

Jitter Histogram

The TIE Histogram is updated with values from the TIE Trend and contains all sources of jitter. For multiple acquisitions, the histogram continues to accumulate until Clear Sweeps is pressed on the Front Panel.

Show TIE Histogram displays the TIE Histogram. The vertical axis is in number of edges in a particular jitter bin. The horizontal axis is the TIE jitter value. The scale is linear, but sometimes using the log10 math function to get a log vertical scale makes it easier to view the tails.



TIE Histogram display, with superimposed Bathtub curve and Q-fit plot.

Show Q-Fit superimposes the Q-Scale representation over the histogram. In the Q-Scale representation, Gaussian tails result in straight lines whose slope is equal to 1/Rj. Teledyne LeCroy uses a special Q-scale which we call nQ-Scale, or normalized Q-Scale. This allows for Gaussian distributions with variable populations or normalizations. Shown with the Q-scale transform is the best straight line fit (the thin white line).

Show CDF superimposes the integrated histogram of the Cumulative Distribution Function for the TIE Histogram.

Show Bathtub superimposes the more standard representation of CDF as a bathtub curve (same information as CDF, but shown in bathtub format).

Note: The Q-FIT, CDF, and Bathtub displays are linked to the histogram and always appear in the same grid as the histogram. They can be turned on/off, but not moved.

Zoom the histogram plots by touching the trace descriptor, and then rescaling on the Zoom subdialog that will appear. Zooming the TIE Histogram will also rescale any superimposed plots.

Jitter Parameters

The jitter parameters are calculated using Teledyne LeCroy's Dual-Dirac NQ-Scale. In the Dual-Dirac NQ-Scale, there are three free parameters that are fit to obtain each tail Gaussian: (1) the mean or mu, (2) the sigma, and (3) the population. A separate Gaussian is fit for both the left and right side of the distributions, so there are six parameters in all. The fit extrapolation for the NQ-scale model can be shown on the histogram for the NQ-scale model.

Jitter parameters are calculated across all active Views and are displayed on the DDR Jitter table.

DDR Jitter	Ti	Ri	Dj	DCD
View1	480.3 ps	34.2 ps	0.0 ps	13.516 ps
View2	423.5 ps	28.2 ps	25.6 ps	0 fs
View3	283.2 ps	17.0 ps	44.7 ps	18.503 ps
View4	---	---	---	0 fs
Reference	163.5 ps	7.5 ps	58.0 ps	---

Rj, Dj, and Tj are automatically calculated when you check Enable Jitter Measurement.

Note: In order to calculate Rj, Tj, and Dj the acquired waveforms need to have sufficient transitions. If insufficient transitions are detected, the jitter values will be reported as "--".

Other parameters are added to the table as selected from the Jitter dialog:

- Show DCD shows the difference in the means of the TIE for the rising edges and falling edges.
- Show pk-pk shows the measured pk-pk value of the TIE histogram.
- Show RMS to show the measured RMS of the TIE histogram.

Choose the Unit used to display jitter results, Time or UI.

Set the BER at which the Tj is reported, 10^{-12} by default.

DDR Measurements

With a toolbox of parameters specific to DDR, it is simple to quickly configure insightful measurements for validation, characterization and debug. Up-to-12 DDR measurements can be simultaneously displayed, each on a different Source signal with different statistics (min, max, mean, and number of measurement instances) calculated.

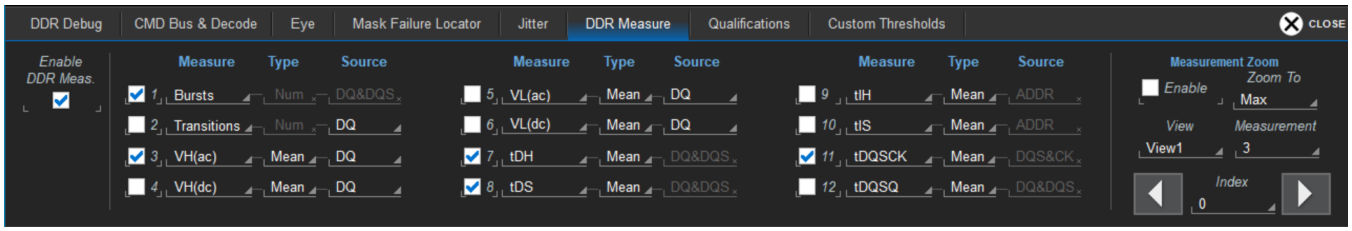
DDR Meas. Table

DDR measurement results are shown on the DDR Meas. table. Each measurement is calculated across all active Views, but using either Read or Write bursts, depending on how the View Analysis Type is configured. The measurement type and source signal are displayed where applicable.

DDR Meas.	Bursts Mean	Transitions DQ, Mean	Vref DQ, Mean	tDQSQ Mean	tDQSQ Max	tDH DQ, Mean	tDS DQ, Mean
View1	878	3.023e+3	945 mV	-101.52 ps	-31.8 ps	226.250 ps	101.52 ps
View2	875	3.527e+3	945 mV	8.25 ps	41.1 ps	347.4 ps	291.5 ps

Enable/disable the display of measurements using the Enable DDR Meas. checkbox in the upper left hand corner of the DDR Measure dialog.

Configuring the DDR Measure Table



For each measurement you wish to add to the table:

1. On the DDR Measure dialog, check the box to turn on the measurement, then touch the Measure field and choose from the standard DDR measurements.
2. Set Type to be mean, max, min, or number.

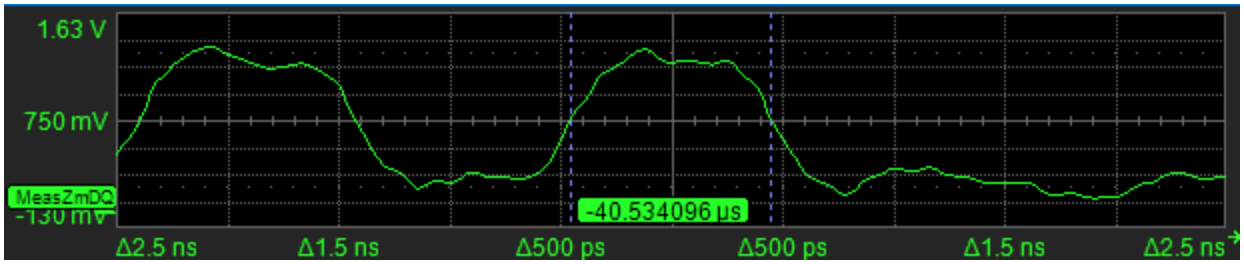
   Note: In order to display more than one statistical feature of a measurement, set up multiple measurement slots with the same measurement but a different statistic in each.

3. Choose the measurement Source signal.

   Note: Available measurement sources depend on the measurement. For measurements where there is only one viable selection (i.e., tDQSCK), the Source field is disabled.

Measurement Zoom

The exact location in the signal at which a measurement was taken can be quickly displayed by enabling Measurement Zoom. Select the View, the Measurement (by number), and type to Zoom To. A new trace appears marking the location on the Source signal. Use the Prev and Next buttons to move through the acquisition, or go right to a particular Index (occurrence) by entering the number, if you know it.



Measurement Zoom trace, showing location of measurement on source signal.

DDR Measurement Definitions

Bursts displays the number of bursts detected as a sum from all acquisitions. Either the number of Read or Write bursts will be measured depending upon what is selected as the Analysis Type. The measurement source is automatically set to DQ & DQS and the type is set to Num. A burst is detected by monitoring the state of the DQS signal. A hysteresis setting is used to detect a rising or falling edge coming out of idle in order to identify bursted activity. Once activity is identified, there is a bit counter which ensures that the activity is a valid burst.

Transitions displays the number of transitions as a sum from all acquisitions. The measurement source can be either DQ or DQS and the type is automatically set to Num. A transition is defined as any time DQ or DQS crosses the Vref level inside of a burst.

AC Logic High - VH(ac) measures the local maximum value from Vref to Vref of the high pulses in the acquisition. For a Read burst this is equivalent to VOH(ac) and for a Write burst this is equivalent to VIH(ac). The measurement source can be set to DQ, DQS, CK or ADDR.

DC Logic High - VH(dc) measures the local maximum value from VH(ac) to Vref of the high pulses in the acquisition. For a Read burst this is equivalent to VOH(dc) and for a Write burst this is equivalent to VIH(dc). The measurement source can be set to DQ, DQS, CK or ADDR.

AC Logic Low - VL(ac) measures the local minimum value from Vref to Vref of the low pulses in the acquisition. For a Read burst this is equivalent to VOL(ac) and for a Write burst this is equivalent to VIL(ac). The measurement source can be set to DQ, DQS, CK or ADDR.

DC Logic Low - VL(dc) measures the local minimum value from VL(ac) to Vref of the low pulses in the acquisition. For a Read burst this is equivalent to VOL(dc) and for a Write burst this is equivalent to VIL(dc). The measurement source can be set to DQ, DQS, CK or ADDR.

DQ to DQS Hold Time - tDH measures the hold time between DQ and DQS. The measurement source is automatically set to DQ & DQS. On a rising edge the hold time is measured between DQS at Vref and DQ at VH(ac). On a falling edge the setup time is measured between DQS at Vref and DQ at VL(ac). The measured values are not derated.

DQ to DQS Setup Time - tDS measures the setup time between DQ and DQS. The measurement source is automatically set to DQ & DQS. On a rising edge the setup time is measured between DQ at VH(ac) and DQS at Vref. On a falling edge the setup time is measured between DQ at VL(ac) and DQS at Vref. The measured values are not derated.

ADDR Hold Time - tIH measures the hold time between ADDR and CK. The measurement source is automatically set to ADD. On a rising edge the hold time is measured between CK at Vref and ADDR at VH(ac). On a falling edge the setup time is measured between CK at Vref and ADDR at VL(ac). The measured values are not derated.

ADDR Setup Time - tIS measures the setup time between ADDR and CK. The measurement source is automatically set to ADD. On a rising edge the setup time is measured between ADDR at VH(ac) and CK at Vref. On a falling edge the setup time is measured between ADDR at VL(ac) and CK at Vref. The measured values are not derated.

CK to DQS Skew - tDQSCK measures the skew between CK and DQS. The measurement source is automatically set to DQS and CK. For DDR2/3/4 and LPDDR4, the skew is measured from the CK rising edge at Vref to the nearest DQS rising edge at Vref within bursts. For LPDDR2/3, the skew is measured from the CK rising edge at Vref to the first DQS rising edge at Vref within each burst.

DQS to DQ Skew - tDQSQ measures the skew between DQS and DQ. The measurement source is automatically set to DQ and DQS. The skew is measured between DQS at Vref to DQ at Vref for all DQ transitions.

Slew rate of rising edge - slewRise measures the slew rate of the rising edges. The measurement source can be set to DQ, DQS, CK or ADDR.

Slew rate of falling edge - slewFall measures the slew rate of the falling edges. The measurement source can be set to DQ, DQS, CK or ADDR.

Reference Voltage - Vref measurement can be used to approximate what an ideal Vref value for the system would be. The measurement source is automatically set to DQ and the type is set to mean. This measurement will find the Top and Base of the acquired DQ waveform and then find the midpoint. This is measured once per acquisition and the displayed value is an average of all acquisitions.

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