Jitter measurements are a critical element in the analysis and certification of serial data systems. With symbol rates above 2.5 Gb/s common in many current designs, the need to accurately characterize jitter is more important than ever. Central to all jitter measurements is a reference clock against which the symbol timing must be measured. In an ideal situation, such a clock is available; but, in practice, this is often not the case. A reference clock, therefore, must be recovered from the signal under test. The method used to recover this clock has a direct effect on the jitter that is measured. Serial data standards such as PCI Express™ and Serial ATA address this by defining not only the jitter but also the specific method of clock recovery that is to be used in deriving the measurement. The choice of clock recovery method affects both the tracking ability as well as the total amount of jitter that can be measured. Flexible clock recovery in a jitter measurement system not only helps support the requirements of specific standards but can also be a powerful analysis tool, allowing you to predict the performance of real receivers.

**CLOCK RECOVERY**

A basic block diagram of a serial data receiver is shown in Figure 1. The receiver detects the transitions of the data stream, which is assumed to be NRZ for this discussion. The clock recovery block derives a sampling clock from the data edges by phase-locking a clock signal to the data transitions, using a phase locked loop (PLL). The action of the PLL generates a clock whose jitter follows that of the data for long-term variations in bit rate, but allows short-term variations to pass. The jitter rates that appear on the recovered sampling clock are determined by the low-pass filter in the PLL feedback loop. This design allows the receiver to be unaffected by relatively large changes in the average bit rate that occur over long time periods.

The detector determines the presence of a one or zero level using the recovered clock to locate the symbol boundaries and sampling the voltage at the nominal center of the symbol (unit interval or UI). The jitter that passes through the clock recovery circuit contains both random and deterministic components.

**TRANSMITTER JITTER**

The transmitter timing jitter is analyzed using a phase locked loop to recover the timing reference. In this respect, the jitter measurement system behaves like a serial data receiver. Phase error between the data stream and the recovered clock is analyzed in the jitter analysis function. The phase error represents the control signal that is used to adjust the frequency of the VCO to track the variations in the symbol rate of the signal under test. This phase error is exactly the jitter between the reference and the data transitions.
The steady-state phase error can be described in Laplace transform notation using the following equation:

$$\epsilon(s) = \frac{1}{1 + \frac{H(s)}{s}} \Phi_i(s) = \frac{s}{s + H(s)} \Phi_i(s)$$

The function $H(s)$ in equation (1) is the low-pass filter in the feedback path in Figure 2. The pole in the denominator $(H(s)/s)$ is from the conversion of phase to frequency in the VCO. The low-pass filter is selected to provide the desired properties in the phase-locked loop. This filter affects both the tracking characteristics and the jitter transfer function of the measurement system.

**CLOCK RECOVERY FILTER OPTIONS**

There are several choices that can be made for the configuration of the PLL loop filter. The commonly used golden PLL employs a simple scaling factor in the feedback path. This type of filter is specified for jitter measurements in several standards including Fibrechannel. A single-pole loop filter can be realized using a filter function of the form $H(s) = \omega_c$. The error signal has the following form:

$$\epsilon(s) = \frac{s}{s + \omega_c} \Phi_i(s)$$

with the cutoff frequency set by $\omega_c$.

Many serial data standards use spread spectrum clocking to control emissions. Spread spectrum clocking (SSC) modulates the symbol rate slowly over a small range. Typically, the spreading rate is 30 kHz, and the peak deviation of the bit rate is –0.5%. The signal rate in the presence of SSC can be viewed as a linear frequency shift vs. time ($f = f_0 + Ct$). The signal phase is the integral of the frequency; therefore, the SSC results in a phase that varies with $t^2$. Assuming the frequency variation starts at time $t=0$, the Laplace transform of the phase has the following form:

$$\Phi_i(s) = \frac{2C}{s^3}$$

Constant $C$ is the rate of change of the signaling frequency, and the steady-state error signal is found by taking the limit as $s$ approaches 0 of $\epsilon(s)$.

$$\lim_{s \to 0} \frac{s^2 2C}{s^3 \omega_n s + \omega_n^2} = \lim_{s \to 0} \frac{2C}{s^2(s + \omega_n)} = \alpha$$

This limit is expressed in equation (4), which indicates that the error grows continuously over time (infinite as $s$ approaches 0). In practical terms, a sufficiently high cutoff frequency in the filter will maintain a small error over a long, but finite, observation period.

A better choice for measuring signals with spread spectrum clocking is a second-order filter with a pole at the origin. This type of filter will track the spreading in the steady state, and has the form:

$$H(s) = \frac{2\zeta \omega_n s + \omega_n^2}{s}$$

The error function associated with this filter is:

$$\epsilon(s) = \frac{1}{1 + \frac{2\zeta \omega_n s + \omega_n^2}{s^2}} = \frac{s^2}{s^2 + 2\zeta \omega_n s + \omega_n^2}$$

The steady state error is found by plugging equation (3) into (6) and taking the limit as in equation (4). The limit is:

$$\lim_{s \to 0} \epsilon(s) = \lim_{s \to 0} \frac{s^2 2C}{s^3 \omega_n s + \omega_n^2} = \lim_{s \to 0} \frac{2C}{s^2(s^2 + 2\zeta \omega_n s + \omega_n^2)} = \frac{2C}{\omega_n}$$

The steady state error is constant in this case, so the loop tracks the SSC with a fixed phase offset.

Standard Serial ATA PHY II specifies this type of loop filter because of this property. Other standards that employ SSC, such as PCI Express™, can also benefit from this type of loop filter. While the latest version of the PCI Express compliance standard specifies a single-pole PLL filter, and that the signal be measured with SSC disabled, it is not always possible to do this. A second-order loop filter allows measurements to be made with SSC enabled.
**JITTER TRANSFER FUNCTION**

In addition to its tracking properties, the PLL also controls the frequency content of the jitter being measured. The phase error signal has a high-pass characteristic that is determined by the loop filter $H(s)$.

Figure 3 shows the jitter transfer functions for first-order and second-order phase locked loops from equations (2) and (6). The cutoff frequency of the first-order PLL and the natural frequency of the second-order PLL are set to 1.8 MHz. The actual cutoff frequency (3 dB point) of the second-order loop is shifted relative to its natural frequency by the following relationship:

\[
B_{3dB} = \frac{\omega_n}{2\pi} \left( 2\zeta^2 + 1 + \sqrt{(2\zeta^2 + 1)^2 + 1} \right)^2
\]

Equation (8) becomes $f_c = 2.06 f_n$ in terms of the cutoff and natural frequencies for a damping factor of 0.707. Equation (8) can be used to determine the natural frequency to achieve the desired cutoff.

The pass band of the error signal controls the amount of jitter that is measured for a given signal. Figures 4 through 6 in the appendix show jitter measurements on a 2.5 Gb/s PCI Express signal using several different PLL filters and cutoff frequencies. The measurements are made on the LeCroy SDA 6000A, which implements the jitter measurement function by processing signal threshold crossing times from a digitized acquisition of a serial data signal. As one would expect, the highest total jitter is measured with the lowest cutoff (100 kHz in this case). Using precise PLL cutoff frequencies allows the evaluation of the performance of specific receivers when presented with a particular data source. In this case, increasing the PLL bandwidth from 7 MHz to 22 MHz reduces the total jitter by 30% (130 ps $T_j$ to 89 ps $T_j$). This indicates that a large amount of the jitter is contained in the 7–22 MHz range. The jitter breakdown also indicates that approximately 24 ps of this additional jitter is deterministic and, therefore, is caused by systematic effects in the transmitter.

This type of jitter analysis gives a more precise view of the actual jitter performance of a given transmitter when viewed by a specific receiver. It is further possible to optimize the design of a receiver to work with a specific type of transmitter. Given a known range of PLL types and cutoff frequencies it is possible, using this tool, to guarantee the performance and interoperability of any transmitter.

**CONCLUSION**

A reference clock recovery function is an essential part of all jitter measurements. The properties of this function affect both the tracking ability as well as the amount of jitter that is measured from a serial data transmitter. Tracking is important for allowing accurate measurements in the presence of spread spectrum clocking while the high-pass cutoff frequency of the jitter transfer function of the clock recovery controls the amount of jitter that is measured. In this respect, the jitter measurement system can be made to emulate the operation of a serial data receiver. With this flexibility, real receiver performance can be accurately predicted.

**REFERENCES**

*Synthesizer Design for Microwave Applications*, Ulrich L. Rohde
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*The Fourier Transform and its Applications*, Ronald N, Bracewell

**APPENDIX**

![Figure 3: Jitter transfer function of first-order (red) and second-order (green) PLL with a cutoff frequency and natural frequency of 1.8 MHz. Note that the second order PLL has a more rapid roll-off than the first order PLL. The blue trace shows the second-order response with its natural frequency shifted as expressed in equation (8).](image-url)
Figure 4. Power spectrum (upper trace) and histogram (lower trace) of transmitter jitter with 100 kHz PLL filter. Note the large amount of low frequency jitter typical of clock generators used in serial data transmitters.

Figure 5. Jitter spectrum and histogram with 2-pole, 7 MHz PLL filter. The total jitter is significantly lower in this case due to the elimination of the large amount of low frequency jitter.

Figure 6. Jitter spectrum and histogram measured with 25 MHz PLL filter. Eliminating a significant amount of jitter below 25 MHz has a significant impact on the histogram, which becomes strongly bi-modal.