PCI Express 3.0 Characterization, Compliance, and Debug for Signal Integrity Engineers

- Transmitter Testing
- Receiver Testing
- Link Equalization Testing

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Product Marketing Manager
High Speed Serial Data
Agenda

- What is new about PCI Express (R) 3.0
  - Comparison to PCI Express (R) 2&1 Testing
  - What needs to be tested in PCI Express 3.0

- Teledyne LeCroy and the PCI-SIG

- SEG Compliance Testing
  - SEG Electrical Test Specifications
  - 5 Areas of Testing

- Live Demo
  - Tx Link Equalization Section 2.4
## PCI Express 3.0 Compared to PCIe 2&1

<table>
<thead>
<tr>
<th></th>
<th>PCI Express 2.0</th>
<th>PCI Express 3.0</th>
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</thead>
<tbody>
<tr>
<td><strong>Bit Rate</strong></td>
<td>5Gb/S</td>
<td>8Gb/s</td>
</tr>
<tr>
<td><strong>Encoding/Decoding</strong></td>
<td>8B/10B</td>
<td>128B/130B</td>
</tr>
<tr>
<td><strong>Overhead</strong></td>
<td>20%</td>
<td>1.5625%</td>
</tr>
<tr>
<td><strong>Scrambling</strong></td>
<td>Optional</td>
<td>Always</td>
</tr>
<tr>
<td><strong>Effective Bit Rate</strong></td>
<td>4Gb/s per lane</td>
<td>7.88Gb/s per lane</td>
</tr>
<tr>
<td><strong>Transmission path</strong></td>
<td>Same as Gen1</td>
<td>Same as Gen1 and Gen2</td>
</tr>
<tr>
<td><strong>Receiver Testing</strong></td>
<td>Informative</td>
<td>Required</td>
</tr>
</tbody>
</table>

![Diagram](image.png)
PCI Express 3.0 PHY Layer

Signal degrades over long transmission path and connectors

IC  System Board  PCIE Connector  Plug-In Card  IC
How does PCI Express 3.0 Work

**TxEQ**

**RxEQ**

**TxEQ – De-emphasis and Pre-shoot**

**RxEQ – DFE**

**RxEQ - CTLE**

Figure 4-69: Loss Curves for Behavioral CTLE

Figure 4-70: Equation and Flow Diagram for 1-tap DFE
How does PCI Express 3.0 Work

- Tx implements a FIR based equalization
- 1 of 11 presets are used during TxEQ process
- Equalization is based on 3 tap (pre cursor + post cursor) to create de-emphasis and pre-shoot

- Rx implements a behavior equalization algorithm
  - Behavioral CTLE
  - Behavioral DFE
  - Behavioral CDR

Rx with send TxEQ preset requests to Tx to optimize TxEQ to achieve **Dynamic Equalization** through link initialization.
PCI-SIG and LeCroy

1. PCI Express Committee and Workgroups
   - CEM (ElectroMechanical)
   - SEG (Serial Enabling Workgroup)

2. New SEG electrical spec v. 0.9
   - Official Compliance Logo Test is planned to begin in April 2013

3. PCI Express 3.0 Compliance Workshop (Gold Suites) Official Logo Testing in April 2013
   - Tx Electrical Testing (Supported by LeCroy)
   - Rx Electrical Testing (Supported by LeCroy)
   - Tx/Rx Link Equalization Testing (Supported by LeCroy)
   - PLL Testing (Supported by LeCroy)
According to the SEG electrical test specification version 0.9, there are 5 sections that need to be tested for PCI Express 3.0 for **Add-In cards** and **Systems**. Official PCI Express 3.0 Logo certification will begin April 2013.

<table>
<thead>
<tr>
<th>Section</th>
<th>Description</th>
<th>Covered by LeCroy</th>
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<tbody>
<tr>
<td>2.1</td>
<td>Tx Signal Integrity (Addin Card)</td>
<td>✓</td>
</tr>
<tr>
<td>2.2</td>
<td>Preset Test (Addin Card)</td>
<td>✓</td>
</tr>
<tr>
<td>2.3</td>
<td>TxEQ Test (Addin Card)</td>
<td>✓</td>
</tr>
<tr>
<td>2.4</td>
<td>Tx Link EQ Response Time Test (Addin Card)</td>
<td>✓</td>
</tr>
<tr>
<td>2.5</td>
<td>Tx Signal Integrity (System Board)</td>
<td>✓</td>
</tr>
<tr>
<td>2.6</td>
<td>Preset Test (System Board)</td>
<td>✓</td>
</tr>
<tr>
<td>2.7</td>
<td>Tx Link EQ Response Time Test (System Board)</td>
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</tr>
<tr>
<td>2.8</td>
<td>Receiver Jitter Tolerance (Addin Card)</td>
<td>✓</td>
</tr>
<tr>
<td>2.9</td>
<td>Receiver Jitter Tolerance (System Board)</td>
<td>✓</td>
</tr>
<tr>
<td>2.10</td>
<td>Receiver Link Equalization Test (Addin Card)</td>
<td>✓</td>
</tr>
<tr>
<td>2.11</td>
<td>Receiver Link Equalization Test (System)</td>
<td>✓</td>
</tr>
<tr>
<td>2.12</td>
<td>PLL Loopback Bandwidth (Addin Card only)</td>
<td>✓</td>
</tr>
<tr>
<td>2.13</td>
<td>Channel Testing (Not Required for Compliance)</td>
<td>✓</td>
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## PCI-SIG Logo Test Gold Suites

<table>
<thead>
<tr>
<th>Gold Test Suites</th>
<th>Test Coverage</th>
<th>Equipment List</th>
</tr>
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<tbody>
<tr>
<td>Transmitter Electrical</td>
<td>2.1 Add-in card Transmitter Signal Quality Test</td>
<td>13Ghz or higher Oscilloscope</td>
</tr>
<tr>
<td></td>
<td>2.2 Add-in card Transmitter Preset Test</td>
<td>Sigtest 3.2.0 or later</td>
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<tr>
<td></td>
<td>2.5 System Board Transmitter Signal Quality Test</td>
<td>CBB3 and CLB3</td>
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<tr>
<td></td>
<td>2.6 System Board Transmitter Preset Test</td>
<td></td>
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<tr>
<td>Receiver Electrical</td>
<td>2.8 Add-in Card Receiver Jitter Tolerance Test</td>
<td>13Ghz or higher Oscilloscope</td>
</tr>
<tr>
<td></td>
<td>2.9 System Receiver Jitter Tolerance Test</td>
<td>BERT</td>
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<tr>
<td></td>
<td></td>
<td>Sigtest 3.2.0 or later</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CBB3 and CLB3</td>
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<tr>
<td>Tx/Rx Link Equalization</td>
<td>2.3 Add-in Card Transmitter Initial TXEQ,Test</td>
<td>13Ghz or higher Oscilloscope</td>
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<tr>
<td></td>
<td>2.4 Add-in Card Transmitter Link Equalization Response Test</td>
<td>PeRT3 Phoenix</td>
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<td></td>
<td>2.7 System Board Transmitter Link Equalization Response Test</td>
<td>Sigtest 3.2.0 or later</td>
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<tr>
<td></td>
<td>2.10 Add-in Card Receiver Link Equalization Test</td>
<td>CBB3 and CLB3</td>
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<td></td>
<td>2.11 System Receiver Link Equalization Test</td>
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<tr>
<td>PLL Loop Bandwidth</td>
<td>2.12 Add-in Card PLL Bandwidth Test</td>
<td>13Ghz or higher Oscilloscope</td>
</tr>
<tr>
<td></td>
<td></td>
<td>BERT</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CBB3 and CLB3</td>
</tr>
</tbody>
</table>
Test Equipment and Fixtures

SDA 813Zi-A Oscilloscope

PeRT3 Phoenix BER Tester

Compliance Test Accessories
- High end SMA-SMA cable (2 pairs)
- Standard SMA-SMA cable (2 pairs)
- SMA-SMP cable (1 pair)
- SMA-BNC cable
- SMP extractor
- Power Splitter (2 pairs)
- DC blocks (1 pair)
- Short SMA-SMP cable (3 pairs)
- Torque Wrench

Compliance Test Fixtures
SEG Compliance Testing for PCI-SIG Certification

Gold Suite 1:
Tests 2.1/2.2/2.5/2.6 - Tx Signal Integrity

Gold Suite 2:
Tests 2.8/2.9 – Rx Signal Integrity

Gold Suite 3:
Tests 2.3/2.4/2.7 – Tx Link Equalization Response Test
Tests 2.10/2.11 - Rx Link Equalization Test

Gold Suite 4:
Tests 2.12 – PLL Loop Bandwidth Test
SEG Compliance Testing for PCI-SIG Certification

Tests 2.1/2.2/2.5/2.6 - Tx Signal Integrity

Tests 2.8/2.9 – Rx Signal Integrity

Tests 2.3/2.4/2.7 – Tx Link Equalization Response Test

Tests 2.10/2.11 - Rx Link Equalization Test

Tests 2.12 – PLL Loop Bandwidth Test
Transmitter Testing for PCI Express 3.0

Challenge: Normative Jitter measurements are required to be tested at the end of the channel with CTLE and DFE enabled, preset measurements are required to be tested prior to the channel.

Solution: The measurement tool (Oscilloscope) will embed the spec required channel (s4p) to simulate the lossy channel and the measurement will be done in the New PCIE Gen3 Sigtest Software. Sigtest software will also implement the necessary CTLE and DFE filters to open the eye.
Tx Preset tests

- Switch control on Compliance Base Board to request DUT to output different Tx Equalization presets.

<table>
<thead>
<tr>
<th>Preset Number</th>
<th>Preemphasis (dB)</th>
<th>De-emphasis (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>P4</td>
<td>0.0</td>
<td>0.0</td>
</tr>
<tr>
<td>P1</td>
<td>0.0</td>
<td>-3.5 ± 1 dB</td>
</tr>
<tr>
<td>P0</td>
<td>0.0</td>
<td>-6.0 ± 1.5 dB</td>
</tr>
<tr>
<td>P9</td>
<td>3.5 ± 1 dB</td>
<td>0.0</td>
</tr>
<tr>
<td>P8</td>
<td>3.5 ± 1 dB</td>
<td>-3.5 ± 1 dB</td>
</tr>
<tr>
<td>P7</td>
<td>3.5 ± 1 dB</td>
<td>-6.0 ± 1.5 dB</td>
</tr>
<tr>
<td>P5</td>
<td>1.9 ± 1 dB</td>
<td>0.0</td>
</tr>
<tr>
<td>P6</td>
<td>2.5 ± 1 dB</td>
<td>0.0</td>
</tr>
<tr>
<td>P3</td>
<td>0.0</td>
<td>-2.5 ± 1 dB</td>
</tr>
<tr>
<td>P2</td>
<td>0.0</td>
<td>-4.4 ± 1.5 dB</td>
</tr>
<tr>
<td>P10</td>
<td>0.0</td>
<td>See Note 2.</td>
</tr>
</tbody>
</table>
Preset test

Capture PCIe Gen3 compliance pattern with 11 presets and feed the results into sigtest.
Capture Compliance Pattern and Run SigTest

Sigtest 3.2.0 or later should be used for all measurements:
SEG Compliance Testing for PCI-SIG Certification

Tests 2.1/2.2/2.5/2.6 - Tx Signal Integrity
Tests 2.8/2.9 – Rx Signal Integrity
Tests 2.3/2.4/2.7 – Tx Link Equalization Response Test
Tests 2.10/2.11 - Rx Link Equalization Test
Tests 2.12 – PLL Loop Bandwidth Test
Challenge: Now that receiver testing is required. We need the test equipment to generate different types of jitter sources and signal conditions to replicate a real PCI Express 3.0 signal.

Solution: PeRT³ Phoenix has all the Built-in jitter sources and signal conditioning functions required for PCI Express 3.0 testing.

Signal with All Jitter sources added:
- De-emphasis = -6dB
- Pre-shoot = 3.5dB
- RJ = 2ps RMS at up to 1Ghz
- SJ = 13ps at 100Mhz
- Differential mode jitter = 14mV and 2.1Ghz
- Calibration channel = -20dB

Total Generated Jitter = 0.3UI to 0.35UI + Channel Effects
Step 1: Preset Calibration

- 11 presets will be calibration per Spec required method
- Main Preset for testing are P0, P4, P7, P8 and special preset (-6dB, 6dB)
Step 2: Rj and Sj calibration

- Rj and Sj will be calibrated at instrument output without going through fixture or channel
- Rj values will be readjusted for eye opening calibration later
- Sigtest is used for all measurement during calibration
Step 3: DM calibration

- DM will be calibrated at the end of the channel through the CBB3/CLB3 and riser card
- Eye height and Eye width will be calibrated at the end of the channel
Step 4: Eye height and Eye Width Calibration

- Eye Height and Eye width will be calibrated as the last step by varying Rj and DM only
- Sigtest applies CTLE/DFE and DUT loss package

<table>
<thead>
<tr>
<th></th>
<th>Eye Height (mV)</th>
<th>Eye Width (ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Add-In Card</td>
<td>46 +0/-5</td>
<td>41.25 +0/-2</td>
</tr>
<tr>
<td>System Board</td>
<td>50 +0/-5</td>
<td>45 +0/-2</td>
</tr>
</tbody>
</table>
Rx Jitter Tolerance

Signal with All Jitter sources added:
De-emphasis = -6dB
Pre-shoot = 3.5dB
RJ = 2ps RMS at up to 1Ghz
SJ = 13ps at 100Mhz
Differential mode jitter = 14mV and 2.1Ghz
Calibration channel = -20dB

Total Generated Jitter = 0.3UI to 0.35UI + Channel Effects

Perform RX Test
- Send Modified Compliance Pattern with all calibrated jitter sources turned on
- Pass if ≤ 1 error in 2:05
- 0 errors in 6:15 for 95% confidence of E-12 BER
SEG Compliance Testing for PCI-SIG Certification

Tests 2.1/2.2/2.5/2.6 - Tx Signal Integrity
Tests 2.8/2.9 – Rx Signal Integrity
Tests 2.3/2.4/2.7 – Tx Link Equalization Response Test
Tests 2.10/2.11 - Rx Link Equalization Test
Tests 2.12 – PLL Loop Bandwidth Test
Preset test (Section 2.3) Repeat?

- Capture PCIe Gen3 compliance pattern with 11 presets and feed the results into sigtest.
- Except this time, we don’t use the toggle switch on the CLB/CBB, Preset changes will be initiated through protocol request from the test equipment.
Tx Link Equalization Test

1) Does the Tx equalization respond to protocol level preset request?
2) Does the generated preset match the preset requested and within the response time?

Response time from Preset request to Preset response should be less than 1mS

Phoenix will send Tx preset request after Gen3 initialization protocols (Protocol Aware)
Test: Section 2.4 (or 2.7)

- Add-In (or System) Card Receiver Link EQ Test for 8.0 GT/s

Procedure

- Measure Response
  - Send EQ TS2 TX Preset P0
  - Change speed to 8G
  - Do equalization phases 0-3
    - Request Preset X (0..9)
    - Monitor transaction including request and response
    - Verify response time ≤ 500 ns
  - Continue into Loopback
  - Send Compliance Pattern
  - Capture waveform from DUT
  - Repeat for other presets

- Evaluate TxEQ
  - Feed waveforms into SigTest
  - Verify valid presets
SEG Compliance Testing for PCI-SIG Certification

Tests 2.1/2.2/2.5/2.6 - Tx Signal Integrity
Tests 2.8/2.9 – Rx Signal Integrity
Tests 2.3/2.4/2.7 – Tx Link Equalization Response Test
Tests 2.10/2.11 - Rx Link Equalization Test
Tests 2.12 – PLL Loop Bandwidth Test
## Rx Link Equalization Training

### Downstream Port

<table>
<thead>
<tr>
<th>Step</th>
<th>Action</th>
<th>Value 1</th>
<th>Value 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>EC = 01, Value C1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>EC = 01, Value C1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>EC = 10, Value C1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>EC = 10, Value C1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>EC = 10, Value C1’</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>EC = 10, Value C1’</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>EC = 11, Value C2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>EC = 11, Value C2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>EC = 11, Value C2’</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>EC = 11, Value C2’</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>EC = 00, Value C2'</td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>EC = 00, Value C2'</td>
<td></td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>IDL1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>IDL1</td>
<td></td>
<td></td>
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<td>15</td>
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<td>16</td>
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<td>17</td>
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<td>18</td>
<td>IDL1</td>
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<tr>
<td>19</td>
<td>IDL1</td>
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### Upstream Port

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<th>Value 2</th>
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<tbody>
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<td>1</td>
<td>EC = 00, Value C2</td>
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<td></td>
</tr>
<tr>
<td>2</td>
<td>EC = 01', Value C2’</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>EC = 10, Value C2’</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>EC = 10, Value C2’</td>
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<td></td>
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<tr>
<td>5</td>
<td>EC = 10, Value C2’</td>
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<td></td>
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<tr>
<td>6</td>
<td>EC = 10, Value C2’</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>EC = 11, Value C2’</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
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<td>10</td>
<td>EC = 11, Value C2’</td>
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<td></td>
</tr>
<tr>
<td>11</td>
<td>EC = 00, Value C2’</td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>EC = 00, Value C2’</td>
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<td>16</td>
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<td>17</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>IDL1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>IDL1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Diagram

![Diagram showing the connection between the Signal Generator, Error Detector, and AIC Under Test]
In order to test the adaptive capabilities of the Receiver Equalizer, the Test Equipment must be able to accept the optimized Tx equalization requests and transmit the corresponding de-emphasised signal **within 1mS** to change to each preset and a total of 12 tries.
Example: Section 2.10 (or 2.11)

- **Add-In (or System) Card Receiver**
  - **Link EQ Test for 8.0 GT/s**
- **Procedure**
  - Enable jitter for target eye
  - Send EQ TS2 P7 at 2.5G
  - Change speed to 8G
  - Do equalization phases 0-3
    - Record final requested cursor from DUT in phase 2 (or 3)
  - Continue into Loopback
  - Perform RX Test
    - Send Modified Compliance Pattern
    - Pass if ≤ 1 error in 2:05
    - 0 errors in 6:15 for 95% confidence of E-12 BER

**Generate Calibrated Eye**

**Perform full equalization and then enter loopback**

**Measure BER**
SEG Compliance Testing for PCI-SIG Certification

Tests 2.1/2.2/2.5/2.6 - Tx Signal Integrity
Tests 2.8/2.9 – Rx Signal Integrity
Tests 2.3/2.4/2.7 – Tx Link Equalization Response Test
Tests 2.10/2.11 - Rx Link Equalization Test
Tests 2.12 – PLL Loop Bandwidth Test
PLL Loopback Bandwidth Testing

4.3.3.12.2. 8.0 GT/s Tx PLL Bandwidth and Peaking

The Tx and Rx PLL bandwidth for 8.0 GT/s signaling is 2 – 5 MHz. Peaking may be from 0 to 2 dB for bandwidths up to 4 MHz and 0 to 1 dB for bandwidths up to 5 MHz. The 8.0 GT/s PLL BW range is substantially lower than the PLL bandwidths specified for 5.0 GT/s or 2.5 GT/s operation to reduce the amount of Refclk jitter at the sample latch of the receiver.

PLL bandwidth and peaking test is essentially a jitter transfer function measurement for a specific frequency range.
PLL Loopback BW Testing

Graph the generated SJ amplitude against measured SJ amplitude and the result is the jitter **transfer functions** of the DUT PLL.

Oscilloscope takes SJ measurement for each frequency of SJ generated on the Phoenix.

Phoenix will generate 100Mhz clock as the reference CLK and generate a sweep of SJ frequencies.

- **Frequency (MHz):** 3.9
- **Magnitude (dB):** -3.03
- **Peaking (dB):** 0.5
Live Demo – Link EQ Compliance

- LeCroy Generator
- Clock Out
- Error Detector
- Trigger Out
- LeCroy PeRT® Phoenix

- Data Rx+
- Data Rx-
- Data Tx+
- Data Tx-
- TX- TX+
- Phase matched SMA-SMA cable pair
- Phase matched SMA-SMP cable pair
- Power Dividers
- DC Blocks
- Terminator

- AUX IN
- Ch1
- Ch2
- Ch3
- Ch4
- LeCroy SDA830Zi-A

- Power Supply
- Terminator

- SMA-SMP cable pair

- Power Dividers
- DC Blocks
- Phase matched SMA-SMP cable pair

- Riser Card
- Add-In Card

- SMA-SMP cable pair

- Phase matched SMA-SMA cable pair
Test description: Verify the DUT response time to preset request during Link EQ training

The Test Script will:
1) Request DUT to initialize with P7
2) Request DUT to change from P7 to P1
3) Capture upstream and downstream waveforms during Link EQ handshake and display the waveform in scope and ProtoSync
4) Measure time between Preset Request and Preset response

Pass/Fail Target: response time must be less than 1 microsecond
LeCroy PeRT³ is capable of protocol level handshake to send and receive TxEQ commands.

LeCroy PeRT³ is also a full blown BERT and Signal conditioner for Jitter generation and programmable De-emphasis controls.
Conclusion:

The Most Comprehensive and Only Protocol Aware Test Tools for PCI EXPRESS Specification Gen 3.0