Xena Z2244

UALink Traffic Generator



Key Features

- Supports 800G, 400G & 200G port speeds using 224G PAM4 SerDes
- Supports 400G, 200G & 100G port speeds using 112G PAM4 SerDes
- Stateful UALink UPLI Originator and Completer
- Raw TL Flit Generation
- TL & DL capture and analysis
- DL messaging generator, capture and analysis
- Advanced Physical Layer testing
- Quiet & compact chassis suitable for desktop use
- Intuitive, platform-independent web UI for easy configuration and live monitoring
- Python-based open-source automation framework (XOA)

The Xena Z2244 delivers comprehensive validation of UALink implementations across 224G and 112G SerDes interfaces, supporting wire-speed traffic generation at 4 speeds up to 800Gb/s per device.

The Xena Z2244 UALink Traffic Generator is the industry's first integrated Ultra Accelerator Link™ (UALink™) traffic generation and error injection test solution.

It builds on Teledyne LeCroy's extensive expertise in high-speed interconnect validation, including industry-leading PCI Express and Ethernet traffic generation solutions and protocol analysis.

The platform enables engineering teams to validate UALink implementations under realistic traffic conditions, quickly identify performance bottlenecks, verify interoperability, and reduce deployment risk in large-scale AI environments.

Equipped with a high-speed OSFP-1600 IHS interface, the Xena Z2244 supports optical transceivers as well as active and passive copper cables and testing of next-generation UALink chips, switches, xPUs, and NICs.

It provides an enhanced stateful UALink UPLI Originator and Completer, as well as UALink Data Link (DL) and Transaction Layer (TL) Flit Traffic Generator, detailed statistic and error injection with advanced Capture Buffer readouts, Flit headers and logs providing full visibility on the Flit data structure.

Xena Z2244 offers an extensive range of advanced Layer 1 features, including comprehensive PCS and PMA layer testing as well as ANLT support.

The Z2244 is a quiet and compact 1U chassis solution that can be used both in a rack as well as a desktop solution, where temperature continuously is monitored on system and inserted mediums to obtain optimal cooling and minimal noise.

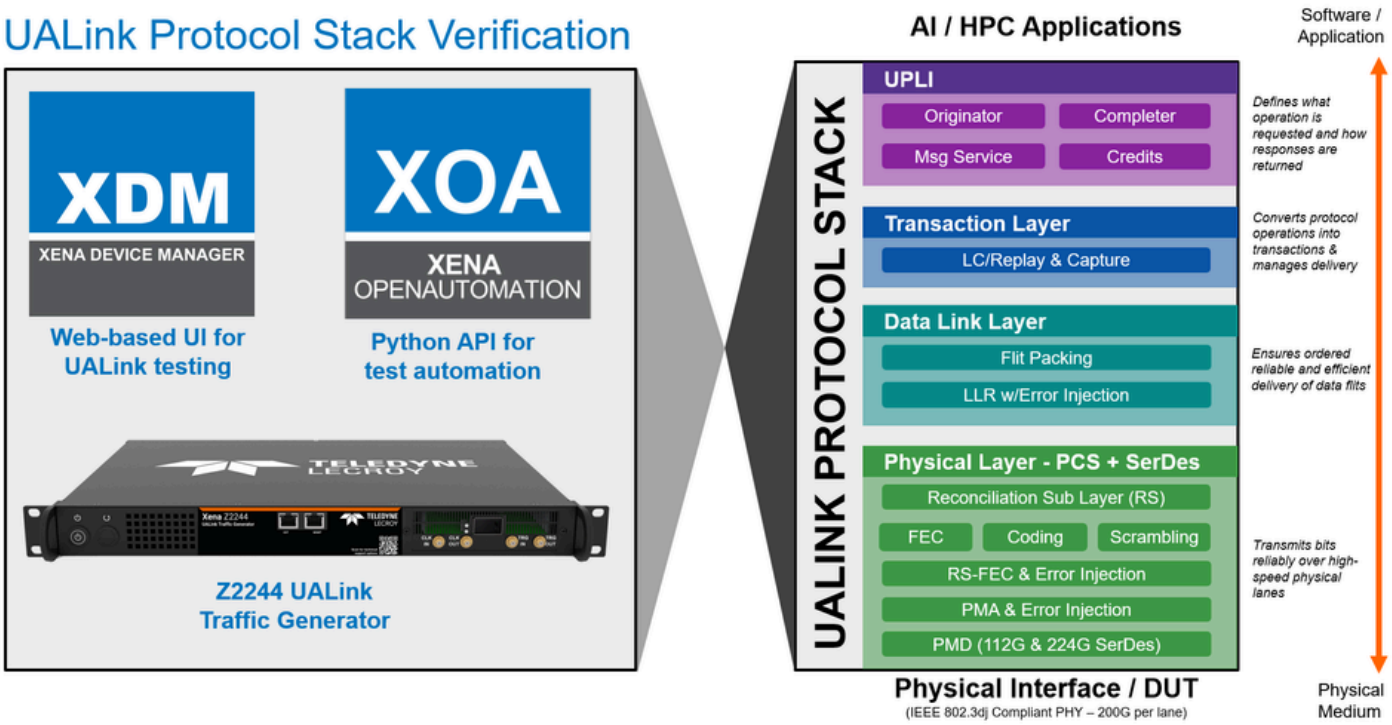
Multiple chassis can be daisy-chained together to create multi-port test configurations, enabling precise PPM control and accurate latency measurements across multiple chassis.

Advanced test software

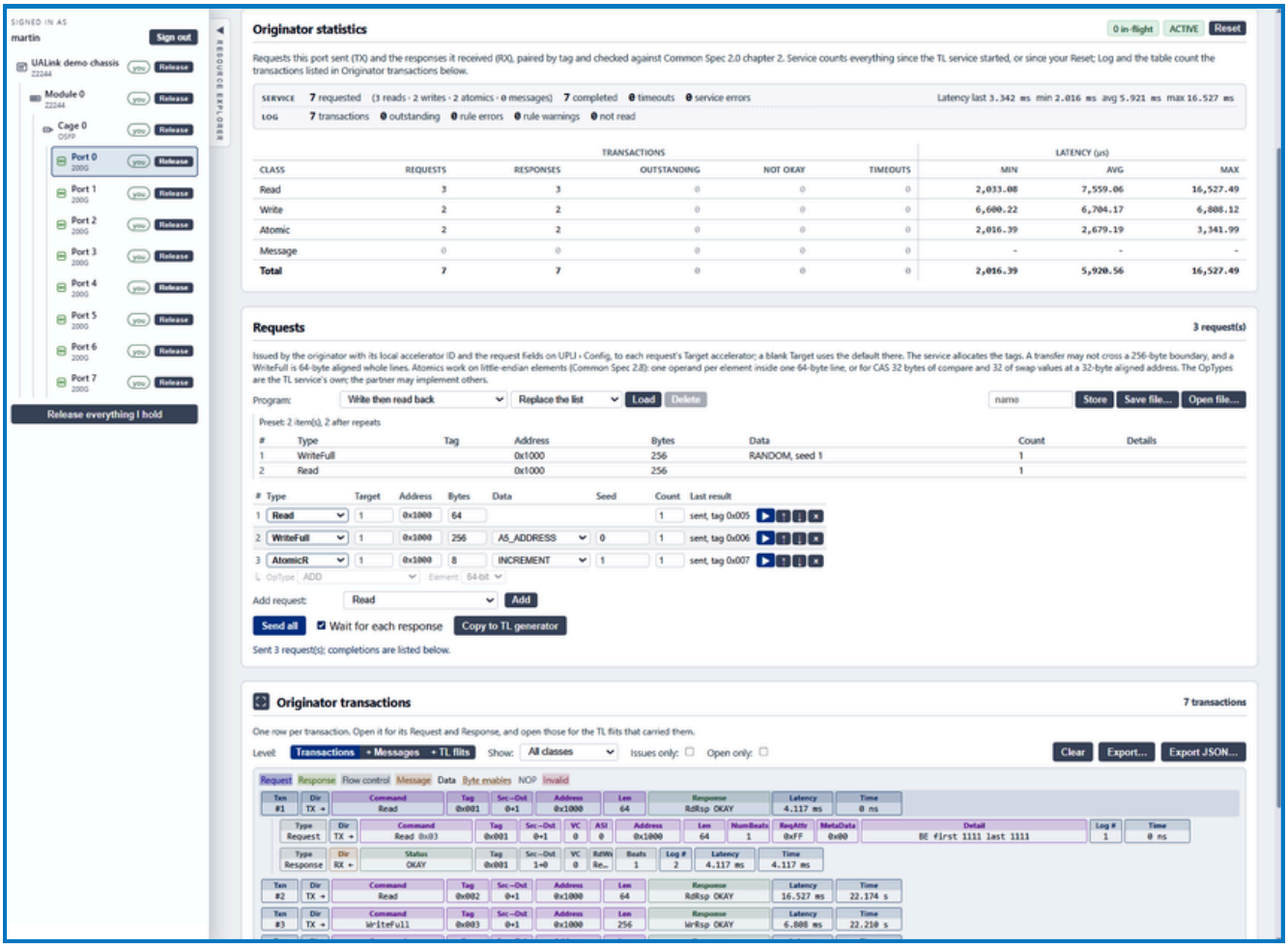
The Xena Z2244 is managed by Xena Device Manager (XDM) an intuitive, platform-independent web interface making it quick and easy to do performance, QA, functional and benchmark testing.

Xena OpenAutomation (XOA) - our open-source scripting and automation framework - is also included to help automate any available command to the system, with tailored tests, scripting and standardized test methodologies.

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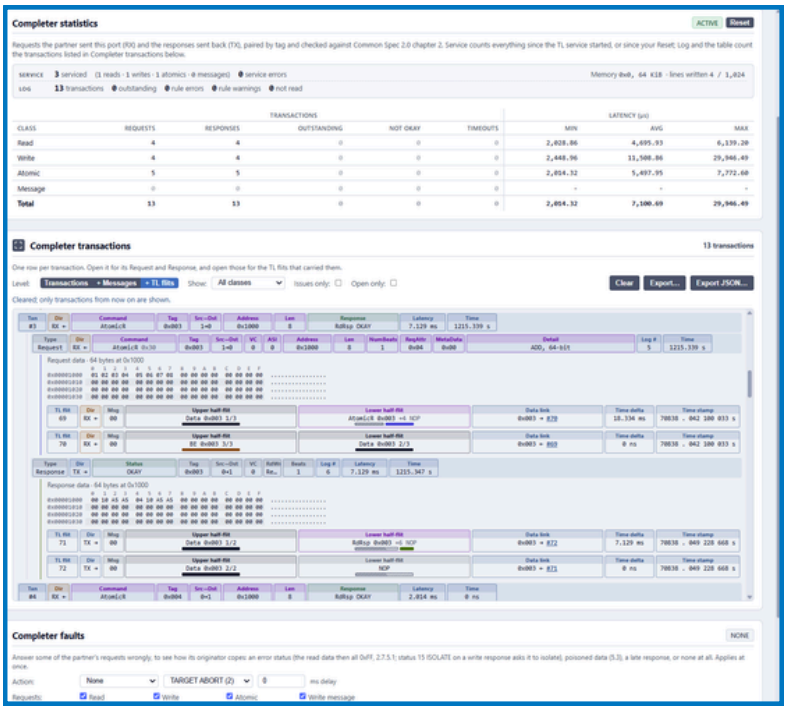


The Xena Z2244 can be controlled through an intuitive web-based UI or the XOA Python API and supports the full UALink protocol stack. Access to all protocol layers provides complete visibility into UALink traffic and enables the injection of impairments for comprehensive testing, validation, and troubleshooting.



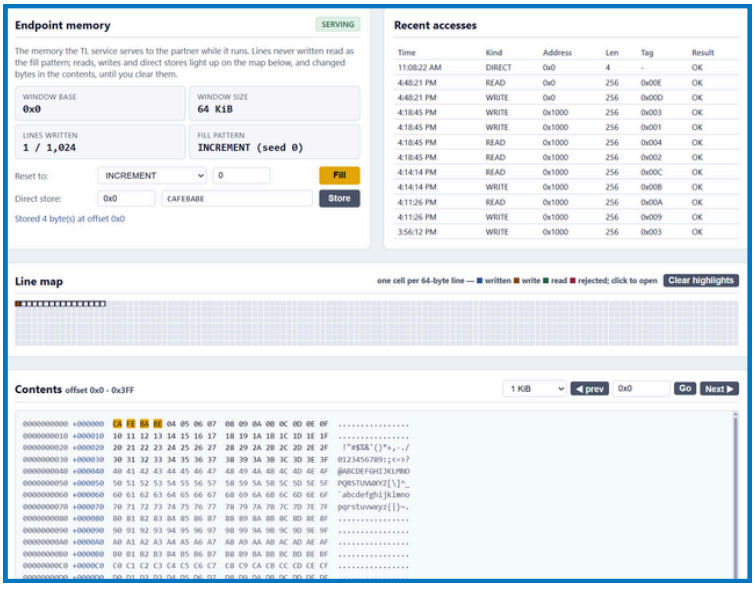
Powerful UALink UPLI Originator with support for programmable, stateful operations, comprehensive statistics, and a detailed overview of Originator transaction communication.
Resource Explorer provides an overview for easy management of hardware port resources.

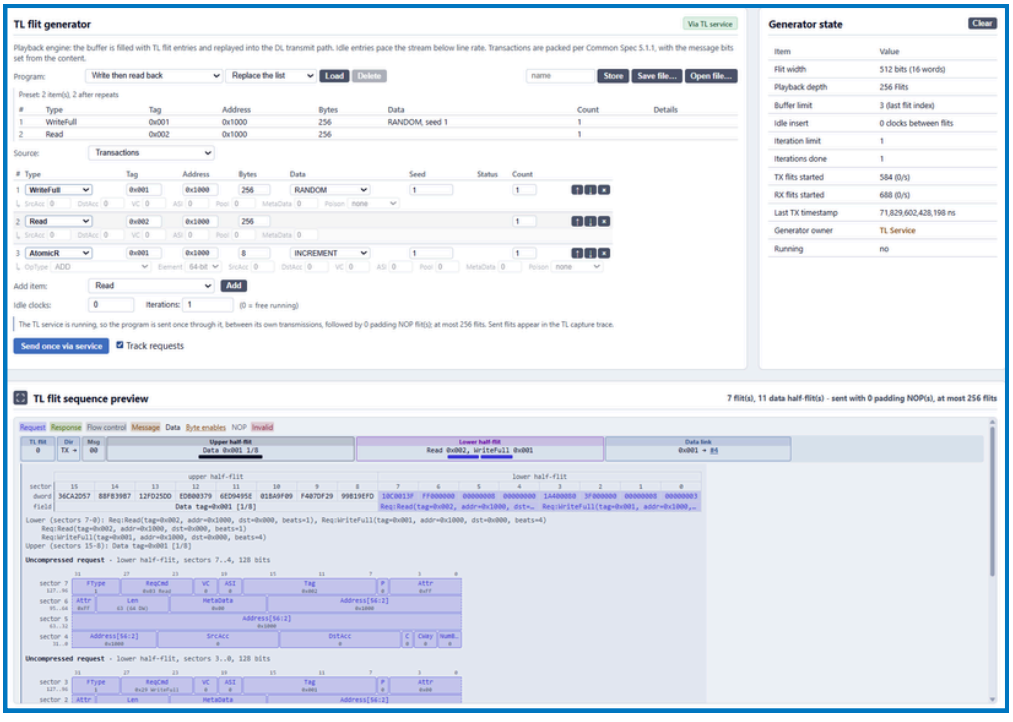
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Powerful UALink UPLI Completer provides comprehensive statistics and detailed transaction-level visibility for analyzing requests, responses, latency, and protocol behavior. Programmable fault injection enables controlled error scenarios to validate UALink endpoint behavior, error handling, and recovery mechanisms, helping engineers efficiently identify issues and troubleshoot UPLI communication.

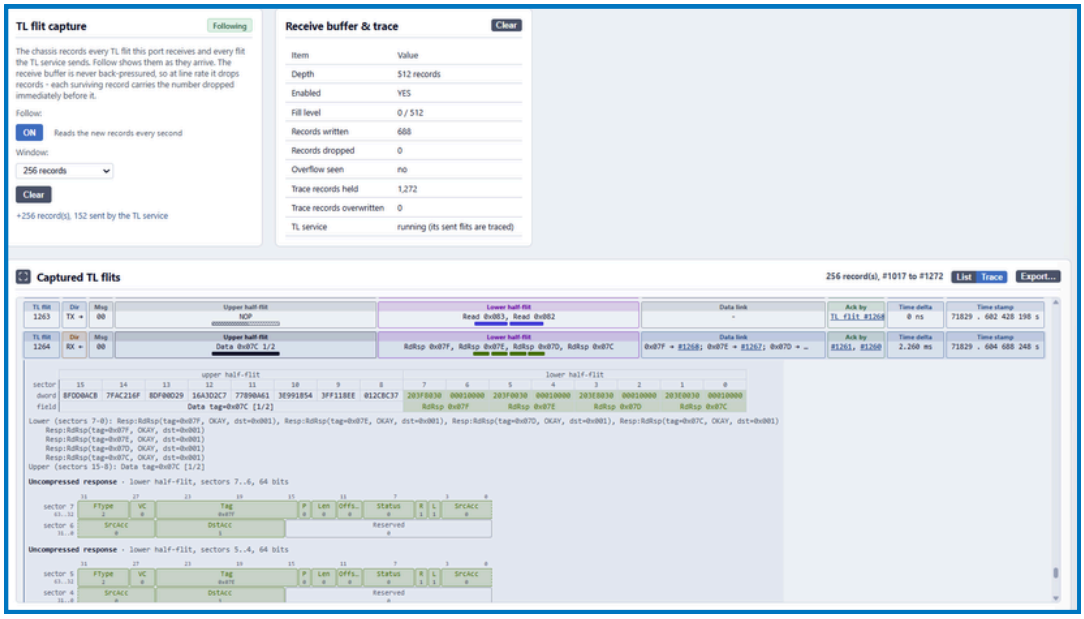
UALink Transaction Layer Service & Memory Access Dashboard provides comprehensive validation of UALink Transaction Layer operations, including credit initialization, memory read/write transactions, protocol handshaking, and latency analysis. The dashboard enables engineers to exercise memory access workflows, monitor credit exchanges, track transaction completion, and inspect live protocol traffic in real time, accelerating debug, interoperability testing, and performance characterization of UALink devices.





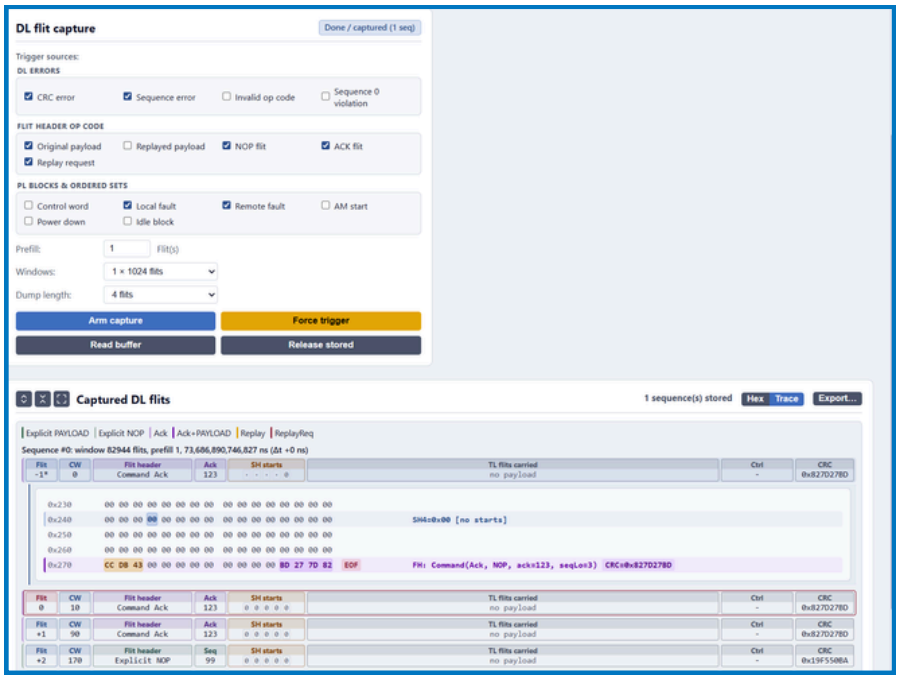
Powerful TL Flit Generator enables programmable generation and replay of UALink TL flit sequences for detailed protocol testing and validation. Users can configure transaction sequences, data patterns, timing, and iterations, while a detailed flit-level preview provides visibility into fields and encoded content before transmission. This enables controlled testing of UALink traffic and detailed analysis of protocol behavior.

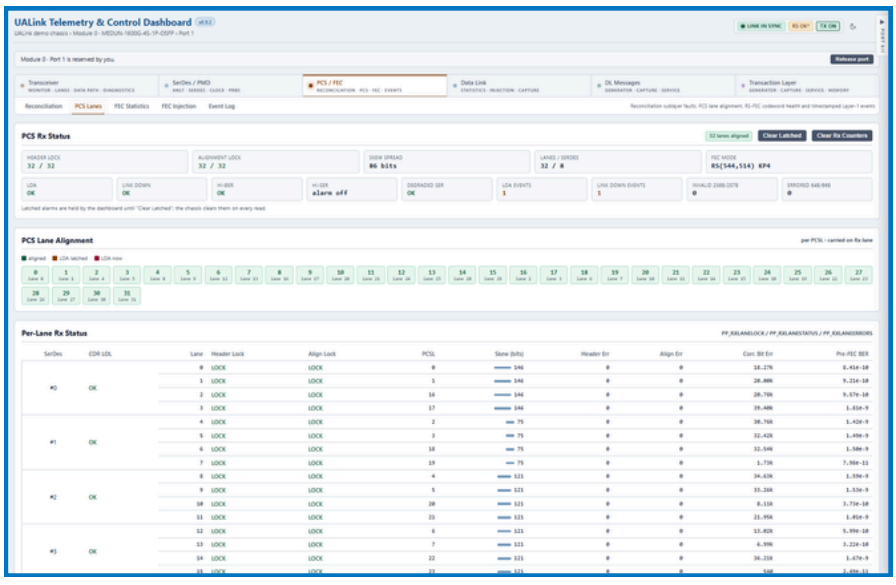
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UALink TL Flit Capture provides detailed visibility into transmitted and received TL traffic for protocol analysis and troubleshooting. Captured flits are displayed with direction, timing, acknowledgements, data-link relationships, and decoded upper and lower half-flit contents. Detailed field-level decoding enables engineers to inspect individual protocol fields and easily trace UALink transactions for validation and debugging.

UALink DL Flit Capture provides detailed capture and analysis of Data Link traffic with configurable triggering on DL errors, flit types, and Physical Layer events. Flexible pre-trigger and capture-window settings make it easy to isolate specific protocol events, while detailed decoding of flit headers, payloads, acknowledgements, sequence information, and CRC enables efficient analysis and troubleshooting of UALink link behavior.





UALink PCS Lane Alignment & FEC Monitoring Dashboard provides comprehensive visibility into PCS lane alignment, reconciliation status, and RS-FEC health across high-speed UALink interfaces. The dashboard enables real-time monitoring of header lock, alignment lock, lane mapping, skew distribution, bit error statistics, and pre-FEC BER, helping engineers rapidly validate link integrity, troubleshoot interoperability issues, and optimize UALink system performance.

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Interfaces and Standards	
Number of module cages/connectors	1 x OSFP-1600
Interface options	**224G SerDes** **Line Code** **IEEE** 2 x 800G PAM4 802.3dj 4 x 400G PAM4 802.3dj 8 x 200G PAM4 802.3dj **112G SerDes** **Line Code** **IEEE** 2 x 400G PAM4 802.3ck 4 x 200G PAM4 802.3dj / 802.3ck 8 x 100G PAM4 802.3ck Power capacity in cage: 42W
I2C & I3C RX/TX Transceiver Access Speed	Maximum of 12.5 MHz (actual speed depends on the transceiver module)
Clock Input/Output	2.048MHz, 10.000MHz, 156.25MHz & 625MHz clock input and output to external equipment via SMA connectors, useful for scope jitter measurements etc.
Trigger And Sync	In and out for triggers and for sync between two or more Z2244 Eduns (up to 6 units) via SMA connectors

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UPLI	
Originator	The TL service's Originator generates programmable UPLI requests to a partner's Completer and correlates received responses with the corresponding requests. Flexible traffic generation, comprehensive statistics, and detailed transaction analysis enable functional validation and troubleshooting of UALink endpoints. • Read, Write, WriteFull, Atomic and UPLI Write Message generation • Configurable addresses, transfer sizes, attributes, data patterns and repeat counts • Advanced Atomic operations with selectable element sizes • Programmable multi-request sequences and predefined test scenarios • Comprehensive transaction, error, timeout and latency statistics • Automatic request/response correlation • Drill-down from UPLI transactions to individual TL flits • Transaction filtering and export for further analysis

Completer	Emulates the UPLI Completer side of a UALink endpoint and services requests received from the partner's Originator.
	• Read, Write, Atomic, and UPLI Write Message servicing
	• Request/response correlation and detailed transaction analysis
	• Comprehensive transaction and latency statistics
	• Drill-down from UPLI transactions to individual TL flits
	• Error, timeout, and protocol-rule monitoring
	• Programmable fault injection:
	  ◦ Error status
	  ◦ Poisoned data
	  ◦ Response delay
	  ◦ Dropped response
	• Selective fault injection by request type, address range, and occurrence

Pattern test	Automates UPLI endpoint memory validation by writing configurable data patterns to the partner's memory, reading them back, and verifying the returned data byte by byte. • Write, read/verify, write/read, interleaved and randomized test sequences • Multiple predefined and configurable data patterns • Configurable memory region, transfer size, in-flight transactions and test passes • Automatic byte-by-byte data verification and mismatch detection • Detailed reporting of failed transactions, errors and timeouts • Test progress and result statistics
Endpoint Memory	Configurable emulated memory for the UPLI Completer with detailed visibility into memory contents and partner access activity. • Configurable memory window and predefined fill patterns • Direct memory and byte-level editing • Graphical visualization of Read, Write, and rejected accesses • Detailed hexadecimal and ASCII memory inspection • Recent-access history with address, transfer length, tag, and result • Easy identification of modified and accessed memory locations
UPLI Config	Centralized configuration and control of the UPLI Originator and Completer for endpoint emulation and protocol testing. • Configurable local and target Accelerator IDs • Configurable request timeout and UPLI request fields • Configurable Completer memory window and automatic Read/Write responses • Automatic Decode Error handling for out-of-range memory accesses • Configurable VC, ASI, Pool Credit, Metadata, and Write attributes • Isolation-mode testing with timeout and ISOLATE-response handling • Monitoring and controlled recovery from isolation conditions

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Transaction Layer	
TL Flit Generator	Programmable generation and replay of UALink TL traffic with control at both transaction and raw flit level. • Generate Requests, Responses, Atomics, Messages, Flow Control, NOPs, and Vendor-defined traffic • Transaction-based or raw flit generation • Predefined sequences for common UALink test scenarios • Configurable data patterns, transaction fields, and Atomic operations • Programmable timing and repeated playback • Detailed preview and field-level decoding of generated TL flits • Store and reuse custom traffic sequences
TL Flit Capture	Captures and analyzes UALink TL traffic, providing detailed visibility into both received traffic and flits transmitted by the TL service. • Continuous capture of TX and RX TL flits • Detailed decoding of Requests, Responses, Flow Control, Messages, Data and NOPs • Direction, Data Link sequence, acknowledgement and timing information • Follow mode for monitoring TL traffic as flits arrive • Receive-buffer and dropped-record monitoring • Detailed list and trace views with export capability
TL Link	Active Transaction Layer endpoint for protocol-conformance testing, interoperability validation, and debugging. • Active UALink 2.0 TL endpoint supporting stateless UPLI Originator and Completer operation • Configurable ReqCmd, RspCmd, ReqData, and RspData credit advertisement • Automatic partner credit discovery and monitoring • Configurable credit announcement for testing different partner implementations • TX/RX TL and credit-flit monitoring • Detailed TL service event and transaction logging • Exportable logs for protocol analysis and troubleshooting

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Data Link	
Data Link Capture trigger sources	Trigger-based capture and analysis of UALink Data Link traffic for protocol validation and troubleshooting. • Trigger on CRC, sequence, op-code, and other DL errors • Trigger on selected payload, replay, NOP, ACK, and replay-request flits • Trigger on Physical Layer events including local/remote faults and alignment markers • Configurable pre-trigger history and capture windows • Manual force-trigger for controlled test scenarios • Hexadecimal and detailed trace views • Export captured traffic for further analysis
DL Error Injection	Controlled injection of Data Link errors for validating UALink error detection, replay recovery, and protocol robustness. • TX payload and NOP CRC error injection • RX payload FCS error injection • Configurable CRC/FCS error bursts of 1 to 16 consecutive flits • Payload and NOP sequence-number corruption • Payload and NOP invalid-opcode injection • Configurable error count and spacing • Supports validation of Link-Level Replay (LLR) and protocol error handling
DL Statistics & Link State Control	Comprehensive Data Link statistics and state-machine control for UALink link validation, debugging, and recovery testing. • Live and cumulative TX/RX flit statistics • Payload, NOP, replay, ACK, and Replay Request counters • CRC, sequence, and invalid-flit error monitoring • Real-time FAULT, IDLE, NOP, and UP state visibility • Automatic or controlled link bring-up • Forced DL fault for recovery and replay testing • Configurable fault duration and ACK timeout

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Data Link Messages	
DL Message Generator	Programmable generation and playback of UALink Data Link messages for link bring-up, interoperability validation, and protocol testing. • Predefined Basic, Control, and UART DL messages • Device ID, Port Number, TL Rate, and TX Ready messaging • Channel Online/Offline and Link Width control messages • Custom 32-bit DL message generation • Configurable repetition and free-running playback • Up to 256 playback entries • Transmission statistics and generator-state monitoring
DL Message Capture	Captures UALink Data Link messages carried in alternative sectors for protocol validation, interoperability testing, and troubleshooting. • Dedicated capture of DL alternative-sector messages • 64-record receive buffer • Selectable record retrieval • Buffer fill, dropped-record, and overflow monitoring • Review of captured DL messages • Export captured messages for further analysis
DL Message Services	Automated Data Link discovery and handshake operation for interoperability validation, protocol testing, and debugging. • Auto-responder, protocol initiator, and bidirectional peer modes • Configurable Accelerator/Switch identity, Device ID, port number, and TL rate • Automated TX Ready, TL Rate, Device ID, Port Number, Channel Online, and Link Width discovery • Automatic acknowledgement of incoming protocol requests • Manual step-by-step handshake testing • Automatic discovery of link-partner attributes • Request, response, acknowledgement, timeout, and latency statistics • Detailed and exportable protocol event logging

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Physical / SerDes	

Pattern Generation	• PRBS-7Q, PRBS-9Q, PRBS-10Q, PRBS-11Q, PRBS-13Q, PRBS-15Q, PRBS-20Q, PRBS-23Q, PRBS-31Q, PRBS-49Q, PRBS-58Q, SSPRQ
	• Per-lane Statistics:
	  ◦ Lock status
	  ◦ PRBS errors
	  ◦ PRBS error rate
	  ◦ Error Injection
	  ◦ RX Lock
	  ◦ Received Bytes
	  ◦ Live BER

PRBS Error Injection	Inject single bit flips or continuous bit errors into active PRBS test streams. ◦ Single lanes or all
Transceiver	• Module Identity • Module Monitors & Flags • Per-Lane Optical Telemetry • CMIS CDB (Command Data Block) • CMIS Memory Map
SerDes Equalization & Coding Matrix	• 6-Tap Equalization FIR Filter: Fine-tune transmitter FIR filter coefficients per SerDes lane or all lanes using native taps. • Quick Preset: physical channel presets or IEEE 802.3ck standards presets • Custom Manual Taps configuration • Per Lane overview of tap settings

PMA Coding	• Control PAM4 precoding and Gray bit-to-symbol mapping per lane:.
	  ▪ Precoding Rx and Tx
	  ▪ Graycoding Rx and Tx

Auto Negotiation and Link Training	• ANLT Configuration
	  ◦ Auto-Neg + Link Training
	  ◦ Link Training Only
	  ◦ Disable ANLT
	• ANLT Status
	  ◦ ANLT Mode
	  ◦ Auto-Neg State
	  ◦ Negotiated FEC
	  ◦ Pause Ability
	• Per-Lane Link Training Status
	  ◦ LT Mode
	  ◦ Training Status
	  ◦ Failure Reason

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RS / FEC	

Reconciliation Sublayer (Local/Remote Fault feature)	• Configuration:
	  ◦ Normal: Acts according to 802.3 standard
	  ◦ Force Local: Port will continuously transmit “Local Fault indication”.
	  ◦ Force Remote: Port will continuously transmit “Remote Fault indication” .
	  ◦ Disabled: Port does not respond to Local/Remote Fault regardless of what it receives on RX.
	• Status:
	  ◦ Current and latched status of Local and Remote Faults
	  ◦ Counts of Local and Remote Faults

Physical Coding Sublayer	• PCS Rx Status
	  ◦ Header Lock, Alignment Lock, Skew Spread, Lanes / SerDes, FEC Mode, LOA, Link Down, HI-BER, HI-SER, Degraded SER, LOA Events, Link Down Events, Invalid 256b/257b, Errored 64b/66b
	• PCS Lane Alignment per PCSL
	  ◦ Alignment Status, LOA latched, LOA current
	• Per-Lane and SerDes Rx Status
	  ◦ CDR LOL, Header Lock, Align Lock, PCSL, Skew (bits), Header Err, Align Err, Bit Err, Pre-FEC BER

FEC Statistics	• FEC Summary ◦ RX Bits, RX Codewords, Corrected CW, Uncorrectable CW, Corrected Symbols, Pre-FEC BER, Post-FEC BER, FEC Mode • Codewords by Symbol Errors graph • Pre / Post-FEC BER graph • Corrected / Uncorrectable Codeword Rate graph
FEC Error Injection	• RS-FEC KP (544, 514, t=15), IEEE 802.3 Clause 91 • Configuration: Consecutive, Errored Codewords, Total Codewords Per Cycle, Errored Symbols Per Codeword • Bit error mask modes: Static, Rotate, Increment • Pre-defined profiles: Max. Consecutive Uncorrectable w/o Link Loss, Min. Consecutive Uncorrectable with Link Loss • Loop modes: Single, Continuous, Repeat • Injection statistics: Injected FEC Errors; Total Codewords, Total Uncorrectable Codewords, Total Correctable Codewords, Total Error-Free Codewords, Codeword Error Ratio, and Total Symbol Errors
Physical Medium Attachment Layer	• SM-PMA Symbol multiplexing (Clause 176) • BM-PMA Bit multiplexing (Clause 120)

Transmit Engines	
Transmit line clock adjustment	• From -100 to 100 ppm in steps of 1 ppm (shared across all ports)
Oscillator Characteristics	• Initial Accuracy is +/- 1 ppm • Frequency drift over 1st year: +/- 2 ppm in total (over 20 years: +/- 3 ppm in total) • Temperature Stability: +/- 0,5 ppm

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Specificiations	
Physical Format	• 1 rack unit (RU) high with 1 module slots • 1.7“ (H) x 17“ (W) x 16.3“(D) (4.5 x 43.2 x 40.6 cm) • 19" rack mount (EIA compatible) • Cooling with variable fan speed based on temperature of system and inserted medium • Front to rear airflow
Weight	• 19.8 lbs (9 kg)
Environmental	• Operating Temperature: 10 to 30ºC • Storage Temperature: -40 to 70ºC • Humidity: 8% to 90% non-condensing
Noise	• Variable: min. 49dB max. 81dB
Power	• AC Voltage: 100-240V • Frequency: 50-60Hz • Max. Power: 600W
Regulatory	• FCC (US) • CE (Europe)
User interface	• Chassis power on/off • Management RJ45 Ethernet (100/1000M BASE-T) • Management interface address: IPv4 and IPv6, static or DHCP • Xena UA Link UI, Xena OpenAutomation (XOA) and XOA CLI
Transceiver management interface	Z2244 UALink provides visibility and control over the complete management interface of the OSFP module inserted into the Z2244 via CMIS.
Connector Insertions	Z2244 UALink modules are provided with high-quality 224Gbps-capable electrical OSFP connectors for optimal signal integrity and performance. These OSFP connectors support a minimum of 1000 cycles (insertions) where optimal signal integrity is guaranteed.

Ordering Information

Product Description

- Xena Z2244 Edun 1U chassis with 800G 1 cage (OSFP-1600 IHS Cage) UALink Traffic Generator for testing 224G PAM4 speeds: 800G/400G/200G + 112G PAM4 speeds 400G/200G/100G

Product Code

C-EDUN-800G-3S-1P-UAL

Local sales offices are located throughout the world. Visit our website to find the most convenient location.

1-800-5-LeCroy • teledynelecroy.com

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