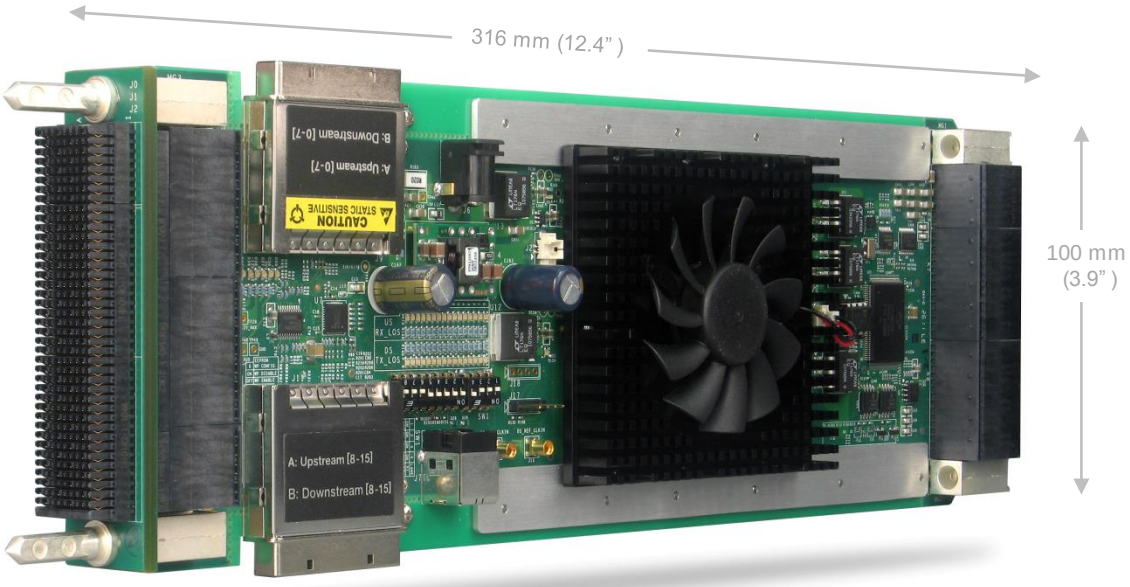
TELEDYNE LECROY
Everywhereyoulook™

VPX Interposer Card
for PCI Express® 2.0

VPX Interposer Card Enables Probing of PCI Express Traffic with Quick, Simple Setup!



Specifications	
Link Width	Supports a single PCIe link of x1, x2, x4, x8 or x16 Note: Interposer must be in configurations where the VPX card lane width matches the chassis backplane lane width
Data Rates	2.5 GT/s and 5 GT/s
Compatibility	VITA 46 compliant modules; supports 3U slots
Dimensions	100 x 316 x 19 mm (3.9" x 12.4" x 0.75")

Ordering Information

Product Description	Product Code
VPX Gen2 x16 Interposer Card	**PE070UIA-X**

The Teledyne LeCroy Specialty Interposer Card for VPX Applications supports VPX developers by providing a quick and easy way to connect a Teledyne LeCroy protocol analyzer to the PCI Express data channels in the VPX interface. The protocol analyzer can then capture, decode and display all PCI Express data traffic between the VPX expansion card and the VPX backplane.

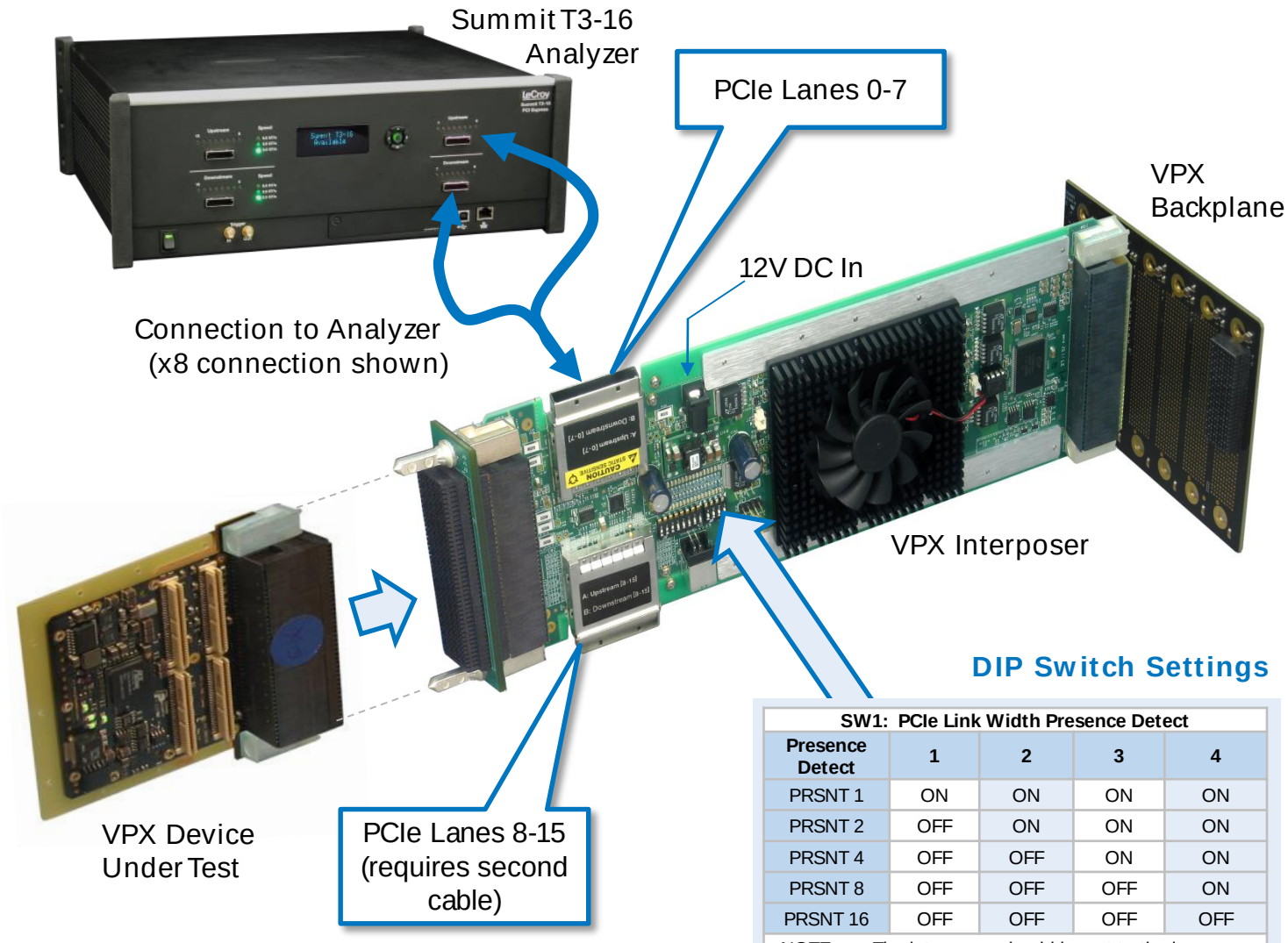
The VPX Interposer Card supports PCI Express data channels with lane widths up to x16, at PCIe® 2.0 data rates up to 5 GT/s. PCI Express protocol analyzers are tools for identifying, diagnosing and solving the interoperability issues typically encountered when system integrators verify VPX-based systems, including problems such as inconsistent board initialization, poor I/O performance, and power up issues. With the ability to directly view the PCI Express data traffic between host and device, VPX developers can more easily identify protocol errors and performance issues that otherwise slow down development and testing of new or updated products. The intuitive software views and built-in protocol translations aid engineers in rapid problem identification and solution, reducing time-to-market in development of new VPX (VITA 46) systems.

The interposer includes a heat sink with an integrated fan, providing compatibility with both air-cooled and conduction-cooled chassis (the heat sink may require an empty adjacent slot in the chassis).

PCI EXPRESS® PERFORMANCE SCALABILITY FOR THE NEXT DECADE

VPX

VPX Interposer Interconnection Overview



DIP Switch Settings

SW1: PCIe Link Width Presence Detect				
Presence Detect	**1**	**2**	**3**	**4**
PRSNT 1	ON	ON	ON	ON
PRSNT 2	OFF	ON	ON	ON
PRSNT 4	OFF	OFF	ON	ON
PRSNT 8	OFF	OFF	OFF	ON
PRSNT 16	OFF	OFF	OFF	OFF

NOTE: The interposer should be set to the lower lane width setting that matches between host and device.

Note on Clock Control through SW2

SW2 should remain set to ON during use. The OFF setting is reserved for factory test use only.

With #5 in the ON position, #1 through #4 control clock selection as shown in the table to the right. If all four switches are ON, then #6 and #7 provide additional options.

SW2: Clock DIP Switches *(Valid only if SW2 #5 is ON)*					
UPSTREAM	**DOWNSTREAM**	**1**	**2**	**3**	**4**
IN0	IN0	ON	ON	ON	ON
US_CLK	US_CLK	OFF	ON	OFF	ON
DS_CLK	DS_CLK	ON	OFF	ON	OFF
US_CLK	DS_CLK	OFF	ON	ON	OFF

SW2: Clock Control DIP Switch *(This switch should remain in the ON position. The OFF position is reserved for factory test use only.)*	
Clock Control	**5**
SW2	ON
[RESERVED]	OFF

SW2: Clock of IN0 and DUT *(Valid only if SW2 #1, 2 ,3, 4 and 5 are ON)*		
CLK IN0/ DUT	**6**	**7**
PO_RES_BUS	ON	ON
PO_REF_CLK	OFF	ON
LOCAL OSC (on PCB)	OFF	OFF

Instructions

To connect the VPX Interposer:

1. Install the VPX Interposer into the VPX Backplane.
2. Install the VPX Device Under Test (DUT) into the VPX Interposer.
3. Connect the Summit T3-16 Analyzer (or other analyzer) to the VPX Interposer. Connect the cable from the analyzer to the VPX Interposer connector marked **"PCIe Lanes 0-7"** in the diagram above. (See note #2 below.)
4. Plug in the AC adapter (supplied with the interposer) and connect the 12V DC plug to the interposer card.
5. Connect the analyzer to a host machine using the USB 2.0 port on the front panel of the Summit T3-16 Analyzer.
6. Install the software on the host machine.
7. Power on the analyzer.
8. Power on the VPX system.
9. Use the Teledyne LeCroy software application to monitor, record and view PCI Express traffic in the VPX system.

Notes:

1. The interposer requires device and VPX backplane (host) lane width to be the same.
2. If using x16 configurations, connect a second cable to the connector marked " **PCIe Lanes 8-15**."

VPX Interposer Test Points

Test Point	Signal	Description
TP18	TP_CLKOUT2P	Test point of PCIe reference clock (REFCLKP).
TP19	TP_CLKOUT2N	Test point of PCIe reference clock (REFCLKN).
TP25	+12V_B	+12V_B power supply from host to device (after current sensor).
TP26	+12V	+12V power supply from host to device. Used to measure current as follows: measure voltage between TP26 and TP25, Current = Voltage / 0.02.
TP27	+12V_AUX_B	+12V_AUX_B power supply from host to device (after current sensor).
TP28	+12V_AUX	+12V_AUX power supply from host to device. Used to measure current as follows: measure voltage between TP28 and TP27, Current = Voltage / 0.02.
TP29	-12V_AUX_B	-12V_AUX_B power supply from host to device (after current sensor).
TP30	-12V_AUX	-12V_AUX power supply from host to device. Used to measure current as follows: measure voltage between and TP29, Current = Voltage / 0.02.
TP31	+3.3V_B	+3.3V_B power supply from host to device (after current sensor).
TP32	+3.3V	+3.3V power supply from host to device. Used to measure current as follows: measure voltage between TP32 TP31, Current = Voltage / 0.02.
TP35	+3V3_RX	3.3V power for interposer. This is the output of regulator U11.
TP36	+3V3_TX	3.3V power for interposer. This is the output of regulator U12.
TP38	P12V	+12V external power supply for interposer.
TP39	+3V3	3.3V power for interposer. This is the output of regulator U15.
TP41	+2V5_TX	2.5V power for interposer. This is the output of regulator U13.
TP43	+2V5_RX	2.5V power for interposer. This is the output of regulator U14.
TP45	+3.3V_AUX_B	+3.3V_AUX_B power supply from host to device (after current sensor).
TP46	+3.3V_AUX	+3.3V power supply from host to device. Used to measure current as follows: measure voltage between TP46 TP45, Current = Voltage / 0.02.
TP47	+5V_B	+5V_B power supply from host to device (after current sensor).
TP48	+5V	+5V power supply from host to device. Used to measure current as follows: measure voltage between TP48 and TP47, Current = Voltage / 0.02.
TP50	INHIBIT#	This is an input signal to turn on/off the whole power of interposer. Ground this signal to turn off power.
	GND	TP33, TP34, TP37, TP40, TP42, TP44, TP49.

VPX Backplane Connector Reference Information

The VPX backplane connectors on the Teledyne LeCroy VPX interposer comply with the definitions provided in the American National Standard for VPX Baseline Standard (ANSI/VITA 46.0-2007) for 3U connectors using P0 (Table 4-3), P1 (Table 4-6) and P2 (Table 5-2). These pinout tables, along with the mapping of PCI Express lanes to VPX data channels, are provided for reference below. The device side connector accepts VPX modules with 3U connectors complying to the same specifications.

All VPX data channels are passed through the interposer, but only those channels (see table below) used for PCIe traffic are sampled. PCIe Lane mapping complies to VITA 46.4, Rev 0.15. All channels which are sampled are reserved for PCIe traffic only.

The alignment keying devices comply with section 4.4 of the specification. On the backplane side, universal sockets (Tyco 1-1469492-9) are used. On the device side, the keying pin is 0 degrees (Tyco 1410956-1). These alignment keying devices may be changed if desired to provide customized keying systems.

Table 4-3 P0 Utility Connector

	Wafer Type	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	Power	Vs1	Vs1	Vs1	No Pad	Vs2	Vs2	Vs2
2	Power	Vs1	Vs1	Vs1	No Pad	Vs2	Vs2	Vs2
3	Power	Vs3	Vs3	Vs3	No Pad	Vs3	Vs3	Vs3
4	Single-ended	SM2	SM3	GND	-12V_AUX	GND	SYSRESET*	NVMRO
5	Single-ended	GAP*	GA4*	GND	3.3V_AUC	GND	SM0	SM1
6	Single-ended	GA3*	GA2*	GND	+12V_AUX	GND	GA1*	GA0*
7	Differential	TCK	GND	TDO	TDI	GND	TMS	TRST*
8	Differential	GND	REF_CLK-	REF_CLK+	GND	RES_BUS-	RES_BUS+	GND

Table 4-6 Common P1 Pinout

	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	P1-RES_BUS_SE	GND	L0-TX-	L0-TX+	GND	L0-RX-	L0-RX+
2	GND	L1-TX-	L1-TX+	GND	L1-RX-	L1-RX+	GND
3	P1-VBAT	GND	L2-TX-	L2-TX+	GND	L2-RX-	L2-RX+
4	GND	L3-TX-	L3-TX+	GND	L3-RX-	L3-RX+	GND
5	SYSCON*	GND	L4-TX-	L4TX+	GND	L4-RX-	L4-RX+
6	GND	L5-TX-	L5-TX+	GND	L5-RX-	L5-RX+	GND
7	P1-REFCLK0_SE	GND	L6-TX-	L6-TX+	GND	L6-RX-	L6-RX+
8	GND	L7-TX-	L7-TX+	GND	L7-RX-	L7-RX+	GND
9	P1-REFCLK1_SE	GND	L8-TX-	L8-TX+	GND	L8-RX-	L8-RX+
10	GND	L9-TX-	L9-TX+	GND	L9-RX-	L9-RX+	GND
11	P1-REFCLK2_SE	GND	L10-TX-	L10-TX+	GND	L10-RX-	L10-RX+
12	GND	L11-TX-	L11-TX+	GND	L11-RX-	L11-RX+	GND
13	P1-REFCLK3_SE	GND	L12-TX-	L12-TX+	GND	L12-RX-	L12-RX+
14	GND	L13-TX-	L13-TX+	GND	L13-RX-	L13-RX+	GND
15	P1-SE7	GND	L14-TX-	L14-TX+	GND	L14-RX-	L14-RX+
16	GND	L15-TX-	L15-TX+	GND	L15-RX-	L15-RX+	GND

P1: PCIe Lane Mapping

Lane	Transmit	Receive
0	P1.E1/P1.D1	P1.B1/P1.A1
1	P1.F2/P1.E2	P1.C2/P1.B2
2	P1.E3/P1.D3	P1.B2/P1.A1
3	P1.F4/P1.E4	P1.C4/P1.B4
4	P1.E5/P1.D5	P1.B5/P1.A5
5	P1.F6/P1.E6	P1.C6/P1.B6
6	P1.E7/P1.D7	P1.B7/P1.A7
7	P1.F8/P1.E8	P1.C8/P1.B8
8	P1.E9/P1.D9	P1.B8/P1.A8
9	P1.F10/P1.E10	P1.C10/P1.B10
10	P1.E11/P1.D11	P1.B11/P1.A11
11	P1.F12/P1.E12	P1.C12/P1.B12
12	P1.E13/P1.D13	P1.B13/P1.A13
13	P1.F14/P1.E14	P1.C14/P1.B14
14	P1.E15/P1.D15	P1.B15/P1.A15
15	P1.F16/P1.E16	P1.C16/P1.B16

Note 1: All sampled channels listed above are dedicated to a single PCIe link of up to x16 lanes, and any unused channels may not be used for other traffic.

Note 2: All Ln-TX+ and Ln-TX- pins (Transmitter differential differential pair of the connector) shall be connected to the Receiver differential pair on the payload board.
Ln-RX+ and Ln-RX- pins (Receiver differential pair of of the connector) shall be connected to the Transmitter differential pair on the payload board.

Table 5-2 Module P2 Differential Pinout

	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	P2-SE0	GND	P2-DP1-	P2-DP1+	GND	P2-DP0-	P2-DP0+
2	GND	P2-DP3-	P2-DP3+	GND	P2-DP2-	P2-DP2+	GND
3	P2-SE1	GND	P2-DP5-	P2-DP5+	GND	P2-DP4-	P2-DP4+
4	GND	P2-DP7-	P2-DP7+	GND	P2-DP6-	P2-DP6+	GND
5	P2-SE2	GND	P2-DP9-	P2-DP9+	GND	P2-DP8-	P2-DP8+
6	GND	P2-DP11-	P2-DP11+	GND	P2-DP10-	P2-DP10+	GND
7	P2-SE3	GND	P2-DP13-	P2-DP13+	GND	P2-DP12-	P2-DP12+
8	GND	P2-DP15-	P2-DP15+	GND	P2-DP14-	P2-DP14+	GND
9	P2-SE4	GND	P2-DP17-	P2-DP17+	GND	P2-DP16-	P2-DP16+
10	GND	P2-DP19-	P2-DP19+	GND	P2-DP18-	P2-DP18+	GND
11	P2-SE5	GND	P2-DP21-	P2-DP21+	GND	P2-DP20-	P2-DP20+
12	GND	P2-DP23-	P2-DP23+	GND	P2-DP22-	P2-DP22+	GND
13	P2-SE6	GND	P2-DP25-	P2-DP25+	GND	P2-DP24-	P2-DP24+
14	GND	P2-DP27-	P2-DP27+	GND	P2-DP26-	P2-DP26+	GND
15	P2-SE7	GND	P2-DP29-	P2-DP29+	GND	P2-DP28-	P2-DP28+
16	GND	P2-DP31-	P2-DP31+	GND	P2-DP30-	P2-DP30+	GND

Note 3: All P2-DP signals are pass-through between P2 on Host and P2 on the Device side. The GND pins defined in the table are connected to GND on the interposer.

System Compatibility	
Summit T3-16	✓
Summit T3-8	✓
Summit T34	✓
Summit T28	✓
Summit T24	✓

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