TELEDYNE | LECROY

# DDR4 System Level Compliance & Debug

## QPHY2-DDR4



## Key Features

- **Test DDR4 up to 3200 MT/s**
- **Validate the JESD79-4D spec**
- **QualiPHY 2 automated compliance**
  - Test at the BGA of the DRAM
  - Measure DQ, DQS, CK and CA signals
  - Increase testing repeatability
  - Save Pass/Fail reports with screenshots and annotations
  - Debug failures during testing
- **External MSO for DDR4**
  - Highest Read/Write separation accuracy
  - Industry's only trigger & decode
  - Validate 20+ CMD bus packets
  - Trigger on six packet types
- **Multi-scenario Views**
  - Accelerate pre-compliance
  - Compare crosstalk, de-embedding, multiple lanes, eye diagrams across each View
  - Measurements and masks defined by JEDEC
- **Improve signal quality and reduce reflections with VirtualProbe**

**Supporting data speeds up to 3200 MT/s, the JEDEC JESD79-4D standard for DDR4 memory brings improved performance and greater energy efficiency than previous generations. Designing, integrating, and building systems with DDR4 memory requires tools to quickly analyze and debug every stage of design, from turn-on, validation and optimizing to final compliance testing.**

### Maximize Turn-on and Initial Validation Testing

Establish basic operation, signal quality checks and packet responses quickly.

- Validate Read and Write packets
- Confirm command bus functionality
- Adjust for mid-bus reflections

### Accelerate Pre-compliance Testing and Fine Tuning

Stability occurs when the DRAM has been tuned and optimized. Test multiple scenarios with dedicated viewing areas.

- The multiple view function is included in DDR Debug Toolkit
- JEDEC defined measurements
- Eye diagram and mask testing

### Automated DDR4 Compliance Testing

QualiPHY 2 automated software enables fast test times by reducing inconsistencies while testing JEDEC measurement requirements. Additionally, pause tests and root-cause failures in the DDR Debug Toolkit.

# FASTEST DDR TEST JOURNEY

**The DDR test journey can be quick when the right tools for engineers enable smooth transitions from all stages of design, DDR turn-on, initial validation testing to fine-tuning, optimizing, pre-compliance and final compliance. Accelerate testing by confidently testing designs quickly and easily. Teledyne LeCroy covers BGA testing tools for JEDEC standards such as DDR2/3/3L/4/5 and LPDDR2/3/4/4X/5/5X.**




## 1. Interposers and Probes

- High bandwidth probes with solder-in tips
- Interposers from reliable partners

## 2. External MSO – HDA125 High Speed Digital Analyzer

- Highest accuracy for Read/Write separation
- Market's only trigger & decode up to DDR5
- Validate 20+ Command Address packets

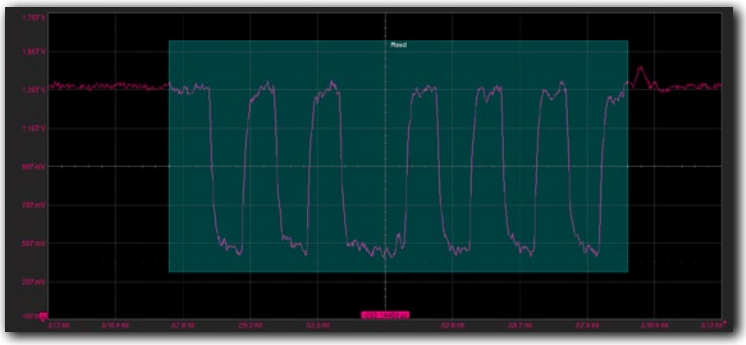
## 3. Tools for Turn-on Through Pre-compliance

- Multi-scenario viewing fast-tracks testing
- Exclusive toolkit with JEDEC defined measurements
- Eliminate signal quality errors with virtual probing

## 4. Automated DDR4 Compliance Testing

- Measure the latest JEDEC specification at the BGA
- Increase repeatability & test consistency
- Save Pass/Fail reports with annotated screenshots

# DDR4 TESTING WITH QUALIPHY 2 & DDR DEBUG TOOLKIT

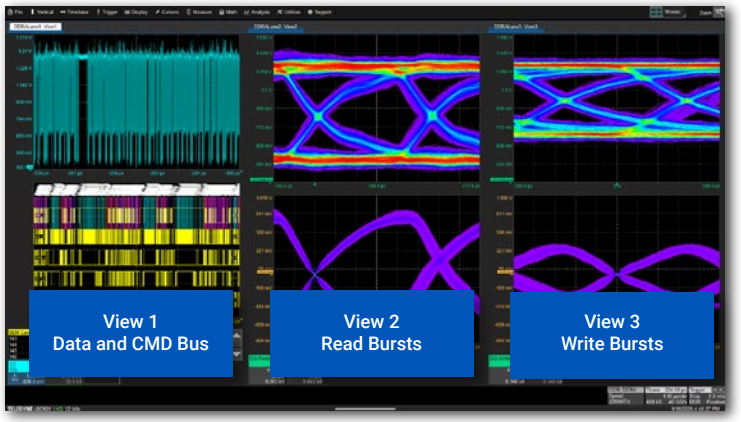


| DDR Cmd Bus | Time | Clocks | State | Abbreviation | Details (Cmd states) |
|---|---|---|---|---|---|
| 140 | -203.153 µs | 28 | Read | RD | PRE RD RD RD PRE RD RD PRE RD RD |
| 141 | -203.130 µs | 12 | Write | WR | ACT ACT WR WR ACT WR |
| 142 | -203.122 µs | 28 | Write | WR | WR ACT WR PRE WR WR WR WR WR |
| 143 | -203.054 µs | 4 | Write | WR | PRE PRE PRE PRE PRE ACT ACT ACT ACT WR |

## Decode and Analyze DDR4 Signals with Ease

Establishing basic operation, signal checks and responses is the foundation of board turn-ons. Decode the command bus to understand if it's correctly communicating and know if Read and Write packets are present.

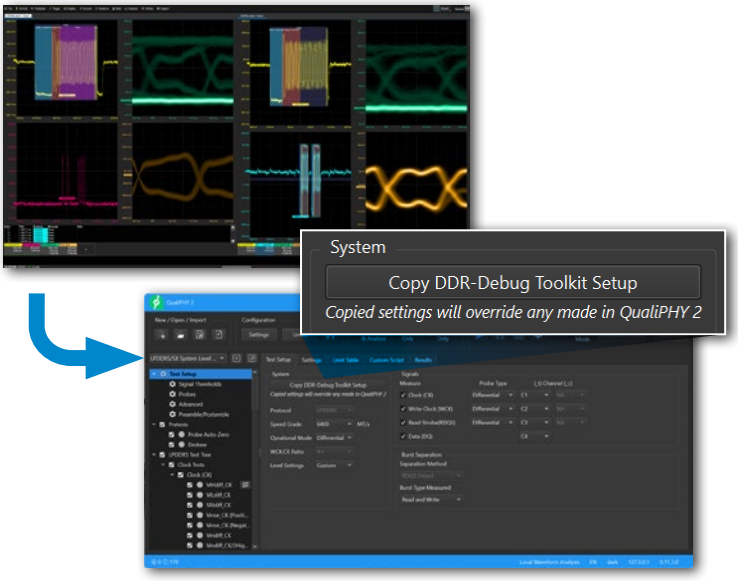
- High-speed external MSO (HDA125) enables the highest accuracy for Read & Write packet separation.
- Overlay Read/Write visuals on channels
- Decode 20+ packets from JEDEC Command Truth Table




## Multiple Scenario Viewing Areas

DDR stability occurs when the DRAM has been fine-tuned and optimized. This occurs when the voltage and timing parameters have been adjusted and measured for peak performance.

- Speed up tuning stages with side-by-side signal comparisons
- Interactively analyze signals using eye diagrams, mask tests, and JEDEC-specific measurements
- Perform measurements per view to validate signal integrity across different perspectives




## Automated DDR4 Compliance Testing

Automated DDR compliance testing enables faster test times by reducing inconsistencies, testing to the JEDEC standard and quick stopping for root-causing failures through the DDR Debug Toolkit.

- DDR4 JEDEC measurements for DQ, DQS, CK, CA signals
- Supports System Level testing at the BGA
- Save Pass/Fail reports with annotated screenshots.
- Set up in DDR Debug Toolkit and once-click transfer to the QualiPHY 2 interface
- Analyze compliance failures in a dedicated Debug Toolkit

# SPECIFICATIONS AND ORDERING INFORMATION

## Specifications

### QPHY2-DDR4 Compliance Measurements

| | |
|---|---|
| Clock (CK) | tCK (avg), tCK (abs), tCH (avg), tCH (abs), tCL (avg), tCL (abs), tJIT (duty), tJIT (cc), tJIT (per), tERR (nper), SRIdiff_CK, VIHdiff_CK, VILdiff_CK |
| Eye Diagram Tests | Write Burst DQ/DQS Mask, VIHL_AC, tDQS2DQ, Read Burst DQ/DQS Eye |
| Electrical Tests | SRIN_clVW, CA AC Over/Undershoot Peak and Area |
| Write Bursts (Inputs) | VIHdiff_DQS, VILdiff_DQS, SRIdiff, tDVAC, srr1, srf1, srr2, srf2, DQ/DQS AC Over/Undershoot Peak and Area |
| Read Bursts (Outputs) | SRQse, SRQdiff |
| Timing Tests | |
| Write Bursts (Inputs) | tDQSS, tDQSH, tDQSL, tDSS, tDSH, TdIPW, tWPRE, tWPST |
| Read Bursts (Outputs) | tDQSQ, tQSH, tQSL, tQH, tDQSCK, tHZ_DQ, tLZ_DQ, tHZ_DQS, tLZ_DQS, tRPRE, tRPST |

### QPHY2-DDR4 Configuration Selections

| | |
|---|---|
| Compliance Speeds (MT/s) | 1600, 1866, 2133, 2400, 2666, 2933, 3200 |
| Probe Connection | CK: Differential or Single-Ended (True CK_t & Compliment CK_c)<br>DQS: Differential or Single-Ended (True DQS_t & Compliment DQS_c)<br>DQ: Single-Ended<br>CA: Single-Ended |
| Clock Pattern Supported | Continuous |
| Report Formats | XML, HTML, PDF |

### DDR4 Debug Toolkit Measurements & Configurations

| | |
|---|---|
| Supported Protocols | DDR4 |
| Supported Speeds | 1600, 1866, 2133, 2400, 2666, 2933, 3200 |
| Measurement Types | Burst Count, Transition Count, VH(AC/DC), VL(AC/DC, tDH, tDS, tIH, tIS, tDQSCK, tDQSQ, SlewRise, SlewFall, Vref |
| Views (Configurations) | View1, View2, View3, View4, Ref |
| Eye Diagram Analysis | Eye One: DQ-Read, DQ-Write, DQS-Read, DQS-Write, ADDR, BUS<br>Eye Two (Matches R/W packet type): DQ, DQS, Clock |
| Mask Speeds Supported | 1600, 1866, 2133, 2400, 2666, 2933, 3200 |
| Mask Packet Type & Signal | Write DQ/DQS Packets |
| Command Bus Decode Types* (JEDEC Command Truth Table) | Bank Activate, Write, Read, Mode Register Write, Mode Register Read, Refresh, Self Refresh Entry, Self Refresh Exit, Precharge, Deselect, ZQ Calibration, Power Down Entry, Power Down Exit, RFU |
| Command Bus Trigger Types* | Write Packet, Read Packet, Write or Read, Bank Activate, Precharge, Refresh, MRS |

**Requires HDA125 Logic Analyzer (additional external MSO)*

### Read/Write Packet Separation (QPHY2-DDR4)

| | |
|---|---|
| Packet Separation Technique | Phase, CMD BUS (HDA125 Logic Analyzer) |
| Packet Burst to Analyze | Read, Write, Read & Write |
| HDA125 Channel Setup | CS, CA0, CA1, CA2, CA3, CA4 |

## Ordering Information

| Product Description | Product Code |
|---|---|
| **Recommended Hardware** | **Equipment** |
| DDR4 up to 3200 MT/s | |
| WaveMaster 8130HD 13 GHz 80 GS/s 12-bit High Definition Oscilloscope | WaveMaster 8130HD |
| Qty. 3 – DH Series Differential 13 GHz High Bandwidth Probes (CK, DQ, DQS) | DH13-PL |
| External MSO - HDA125 High-speed Digital Analyzer for decoding/triggering the Command Address Bus (CS, CA0, CA1, CA2, CA3, CA4) | HDA125 |
| HDA125 Digital Leadset with QuickLink Solder-In Tips (includes nine solder tips) | HDA-DLS-09QL |
| **Recommended Software (Turn-On through Compliance Testing)** | **Options** |
| QualiPHY 2 DDR4 System Level Automated Compliance Software | QPHY2-DDR4 |
| DDR4 Debug Toolkit (decode/trigger, multiple views, eye diagram, mask test, DDR measurements) | WM8KHD-DDR4-TOOLKIT |
| VirtualProbe Software (de-embed interposers, fix reflections and termination issues) | WM8KHD-VIRTUALPROBE |

### Customer Service

Teledyne LeCroy oscilloscopes and probes are designed, built and tested to ensure high reliability. In the unlikely event you experience difficulties, our digital oscilloscopes are fully warranted for three years and our probes are warranted for one year. This warranty includes:

- No charge for return shipping
- Long-term 7-year support
- Upgrade to latest software at no charge

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