Comprehensive DDR Memory Test Suite

Key Features

Test support for the entire DDR design cycle
Support for DDR2/3/4 and LPDDR2/3/4

Physical Layer Debug Toolkit
- Test, debug, and analysis tools for the entire DDR design cycle
- Eye Diagrams with mask testing
- Flexible DDR Measurements

Physical Layer Compliance
- JEDEC clock, electrical and timing compliance tests
- Automatic reporting
- Stop-on-test debug feature

High-speed Digital Analyzer
- Acquire and analyze DDR command bus signals
- 12.5 GS/s digital acquisition
- Unique QuickLink probing architecture

Protocol Compliance and Debug
- Quick and easy setup
- Triggering for 50+ JEDEC Timing Violations
- JEDEC protocol compliance

Teledyne LeCroy offers a full line of DDR test solutions for system bring-up, debug, performance analysis, and compliance. The DDR Debug Toolkit is a unique and flexible tool for analyzing all aspects of the physical layer design. The HDA125 enables advanced command triggering and sophisticated, searchable bus state viewing. JEDEC compliance testing is supported on the physical layer with the QualiPHY compliance package and on the protocol layer with the Kibra compliance analyzer.

Physical Layer DDR Toolkit
The DDR Debug Toolkit provides test, debug, and analysis tools for the entire DDR design cycle. Unique DDR analysis capabilities provide automatic Read and Write burst separation, bursted data jitter analysis, and DDR-specific measurement parameters. All this DDR analysis can be performed simultaneously over four different measurement views.

Physical Layer Compliance
The QualiPHY DDR packages perform all of the clock, electrical and timing tests per the JEDEC standards. Upon completion of each test run a report is generated which contains pass/fail results as well as fully annotated screenshots of the worst case measurement.

High-speed Digital Analyzer
The HDA125 turns your Teledyne LeCroy oscilloscope into the highest-performance, most flexible mixed-signal solution for DDR debug and evaluation. With 12.5 GS/s digital sampling rate on 18 input channels and the revolutionary QuickLink probing solution, validation of DDR interfaces has never been simpler or more comprehensive.

Protocol Compliance and Debug
A combination of quick and easy hardware setup and immediate feedback on violations allows users to quickly validate JEDEC timing compliance or swiftly identify problem areas with their memory system. Capturing the Command Address and Control bus, the Kibra 480 can quickly identify timing issues associated with the JEDEC defined speed bins.
Successful development of new DDR products requires a coordinated test program to cover all aspects of the DDR design cycle. During system bring-up it is essential to perform functional testing which involves monitoring traffic on the protocol level and verifying eye diagrams and setup and hold time measurements on the physical layer. As the design matures, signal integrity analysis becomes crucial to perform optimization and system tuning to maximize system margin. Finally, no design is complete without testing compliance to JEDEC requirements on both the physical and protocol layers. It is critical to have a powerful arsenal of tools for debugging at every step along the way.

The Right Solution for Every Stage of Development
Teledyne LeCroy offers a complete line of DDR test solutions covering both the physical and protocol layers at every stage of the DDR design cycle. Having the right tools for each step in the design cycle will reduce time-to-insight and provide comprehensive verification, debug, and compliance.

QualiPHY’s automated compliance framework provides automated physical layer testing for DDR2/3/4 and LPDDR2/3/4, while the DDR Debug Toolkit offers unmatched flexibility for debug and pre-compliance testing. The Kibra line of protocol analyzers is the first standalone protocol analyzer for DDR supporting both DDR3 and DDR4. It offers compliance analysis as well as full protocol and performance analysis.

Innovative DDR Test Tools
Unique and innovate test tools allow for debugging and validation to be completed in an intuitive manner, greatly expediting the DDR design process.

Experience and leadership in providing high-speed serial data test tools make Teledyne LeCroy the natural choice as a test partner for DDR development.
Challenges with Adopting Next Generation DDR

DDR standards are developed by the Joint Electron Device Engineering Council (JEDEC) but the responsibility for adhering to these standards is left up to the designer. Not all DDR implementations will require testing to the JEDEC standard but almost all will require some level of testing to ensure reliable data transfer.

The adoption of each new generation of DDR seemingly offers double the maximum data transfer rate with a lower power consumption, leaving less design margin and presenting increasingly difficult design and test challenges. Having the right set of tools can make it easier to overcome these design challenges.

Given the bidirectional nature of the DDR interface, it is critical to reliably separate Read and Write bursts. Manually identifying bursts can be both time consuming and error prone. The DDR Debug Toolkit allows the user to separate Read and Write bursts with a push of a button based on DQS-DQ phase. When used in conjunction with the High-speed Digital Analyzer the command bus can be used for situations with non-ideal signal integrity (e.g. reflections).

Testing of the JEDEC specification can require upwards of 50+ measurements to be made, making it very difficult to manually perform these measurements. Using an automated compliance package allows even the most novice engineering to make consistent measurements with ease.

Along with doubled speed and lower power additional features have been added that can be dynamically enabled or disabled. Being able to capture and follow these dynamic commands real time allows debug of the memory system based on memory behavior at the exact moment in time.

Testing a DDR interface requires proper probing techniques to ensure accurate and repeatable results. The DDR specifications require the signals to be tested at the balls of the DRAM chip; however, these signals are not always accessible. Virtual Probing techniques can be used to improve the DDR probing experience to maximize signal integrity when it is not possible to probe in the desired locations.
**Key Features**

Automated Read/Write burst separation

Simultaneous analysis of four different measurement views

View up to 10 eye diagrams with mask testing and eye measurements

Searchable Bus State views with intuitive color-coded overlay

Command bus based triggering

Perform jitter analysis for root cause analysis

Quickly configure DDR-specific measurements

Analyze specific regions of bursts with configurable qualifiers

Support for DDR2/3/4 and LPDDR2/3/4

Select standard and custom speed grades

Most oscilloscope-based DDR physical layer test tools are targeted exclusively at JEDEC compliance testing, whereas the DDR Debug Toolkit provides test, debug, and analysis tools for the entire DDR design cycle. The unique DDR analysis capabilities provide automatic Read and Write burst separation, bursted data jitter analysis, and DDR-specific measurement parameters. All this DDR analysis can be performed simultaneously over four different measurement views.

**Effortless Burst Separation**

Automatic separation of Read and Write bursts, eliminates the time-consuming process of manual burst identification and simplifies the analysis of DDR systems. Bursts can be separated based on DQ-DQS phase or based on the command bus when used in conjunction with the HDA125. The HDA125 additionally enables a unique “bus view”, tabulating the Command Bus activity and placing color-coded overlays and annotations on top of the physical layer waveform in an intuitive manner. The built in search feature allows for quick navigation of the various command bus states.

**Eye Diagram Analysis**

Any DQ, DQS or command/address signal can be tested against a standard or a custom defined mask, with up to 10 eye diagrams viewed simultaneously. Enabling mask failure indicators will automatically identify and locate the specific UI where any mask violation occurred. Built-in measurements such as eye height, eye width, and eye opening are critical to gaining a quantitative understanding of the system performance. With simultaneous eye measurements it is easy to compare performance across multiple testing views.
The bursted nature of DDR signals makes it very different than most serial data communication standards. As a result, the traditional oscilloscope-based methods and algorithms for measuring jitter and analyzing system performance are not capable of measuring DDR signals. The DDR Debug Toolkit uses jitter algorithms which have been tailored for bursted DDR signals. Built-in DDR measurement parameters provide various JEDEC compliance measurements which are important for debugging and characterizing DDR systems.

### Four Measurement Views
When configuring a measurement, each view can be independently assigned a signal providing extensive flexibility for analysis. For example, it is simple to setup a comparison of system performance between read and write burst operation across multiple DQ lanes. Simultaneous analysis of up to four measurement views simplifies the measurement process and eliminates concerns about making unsynchronized measurements.

### DDR Jitter Analysis
Bursted DDR signals create undesirable complications and challenges for traditional serial data analysis and jitter tools preventing analysis of DQ, DQS and address signals. Jitter parameters including Tj, Rj, and Dj are calculated across all active DDR measurement views. To gain a deeper understanding of the jitter distribution, traditional displays such as TIE histograms, TIE track, and bathtub curves are available.

### DDR-Specific Parameters
With a toolbox of parameters specific to DDR it is simple to quickly configure insightful measurements for validation, characterization, and debug. Up to 12 configurable measurements can be displayed and analyzed simultaneously across all active measurement views. For each measurement, advanced statistics such as min, max, mean, and number of measurement instances can be displayed and easily located with the searchable zoom feature.
Key Features

Complete test coverage as described by JEDEC specifications

Supports all standard and custom speed grades

Separate bursts using DQ-DQS phase or DDR command bus

Statistically relevant results achieve measurement confidence

Report generation with pass/fail results and fully annotated worst case measurement screenshot

DDR Debug Toolkit integration for easy and flexible debug

Maximize signal integrity with de-embedding and Virtual Probing

Leverages industry leading serial data algorithms for jitter breakdown and eye rendering

Accurate Burst Separation

Read and Write bursts can be separated based on DQ-DQS phase or based on the command bus when used in conjunction with the HDA125 High-speed Digital Analyzer. The HDA125 enables bursts to be separated using the commands sent from the controller, allowing for accurate burst separation even in situations with non-ideal signal integrity (e.g. reflections).

Measurement Confidence

Due to the high level of variability in DDR measurements, it is important to make statistically relevant measurements to fully characterize a DDR interface. By measuring thousands of cycles in one acquisition, the user can be more confident that they are catching the true maximum and minimum points for their measurement.

Most Flexible DDR Debug

QualiPHY DDR packages use the DDR Debug Toolkit to perform all compliance testing. Using the “Stop on Test” feature, the user can pause testing after each individual test and clearly see where the worst case measurement occurred. At that point the DDR Debug toolkit can be leveraged for further debug and upon completion, testing can be seamlessly resumed with one click of a button.

Fully Annotated Screenshots

In addition to the measured value and the pass/fail status for each test, QualiPHY reports contain screenshots of the worst case measurement for each test. Each screenshot is fully annotated including trace labels and pertinent voltage levels.
QualiPHY

QualiPHY is designed to reduce the time, effort, and specialized knowledge needed to perform compliance testing on high-speed serial buses.

- Guides the user through each test setup
- Performs each measurement in accordance with the relevant test procedure
- Compares each measured value with the applicable specification limits
- Fully documents all results
- QualiPHY helps the user perform testing the right way — every time

Compliance Reports contain all of the tested values, the specific test limits and screen captures. Compliance Reports can be created as HTML, PDF or XML.

Eye Diagram Tests

Clock Tests

Timing Tests

Electrical Tests
Key Features

12.5 GS/s sampling rate for 80ps timing accuracy

3 GHz leadset for capturing digital signals up to 6 Gb/s

Add high-speed mixed-signal capability to your Teledyne LeCroy high-bandwidth oscilloscope

- LBUS connection for precise timing synchronization
- USB 3.1 for fast data transfer

Unique QuickLink probing system

- Differential solder-in tips with 9-inch lead simplify access to difficult test points
- Ultra low loading for superior performance
- 8 GHz bandwidth tips are compatible with both HDA digital leadset and Teledyne LeCroy WaveLink differential analog probes for unmatched acquisition flexibility

The HDA125 transforms your Teledyne LeCroy oscilloscope into the highest-performance, most flexible mixed-signal solution for high-speed digital debug and evaluation. With 12.5 GS/s digital sampling rate on 18 input channels, and the revolutionary QuickLink probing solution allowing seamless transitions from digital to high-bandwidth analog acquisitions, validation of challenging interfaces such as DDR4 has never been simpler or more comprehensive.

Complete Embedded System Debug

Modern embedded systems increasingly utilize high-speed digital buses, posing new and evolving challenges to validation and debug engineers. While analog signal-integrity characterization is a critical part of this process, the ability to decode and trigger on related digital buses is becoming a vital capability. The HDA125 High-speed Digital Analyzer addresses this need with the most flexible solution available.

Unique probing solution

One of the most challenging aspects of high-speed embedded test is simply getting the signals from the system under test to the instrumentation with sufficient fidelity. The HDA125 is built around Teledyne LeCroy’s revolutionary QuickLink probing concept - enabling high signal quality, easy access to remote test points, and simple transitions from digital to analog probing.

Enhanced DDR Debug

Teledyne LeCroy already offers the industry’s only dedicated DDR Debug Toolkit, designed to simplify challenging memory interface validation. Adding the HDA125 allows the DDR command bus to be directly acquired and integrated into the analysis, enabling advanced command triggering and sophisticated, searchable bus state viewing.
Command Bus Capture for Full Interface Visibility
Basic debugging and validation of embedded DDR interfaces typically involves analysis of the analog properties of the clock, data (DQ) and strobe (DQS) signals - and Teledyne LeCroy’s DDR analysis tools are established industry leaders in this application. But when validation tasks become more complex and problems require deeper insight, the ability to trigger on, acquire and visualize the state of the DDR command bus is invaluable. The HDA125 brings command bus acquisition to Teledyne LeCroy’s already comprehensive toolset, providing the ultimate in memory bus analysis capability.

Analyze Bus Activity
The HDA125 enables the unique “bus view” feature of the DDR Debug Toolkit, which brings Teledyne LeCroy’s advanced bus analysis feature set to bear on DDR analysis. View bus activity in tabular form, and move time-correlated views to a desired event with the touch of a button. Search for specific events and bus states within the acquired record. Intuitive color overlays and annotations make it easy to identify areas of interest in the acquired analog waveforms.

Trigger on DDR Commands
The ability to trigger on specific states of the command bus becomes an invaluable tool for quick understanding of DDR signal quality. The HDA125’s logic triggering combines with the DDR Debug Toolkit’s intuitive setup and intelligent software cross-triggering to provide the ultimate DDR triggering system. Persistence maps of read and write bursts provide an easy and fast means of identifying subtle signal-quality problems for further investigation.
Key Features

Fast and Easy Debug for DDR3 and DDR4
- Self-contained system offers easy connection and setup
- Custom probe design supports higher speed modules
- No calibration needed!
- Free trace viewer runs on any PC

Comprehensive JEDEC Trigger and Capture
- Detects over 65 JEDEC bus event & timing violations in real time
- Extended recording time captures 4X the memory events vs. Logic Analyzer
- Interposers capture SPD data for fast configuration of the analyzer
- Dedicated trigger output to scope for Read/Write operations

Innovative Displays
Focused on Timing Analysis
- Traditional State and Timing Waveform views
- Visualize I/O distribution with the Bank State View
- Bus metrics are tracked per bank and per DIMM slot
- Real Time performance displays

Flexible, Scalable Platform
- Monitor two slots of quad rank DDR3 or DDR4 DIMMs concurrently
- Supports registered and unbuffered DIMM types
- Address multi-channel application by cascading analyzers

Kibra™ 480 DDR4 Protocol Analyzer
Kibra™ 480 is a stand-alone protocol analyzer that provides comprehensive DDR3 and DDR4 JEDEC timing analysis. Based on the ground breaking Kibra 380, the 480 platform introduces proprietary probing technology designed to non-intrusively monitor higher speed DDR3 as well as the new DDR4 specification without time consuming calibration and setup. Sitting in-line on a live system, the analyzer records bus traffic while automatically identifying timing and protocol violations. It displays both commands and errors using a full function waveform viewer allowing fast debug of memory devices and controllers.

Proprietary Probe Design for higher speed memory
Teledyne LeCroy developed a custom ASIC for the Kibra 480 probe to support higher speed DDR modules. This proprietary probe implementation allows loss-less capture of DDR3 to 2133 MT/s; and DDR4 to 2400 MT/s and higher. The probes are self-powered to provide instant signal lock – including reliable capture of the DDR4 power-on sequence. Separate probes are available for DDR3 and DDR4 supporting UDIMM/RDIMM/LRDIMM and SODIMM as well as the newer hybrid NVDIMMs.

Easy Setup – No Calibration Needed!
Start using the Teledyne LeCroy Kibra 480 immediately without time consuming calibration. Simply enter the memory controller parameters and start recording. The software will automatically load JEDEC trigger values for the DIMM type specified. Users can selectively disable or override any of the JEDEC triggers on-the-fly.

JEDEC timing values load automatically based on memory parameters.
Accurate wave-form display of all physical address attributes (RA, CA, BA, CS)

Timing Navigation bar allows fast zoom-in

Annotate and analyze traces with custom markers

State listing shows all command information including timing errors

Visualize I/O distribution with the Bank State View

Use event metrics to navigate to individual commands, addresses or violations

Traffic Summaries for Faster Analysis
In addition to timing analysis, the Kibra 480 generates performance metrics that are displayed for read, write and power down operations. Bus metrics are tracked per bank, per rank, and per channel to provide insights into overall memory utilization. The error report shows protocol and timing violations with hyperlinks to the error in question.
### Product Description

#### Physical Layer Debug – DDR Debug Toolkit

<table>
<thead>
<tr>
<th>Product Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR2-TOOLKIT*</td>
<td>DDR2 and LPDDR2 Debug Toolkit</td>
</tr>
<tr>
<td>DDR3-TOOLKIT*</td>
<td>DDR3, DDR3L, LPDDR3, DDR2, and LPDDR2 Debug Toolkit</td>
</tr>
<tr>
<td>DDR4-TOOLKIT*</td>
<td>DDR4, DDR3, DDR3L, LPDDR4, LPDDR3, DDR2, and LPDDR2 Debug Toolkit</td>
</tr>
<tr>
<td>VIRTUALPROBE*</td>
<td>Advanced De-embedding, Emulation and Virtual Probing Toolkit</td>
</tr>
</tbody>
</table>

* Exact ordering part numbers can be obtained from pre-pending the oscilloscope model prefix from the list below. For example, the part number for DDR4-TOOLKIT on the WaveMaster 8 Zi-B would be "WM8Zi-DDR4-TOOLKIT".

#### Physical Layer Compliance – QualiPHY

<table>
<thead>
<tr>
<th>Product Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>QPHY-DDR2</td>
<td>QualiPHY Enabled DDR2 Software Option</td>
</tr>
<tr>
<td>QPHY-LPDDR2</td>
<td>QualiPHY Enabled LPDDR2 Software Option</td>
</tr>
<tr>
<td>QPHY-DDR3</td>
<td>QualiPHY Enabled DDR3, DDR3L, and LPDDR3 Software Option</td>
</tr>
<tr>
<td>QPHY-DDR4</td>
<td>QualiPHY Enabled DDR4 and LPDDR4 Software Option</td>
</tr>
<tr>
<td>VIRTUALPROBE*</td>
<td>Advanced De-embedding, Emulation and Virtual Probing Toolkit</td>
</tr>
</tbody>
</table>

* Exact ordering part numbers can be obtained from pre-pending the oscilloscope model prefix from the list below.

#### High-speed Digital Analyzer

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>WM8Zi</td>
<td>12.5 GS/s High-speed Digital Analyzer with 8 Channel QuickLink leadset and LBUS connection</td>
</tr>
<tr>
<td>WM8Zi</td>
<td>12.5 GS/s High-speed Digital Analyzer with 9 Channel QuickLink leadset and LBUS connection</td>
</tr>
</tbody>
</table>

#### Kibra Analyzers

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR-T0S3-D01-X</td>
<td>Kibra 380 DDR3 Standard Analyzer Base System</td>
</tr>
<tr>
<td>DDR-T0S3-D02-X</td>
<td>Kibra 480 DDR3 Standard Analyzer Base System</td>
</tr>
<tr>
<td>DDR-T0P4-D02-X</td>
<td>Kibra 480 DDR4 Pro Analyzer Base System</td>
</tr>
</tbody>
</table>

#### Kibra Compliance Analyzers

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR-CS03-D02-X</td>
<td>Kibra 480 DDR3 Compliance Analyzer</td>
</tr>
<tr>
<td>DDR-CS04-D02-X</td>
<td>Kibra 480 DDR4 Compliance Analyzer</td>
</tr>
</tbody>
</table>

#### DDR Protocol

<table>
<thead>
<tr>
<th>Bandwidth</th>
<th>Oscilloscope</th>
<th>Probe</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR2 (All Speeds)</td>
<td>WaveRunner 8404M</td>
<td>D410-A/PS / D420-A/PS (Qty. 3 or 4)</td>
</tr>
<tr>
<td>DDR2 (1600 MT/s or less)</td>
<td>WavePro 760Zi-A</td>
<td>D610-A/PS / D620-A/PS (Qty. 3 or 4)</td>
</tr>
<tr>
<td>DDR3 (1866 MT/s or more)</td>
<td>WaveMaster 808Zi-B</td>
<td>D830-P (Qty. 3 or 4)</td>
</tr>
<tr>
<td>DDR4 (All Speeds)</td>
<td>WaveMaster 813Zi-B</td>
<td>D1330-P (Qty. 3 or 4)</td>
</tr>
<tr>
<td>LPDDR4 (All speeds)</td>
<td>WaveMaster 813Zi-B</td>
<td>D1330-P (Qty. 3 or 4)</td>
</tr>
</tbody>
</table>

Please visit teledynelecroy.com for the most up to date compatibility and ordering information.