Verification of USB Software Stack in a Development System  
(USB 2.0 Slow Clock Option)  
Matthew Dunn  
Teledyne LeCroy

Introduction

When developing a USB software stack which is to be embedded in an FPGA or ASIC, it is often desirable to verify the implementation by using a accelerator or debugger.

However in either case it is not normally possible to run the system at the final system speed. FPGA debuggers can reduce the system speed typically by a factor of 10-100. ASIC simulation systems such as the Mentor Graphics Veloce™ hardware accelerator may run at a factor of 125 slower than final design speeds.

Protocol analysers are the most common test tools used to validate logical link and application layers in USB systems. Teledyne LeCroy’s USBTracer/Trainer™ and the Teledyne LeCroy Voyager M3i include special functionality to analyze traffic at slower than standard clock rates. This technical brief looks at the various ways of using these two test systems to validate a design before it is committed to silicon.

Speed Control

The first part of the process is to determine what the bit clock speed is in the development system. Ideally it may be possible to expose the development system’s USB bit clock to a physical pin for testing. Live USB has a bit clock as per the table below:

<table>
<thead>
<tr>
<th>Speed</th>
<th>Clock Speed</th>
</tr>
</thead>
<tbody>
<tr>
<td>High Speed</td>
<td>480.0 MHz</td>
</tr>
<tr>
<td>Low Speed</td>
<td>1.5 MHz</td>
</tr>
</tbody>
</table>

Depending on the type of traffic being generated (High, Full, Low) we can divide the development system’s bit clock into the standard USB clock and determine the factor to enter in the USB analyser.

For the Teledyne LeCroy USBTracer/Voyager Product Family of USB Analysers, the control for slowing the clock down requires that the auto speed detect be disabled and the target speed is selected. The example in Figure 1 shows a factor of 6 being used to set the bit clock to 2 MHz. This option affects both the analyser and the exerciser if fitted.

![Figure 1: Slow Clock Options for Voyager](image-url)

Note: The slow clock feature for High speed USB is an additional license option which is only enabled when licensed hardware is attached.
The Teledyne LeCroy Family of USB analysers also have a facility for working with slow USB clocks. The control for this is found in the project setting tab for the analyser and host exerciser. The device emulation project also has a similar option on the setting tab.

![Figure 2: Slow Clock Options for Teledyne LeCroy SBAE30](image)

When using the Teledyne LeCroy SBAE30 system, the settings tab provides four fixed division factors for specifying slow clock timing. There is an additional option to provide an external reference clock. The external clock should operate in the range of

<table>
<thead>
<tr>
<th>Clock</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>High Speed</td>
<td>400 KHz – 8 MHz</td>
</tr>
<tr>
<td>Low/Full Speed</td>
<td>1 KHz – 100 KHz 400 KHz – 8 MHz</td>
</tr>
</tbody>
</table>

The external clock does not have to come from the system under test (although this is preferred), and so a signal generator could be used if needed. The caveat here is that the difference in clock rates needs to be minimised to avoid spurious bit errors being recorded by the analyzer as the system clock and reference clock drift independently. Providing the external clock to the accelerator too may be advantageous in this situation.

## Two Ends to a Link

USB is a master-slave point-to-point protocol. Comprehensive test coverage for a USB link requires both host and device functionality. Depending on the designed function (or functions) of the system under development, a reference system capable of running at the reduced speed is required. In some cases, where the system under development supports both, host and device functions, two such systems could be connected and the analyser (running to match the reduced system speed) can be used to verify the protocol. However it is not recommended that a single IP source be used to validate a design. Additionally it is desirable to be able to run the USB-IF’s Chapter 9 tests and other tests designed to verify if the IP under development responds correctly to errors or unusual conditions.

Using a USB host or device exerciser such as the USB Tracer/Trainer, Voyager or the Teledyne LeCroy SBAE30 can solve this problem. The precise type of testing required may determine which of the exerciser optimisations are most suited to the tests. Factors which affect the choice are the bit clock rate required, whether host or device emulation is needed and the types of protocol errors required to be generated. Using the exerciser to emulate one-half of the link provides substantially greater test coverage than testing against the same IP at both ends (e.g., in a loopback).

## A Question of Interfaces

The analyser probes and exerciser ports are
designed to work with USB-compliant electrical signalling. Consequently for a successful emulation to operate either a PHY must be synthesised in the IP under test or a non-standard interface implementation specific interface must be developed.

It may be possible to use a standard external PHY if it can also be slowed to the same bit rate as the system is running at.

Single-ended solutions connected to the Data line are not suitable for USB testing, because USB uses special states in the differential path to carry side band information (such as Reset signalling and end of packet markers). SE0 cannot be created with a single ended source so both D+ and D- must be provided.

For some hardware acceleration systems such as the Mentor Graphics VStation™, Teledyne LeCroy provides an optional board (part # EM316) that adapts a standard USB connector to the SCSI-100 connector on the accelerator. For more information on this adapter please see Teledyne LeCroy’s application note “Using the EM316 Adapter”.

Another note of caution would be that USB uses 300-400mv signalling levels, although it is the transitions not the voltage levels that are key. However the Trainers inputs although fairly tolerant, will not support infinitely high voltages. It may be needed to reduce the output voltage from the accelerator to match. Care would be needed to ensure the ability to drive the USB data lines with sufficient current to meet the rise/fall requirements (although these become more tolerant as the emulation speed goes down).

**Testing a USB Device**

The Teledyne LeCroy exercisers can emulate USB host behaviour to test USB device implementations and functionality. Tests such as verification of retransmission protocols in the event of an error, tolerance to unsupported frame structures and tolerance to poor frame timing, can be performed in addition to USB Spec Chapter 9 testing. A typical setup might look like Figure 3, below.

![Figure 3](image)

If the Teledyne LeCroy USB Trainer / Voyager is used with the slow clock option then the BitStream™ mode should be used. The Vbus supply will come from either the Teledyne LeCroy USB Trainer/Voyager or the SBAE30 (depending on which is used) and should not be connected to any power supplied from the accelerator or debugger. The Accelerator or debugger will need to provide the correct USB pull-up signalling to indicate if it is appearing as a HS/FS device or LS device.

**Testing a USB Host**

Using a USB device exerciser, USB host implementations and functions can be tested. This sort of testing is generally a little more complex since the device emulator must respond to the host requests in the order requested, and the exerciser will need to be programmed with appropriate endpoint and function codings. A typical USB device
emulation setup might look like Figure 4, below.

If a suitable bit clock reference signal is not available from the accelerator, an external signal generator can be used to provide a suitable reference frequency.

Testing True OTG Systems

A true OTG system is one that supports the HNP protocol to change host/device role dynamically after initial connection. Systems that support either a host mode or a device mode but do not support HNP can be best tested using the two previous setups. True Native OTG devices can also be tested with those setups. However, to test the HNP and SRP extensions to the USB protocol from the OTG addendum, the OTG test port on the Teledyne LeCroy SBAE30 should be used. This is designed to aid the testing of dual role capable devices which support dynamic role reversal. Figure 5 shows a suggested setup with the SBAE-30 exerciser for OTG emulation. This illustration uses a combination of Teledyne LeCroy USB Analyser/Exerciser.

The USBTracer specifically supports the VBus signalling protocol of OTG. When using a slow clock, the USBTracer’s OTG configuration file (OTGTimingParam.txt in the applications install directory) should be modified to accommodate the “slowed” timings for OTG sideband signalling to be verified correctly.

Reading the Trace

Traces recorded while using the slow clock option will look essentially identical to traces running at normal speeds. The primary difference will be noted in the delta timings between the packets—these will be substantially larger than normal. The application software will automatically adjust the timing analysis of recorded traces to compensate for the reduced clocking scheme.